Analytical Modeling of a ZVS Bidirectional Series Resonant DC-DC Converter

Aleksandar Vuchev[1], Nikolay Bankov[2], Yasen Madankov[3] and Angel Lichev[4]

Abstract – **The present article considers a bidirectional series resonant DC-DC converter, operating above the resonant frequency. The conditions of operation with ZVS are discussed. The processes in the converter resonant tank circuit are presented on the basis of well-known analytical models and their coefficients are defined. The obtained theoretical results are compared with those from simulation in the environment of OrCAD PSpice.**

Keywords – **Bidirectional Series Resonant DC-DC Converter, ZVS, Phase-Shift Control.**

I. INTRODUCTION

The bidirectional DC-DC converters are suitable for different applications where it is necessary to control the electrical energy transmission [3], such as in motor drives [4, 8], grids with renewable energy sources [6, 9], etc. They are realized on the base of two inverter stages. For connection between the inverters, a single inductance can be used [5, 9].

It is long known that series resonant DC-DC converters can also be used for bidirectional energy transfer [1, 3, 4]. They have various advantages, one of which is the possibility of significant switching loss reduction. When the converters operate above the resonant frequency, it is really possible that their power devices switch at zero voltage (ZVS – Zero Voltage Switching) [2]. This makes them a preferred solution for different applications.

There is a plenty of investigations [3, 4, 7, 10] of bidirectional series resonant DC-DC converters operating at higher than their resonant frequency. They show that the characteristics of the considered solutions depend on the applied control technique to a significant extend. It is known that these characteristics can be obtained as a result of modelling of the converter resonant tank circuit processes [2]. In general, this is the description of the variation of the

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inductor current and the capacitor voltage. These models are well-known, but their coefficients depend on the converter circuit and the used control technique.

The current work presents analytical modelling of the resonant tank circuit processes of bidirectional series resonant DC-DC converter operating above the resonant frequency. For this purpose, well-known analytical models are used and their coefficients are determined for the considered circuit.

II. PRINCIPLE OF THE CONVERTER OPERATION

Circuit of the examined converter is presented in Fig. 1. It consists of two identical bridge inverter stages, resonant tank circuit (L, C), matching transformer Tr, capacitive input and output filters (C_d и C_0). Fig. 1 also presents the snubber capacitors $C_1 \div C_8$ by which a zero voltage switching is obtained.

A voltage U_d is applied to the DC terminals of the „input" inverter stage (transistors $Q_1 \div Q_4$ with freewheeling diodes $D_1 \div D_4$), and a voltage U_0 – to those of the „output" stage (transistors $Q_5 \div Q_8$ with freewheeling diodes $D_5 \div D_8$).

Depending on the energy transfer direction, two operating modes are possible for the converter. The first of them is called **DIRECT MODE**. In this mode, it is assumed that energy flows from the „input" to the „output", i.e. from the source of voltage U_d to the one of voltage U_0. The second is **REVERCE MODE**. In this mode, the energy flows from the
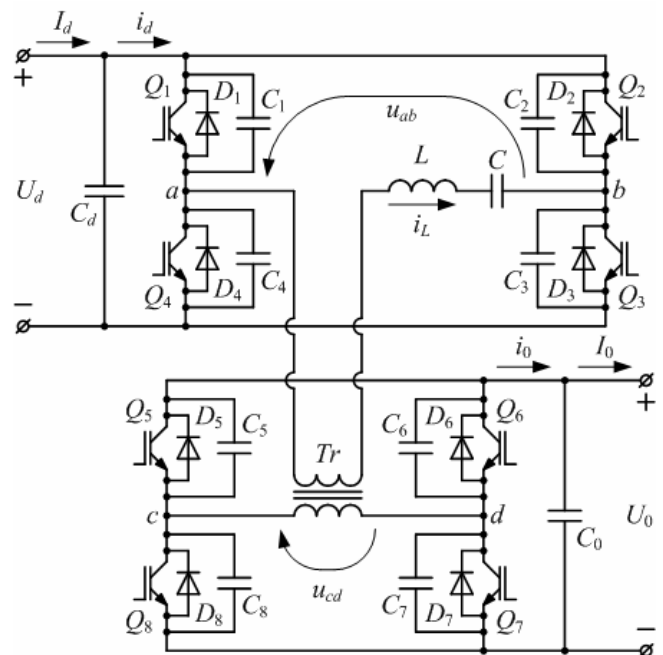

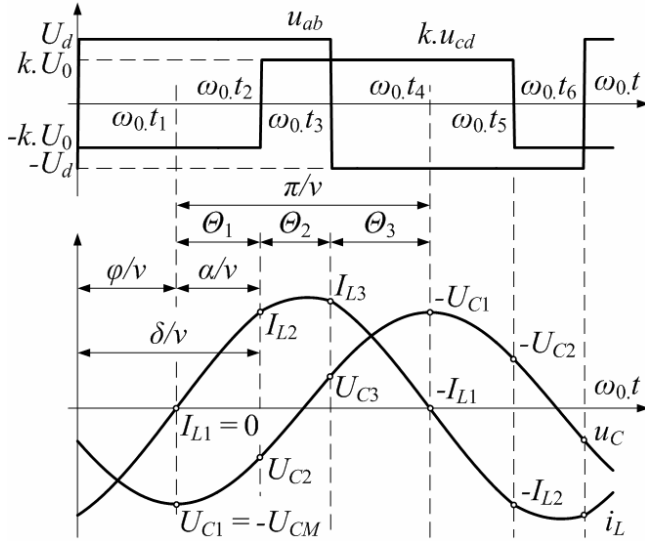Fig. 1. Circuit of the Bidirectional Resonant DC/DC Converter

Fig. 2. Waveforms at **DIRECT MODE**

Fig. 3. Waveforms at **REVERCE MODE**

„output" to the „input" (from U_0 to U_d).

The waveforms, shown in Fig. 2, illustrate the converter operation in **DIRECT MODE**, and those in Fig. 3 – in **REVERCE MODE**.

Independently from the mode, the converter operates at constant frequency ω_S, which is higher than the resonant ω_0. Therefore, the transistor pairs of the „input" stage (Q_1, Q_3 or Q_2, Q_4) operate at ZVS. They are controlled in such a way that the voltage u_{ab} has almost square-wave form and amplitude U_d. Along with this, the resonant current i falls behind the voltage u_{ab} at an angle φ. The transistors of the „output" stage also operate at ZVS. Therefore, when the current i passes through zero, the corresponding pair (Q_5, Q_7 or Q_6, Q_8) begins conducting. This pair switches off after time, corresponding to an angle δ, accounted to the moment of switch-off of the „input" stage transistors that conducted in the same half cycle. The voltage u_{cd}, which also has almost square-wave form and amplitude U_0, is shifted in time from u_{ab}. In this way, the output power control is obtained by phase-shifting – the variation of the angle δ.

Angle φ corresponds to the conduction time of the „input" stage freewheeling diodes, and angle α – to the conduction time of the „output" stage transistors. When $\varphi < \pi/2$ and $\alpha < \pi/2$, energy is transferred in „forward" direction, and when $\varphi > \pi/2$ and $\alpha > \pi/2$ – in „reverse" direction. From Figs. 2 and 3, it can be observed that the following equation is valid: $\varphi + \alpha = \delta$. Therefore, when $\delta > \pi$, **REVERCE MODE** is observed, and when $\delta < \pi$ – **DIRECT MODE**.

Angles φ, α and δ are related to the operating frequency ω_S.

III. MODELING OF THE CONVERTER OPERATION

For the purposes of the analysis, the following assumptions are made: the matching transformer is ideal with a transformation ratio k, all the circuit elements are ideal, the influence of the snubber capacitors $C_1 \div C_8$ and the ripples of the „input" voltage U_d and the „output" voltage U_0 are neglected, i.e. voltages u_{ab} and u_{cd} have rectangular shape.
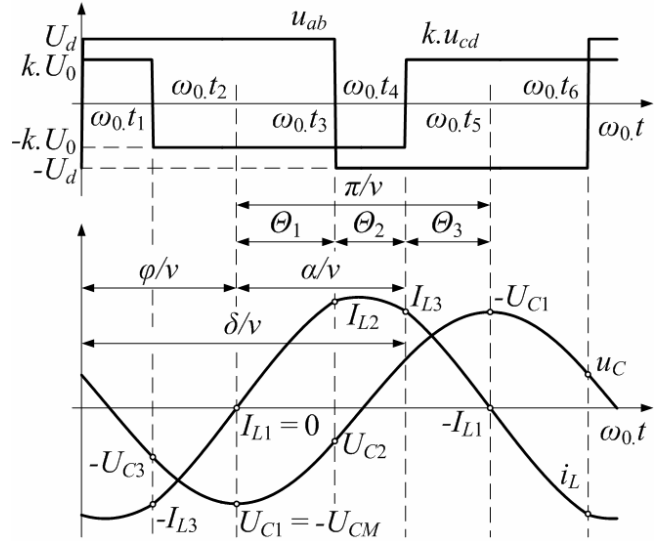
The waveforms (Figs. 2 and 3) show that, independently from the converter mode, any of the half cycles can be divided into three intervals. For each of them, an equivalent DC voltage U_{EQ}, defined by the values of u_{ab} and u_{cd}, is applied to the resonant tank circuit. This fact allows only the resonant tank circuit processes to be investigated. Therefore, apart from the waveforms of the current i_L through the inductor L and the voltage u_C across the capacitor C, Figs. 2 and 3 show the initial values ($I_{C1} \div I_{L3}$, $U_{C1} \div U_{C3}$) for each of the mentioned intervals.

In accordance with the assumptions made, the resonant frequency, the characteristic impedance and the frequency detuning are:

$$\omega_0 = 1/\sqrt{LC} \; ; \; \rho_0 = \sqrt{L/C}; \; \nu = \omega_S/\omega_0 \qquad (1)$$

Because of the similarity, the modelling of the resonant tank circuit processes is realized in the same way as in [2]. For each of the half cycle intervals, the current i_L and the voltage u_C values are determined as follows:

$$i_{Lj}(\theta) = I_{Lj}\cos\theta - \frac{U_{Cj} - U_{EQj}}{\rho_0}\sin\theta \qquad (2)$$
$$u_{Cj}(\theta) = \rho_0 I_{Lj}\sin\theta + \left(U_{Cj} - U_{EQj}\right)\cos\theta + U_{EQj}$$

where j is the number of the considered interval; I_{Lj} and U_{Cj} are the inductor current and the capacitor voltage values at the beginning of the interval; $\theta = 0 \div \Theta_j$; Θ_j – angle of the interval for the resonant frequency ω_0; U_{EQj} – the value of the equivalent DC voltage applied to the resonant tank circuit.

Actually, the parameters I_{Lj}, U_{Cj} и U_{EQj} represent coefficients of the modelling Eqs. (2).

In order to obtain generalized results, all the quantities are normalized as follows: the voltages according to U_d; and the currents – according to U_d/ρ_0. Then, Eqs. (2) are transformed and in normalized form are:

$$i'_{Lj}(\theta) = I'_{Lj}\cos\theta - \left(U'_{Cj} - U'_{EQ_j}\right)\sin\theta$$
$$u'_{Cj}(\theta) = I'_{Lj}\sin\theta + \left(U'_{Cj} - U'_{EQ_j}\right)\cos\theta + U'_{EQ_j} \tag{3}$$

where the normalized values of the corresponding quantities are marked with the prime symbol.

From Figs. 2 and 3 it is observed that the value of i_L at the end of given interval appears to be initial value for the following one. The same applies to the voltage u_C. Therefore:

$$I'_{Lj+1} = I'_{Lj}\cos\Theta_j - \left(U'_{Cj} - U'_{EQ_j}\right)\sin\Theta_j$$
$$U'_{Cj+1} = I'_{Lj}\sin\Theta_j + \left(U'_{Cj} - U'_{EQ_j}\right)\cos\Theta_j + U'_{EQ_j} \tag{4}$$

Taking into consideration that $I_{L3} = -I_{L1}$ and $U_{C3} = -U_{C1}$, after recursion of the Eqs. (4) the following system is obtained for the three consecutive intervals in a half cycle:

$$I'_{L1}\left(1 + \cos\frac{\pi}{\nu}\right) - U'_{C1}\sin\frac{\pi}{\nu}$$
$$= \sum_{j=1}^{3} U'_{EQ_j}\left[\sin\left(\frac{\pi}{\nu} - \sum_{i=1}^{j}\Theta_i\right) - \sin\left(\sum_{i=j}^{3}\Theta_i\right)\right] \tag{5}$$

$$I'_{L1}\sin\frac{\pi}{\nu} + U'_{C1}\left(1 + \cos\frac{\pi}{\nu}\right)$$
$$= \sum_{j=1}^{3} U'_{EQ_j}\left[\cos\left(\sum_{i=j}^{3}\Theta_i\right) - \cos\left(\frac{\pi}{\nu} - \sum_{i=1}^{j}\Theta_i\right)\right] \tag{6}$$

It is convenient the interval at which the initial values are $I_{L1} = 0$ and $U_{C1} = -U_{CM}$ to be chosen as first. In this case, the parameters Θ_j and U'_{EQj} are defined on the base of the waveforms (Figs. 2 and 3). Their values are presented in Table I for each of the two operating modes.

TABLE I

MODE	Parameter	Number of interval		
		1	2	3
DIRECT	Θ_j	$\dfrac{\delta - \varphi}{\nu}$	$\dfrac{\pi - \delta}{\nu}$	$\dfrac{\varphi}{\nu}$
	U'_{EQj}	$1+kU'_0$	$1-kU'_0$	$-1-kU'_0$
REVERCE	Θ_j	$\dfrac{\pi - \varphi}{\nu}$	$\dfrac{\delta - \pi}{\nu}$	$\dfrac{\pi - \delta + \varphi}{\nu}$
	U'_{EQj}	$1+kU'_0$	$-1+kU'_0$	$-1-kU'_0$

As $I'_{L1} = 0$, after substitution of the actual values for U'_{EQj} in Eqs. (5) and (6), expressions for the voltages U'_0 and U'_{CM} are obtained. Thus, for the **DIRECT MODE** the following normalized dependencies are obtained:

$$U'_0 = \frac{1}{k}\frac{\sin(\Theta_1 + \Theta_2) - \sin(\Theta_3)}{\sin(\Theta_2 + \Theta_3) - \sin(\Theta_1)} \tag{7}$$

$$U'_{CM} = 2\frac{\sin(\Theta_3) + U'_0\sin(\Theta_2 + \Theta_3)}{\sin(\pi/\nu)} - \left(1 + kU'_0\right) \tag{8}$$

Respectively, for the **REVERCE MODE** the following is obtained:

$$U'_0 = \frac{1}{k}\frac{\sin(\Theta_1) - \sin(\Theta_2 + \Theta_3)}{\sin(\Theta_3) - \sin(\Theta_1 + \Theta_2)} \tag{9}$$

$$U'_{CM} = 2\frac{\sin(\Theta_2 + \Theta_3) + U'_0\sin(\Theta_3)}{\sin(\pi/\nu)} - \left(1 + kU'_0\right) \tag{10}$$

When the values for the angles Θ_j are substituted in the above equations, identical expressions are obtained for the two operating modes:

$$U'_0 = \frac{1}{k}\frac{\sin\left(\dfrac{\pi - \varphi}{\nu}\right) - \sin\left(\dfrac{\varphi}{\nu}\right)}{\sin\left(\dfrac{\pi - \delta + \varphi}{\nu}\right) - \sin\left(\dfrac{\delta - \varphi}{\nu}\right)} \tag{7}$$

$$U'_{CM} = 2\frac{\sin\left(\dfrac{\varphi}{\nu}\right) + U'_0\sin\left(\dfrac{\pi - \delta + \varphi}{\nu}\right)}{\sin\left(\dfrac{\pi}{\nu}\right)} - \left(1 + kU'_0\right) \tag{8}$$

Now, after calculation of the U'_0 and U'_{CM} values, the other coefficients of the model – the initial values of the current i'_L through the inductor and the voltage u'_C across the capacitor, can also be determined for the second and the third intervals. For this purpose, Eqs. (4) are used.

Analyzing the obtained dependencies, it can be observed that all the model coefficients are expressed by two angles. One of them is the control angle δ, which represents a parameter. The other angle is φ. Its value depends on the converter load. In other words, the model coefficients are determined in accordance with the value of the control parameter δ for a determined load expressed by the angle φ.

TABLE II

MODE	Angle δ	Angle φ
DIRECT	$0 \div \pi/2$	$0 \div \delta$
	$\pi/2 \div \pi$	$0 \div \pi/2$
REVERCE	$\pi \div 3\pi/2$	$\pi/2 \div \pi$
	$3\pi/2 \div 2\pi$	$\delta - \pi \div \pi$

During the calculations, the limits of the angle φ variation must be taken into consideration. They depend on the operating mode, as well as, on the value of angle δ. The possible limits are presented in Table II.
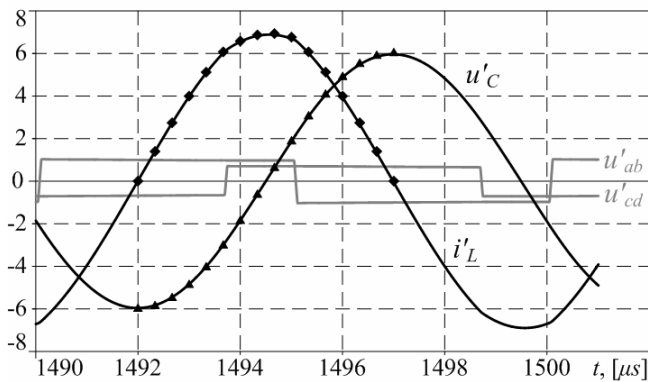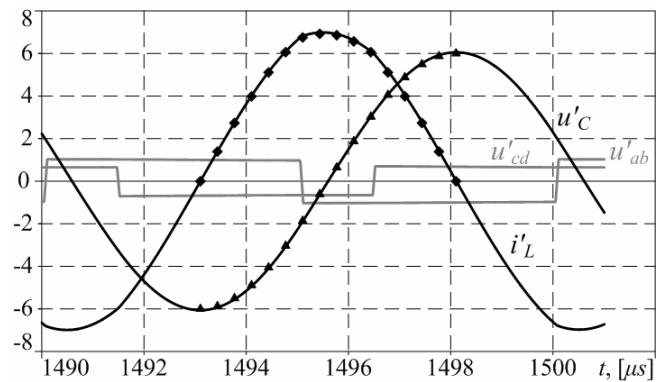
Fig. 4. Comparison at *DIRECT MODE*

Fig. 5. Comparison at *REVERCE MODE*

IV. RELIABILITY OF THE RESULTS

For verification of their authenticity, the results from the accomplished modeling are compared to ones obtained from computer simulations. For this purpose, a model of a bidirectional series resonant DC-DC converter operating above the resonant frequency is realized in the environment of OrCAD PSpice. The simulation model has the following main parameters: Input source voltage – U_d = 200V; Resonant tank circuit inductance – L = 223,332μH; Resonant tank circuit capacitance – C = 15nF; Operating frequency – f_S = 100kHz; Frequency detuning – ν =1,15; Transformation ratio k = 1.

The obtained simulation results are normalized in the same way as the values from the above presented modelling. Comparison in graphic form for the *DIRECT MODE* is presented in Fig. 4, and for the *REVERCE MODE* – in Fig. 5. The waveforms of the voltages u_{ab}, u_{cd}, u_C and the current i_L obtained from the computer simulations are shown with thick lines. The calculation results are presented by means of symbols (♦ – for the current i_L and ▲ – for the voltage u_C). The examinations for the *DIRECT MODE* are accomplished at δ = 0,722π and φ = 0,389π (U'_0 = 0,67972), and for the *REVERCE MODE* – δ = 1,278π and φ = 0,611π (U'_0 = 0,67972).

A very good coincidence between the results obtained from the simulations and from the calculations is observed from the charts. This is also confirmed by the accomplished examinations for other converter operating points.

V. CONCLUSION

A modelling of the resonant tank circuit processes of bidirectional series resonant DC-DC converter operating above the resonant frequency is executed. For this purposes, well-known analytical models are used with their coefficients being determined for the considered circuit.

Computer simulations are accomplished, the results of which show very good coincidence with those from the analytical modelling.

The obtained models can be used for future investigation and design of such converters.

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Load and Control Characteristics of a ZVS Bidirectional Series Resonant DC-DC Converter

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Abstract – **The present paper considers a bidirectional series resonant DC-DC converter, operating above the resonant frequency. On the basis of a well-known analytical modelling of the resonant tank circuit processes, a sequence for determination of the main converter quantities is proposed. As a result, its normalized load and control characteristics are built.**

Keywords – **Bidirectional Series Resonant DC-DC Converter, ZVS, Phase-Shift Control.**

I. INTRODUCTION

The well-known series resonant DC-DC converter operating at frequency higher than the resonant one [2] has a significant disadvantage. It does not allow energy to be transferred back to the power supply source, which is necessary for a significant number of applications. The most common solution to this problem is the use of controllable rectifier [1] combined with a phase-shifting control. In this way, the converter becomes bidirectional with preservation of the option for ZVS (Zero Voltage Switching).

It is known that the characteristics of each converter are to a significant extend defined from the used control method.

In [3], a time-domain analysis of bidirectional series resonant DC-DC converter operating above the resonant frequency is presented. As a result, modelling of the converter resonant tank circuit processes is accomplished and expressions for the model coefficients are obtained.

The current paper presents sequel of the theoretical examinations achieved in [3]. Its purpose is load and control characteristics of the bidirectional series resonant DC-DC converter to be obtained with phase-shift control and operation at constant frequency above the resonant one.

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II. PRINCIPLE OF THE CONVERTER OPERATION

Circuit of the examined converter is presented in Fig.1. It consists of two identical bridge inverter stages, resonant tank circuit (L, C), matching transformer Tr, capacitive input and output filters (C_d и C_0). Fig.1 also presents the snubber capacitors $C_1 \div C_8$ by which a zero voltage switching is obtained.

A voltage U_d is applied to the DC terminals of the „input" inverter stage (transistors $Q_1 \div Q_4$ with freewheeling diodes $D_1 \div D_4$), and a voltage U_0 – to those of the „output" stage (transistors $Q_5 \div Q_8$ with freewheeling diodes $D_5 \div D_8$).

The converter operation is discussed in details in [3] with the possible operating modes being defined. The first of them is called **DIRECT MODE**. In this mode, it is assumed that energy is transmitted from the source with voltage U_d to the one with voltage U_0. In the second mode – **REVERCE MODE**, energy flows in reverse direction – from U_0 to U_d.

The presented in Fig. 2 waveforms illustrate the converter operation in **DIRECT MODE**, and those in Fig. 3 – in **REVERCE MODE**.

The „input" stage generates the voltage u_{ab}, which has square-wave form and amplitude U_d. Because of the fact that the converter operates at constant frequency ω_S, which is higher than the resonant ω_0, the current i_L falls behind the voltage u_{ab} at an angle φ. The „output" stage generates the
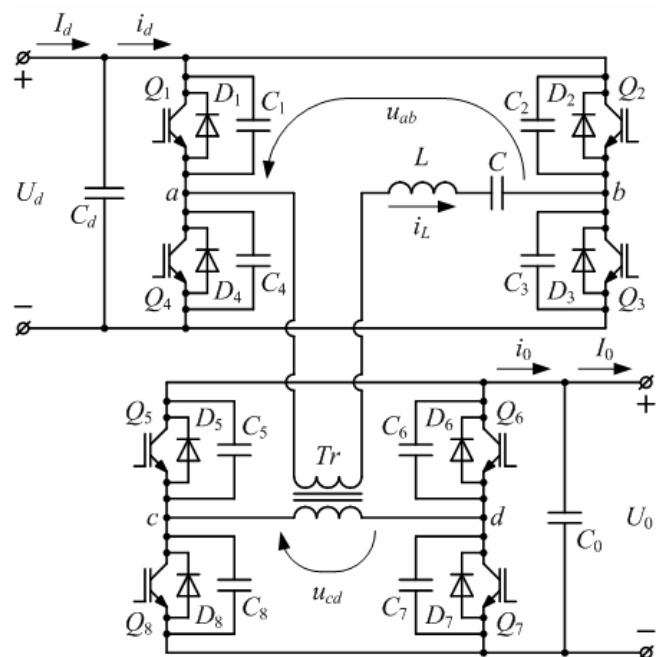

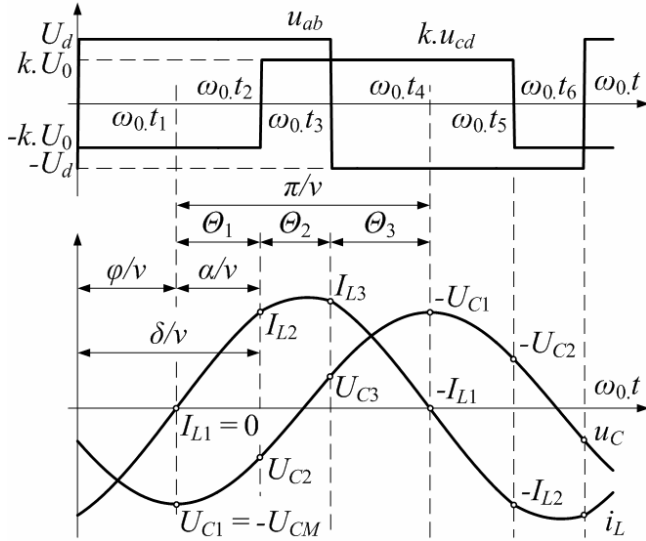Fig. 1. Circuit of the Bidirectional Resonant DC/DC Converter

Fig. 2. Waveforms at **DIRECT MODE**

Fig. 3. Waveforms at **REVERCE MODE**

voltage u_{cd}, which also has square-wave form and amplitude U_0. This voltage is shifted from u_{ab} at an angle δ. When δ < π, **DIRECT MODE** is observed, and when δ > π – **REVERCE MODE** is observed. In this way, the output power control is achieved by the variation of angle δ.

Angle φ corresponds to the conduction time of the „input" stage freewheeling diodes, and angle α – to the conduction time of the „output" stage transistors.

Angles φ, α and δ are related to the operating frequency $ω_S$.

III. MODELING OF THE CONVERTER OPERATION

For the purposes of the analysis, the following assumptions are made: all the circuit elements are ideal, the transformer *Tr* has a transformation ratio *k*, the commutations are instantaneous, and the ripples of the voltages U_d and U_0 are negligible.

The waveforms (Figs. 2 and 3) show that any of the half cycles can be divided into three intervals. For each of them, an equivalent DC voltage U_{EQ} is applied to the resonant tank circuit.

In accordance with the assumptions made, the resonant frequency, the characteristic impedance and the frequency detuning are:

$$\omega_0 = 1/\sqrt{LC} \; ; \quad \rho_0 = \sqrt{L/C}; \quad \nu = \omega_S / \omega_0 \qquad (1)$$

In order to obtain generalized results, all the quantities are normalized as follows: the voltages according to U_d; and the currents – according to U_d/ρ_0. For each of the mentioned intervals, the normalized values of the current i_L through the inductor *L* and the voltage u_C across the capacitor *C* are determined as follows:

$$i'_{Lj}(\theta) = I'_{Lj}\cos\theta - \left(U'_{Cj} - U'_{EQj}\right)\sin\theta$$
$$u'_{Cj}(\theta) = I'_{Lj}\sin\theta + \left(U'_{Cj} - U'_{EQj}\right)\cos\theta + U'_{EQj} \qquad (2)$$
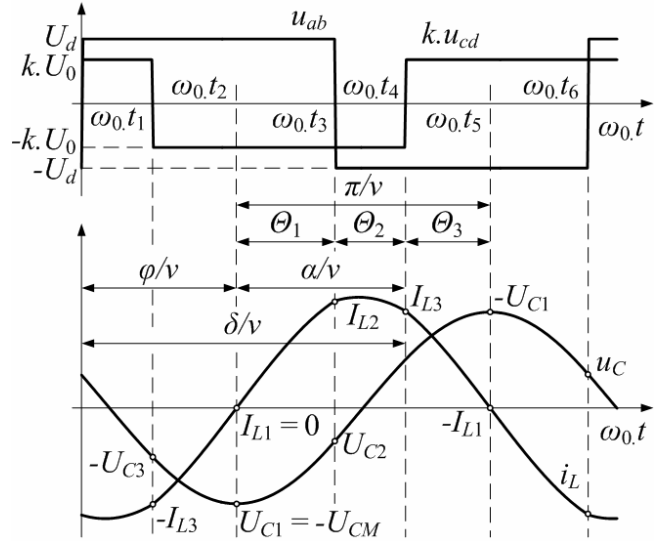
where *j* is the interval number; I'_{Lj} and U'_{Cj} are normalized values of the inductor current and the capacitor voltage at the beginning of the interval; $\theta = 0 \div \Theta_j$; Θ_j – angle of the interval for the resonant frequency ω_0; U'_{EQj} – normalized value of the voltage applied to the resonant tank circuit during the interval.

From Figs. 2 and 3, it is observed that the value of i'_L at the end of given interval appears to be initial value for the following one. The same applies to the voltage u'_C. Therefore:

$$I'_{Lj+1} = I'_{Lj}\cos\Theta_j - \left(U'_{Cj} - U'_{EQj}\right)\sin\Theta_j$$
$$U'_{Cj+1} = I'_{Lj}\sin\Theta_j + \left(U'_{Cj} - U'_{EQj}\right)\cos\Theta_j + U'_{EQj} \qquad (3)$$

It is convenient the interval at which the initial values are $I'_{L1} = 0$ and $U'_{C1} = -U'_{CM}$ to be chosen as first. Then, for the second and the third intervals, the initial values of the current (I'_{L2} and I'_{L3}) and the voltage (U'_{C2} and U'_{C3}) are calculated on the base of Eqs. (3). For one half cycle the necessary for the purpose parameters Θ_j and U'_{EQj} are pointed out in Table I.

TABLE I

MODE	Parameter	Number of interval		
		1	2	3
DIRECT	Θ_j	$\dfrac{\delta - \varphi}{\nu}$	$\dfrac{\pi - \delta}{\nu}$	$\dfrac{\varphi}{\nu}$
	U'_{EQj}	$1+kU'_0$	$1-kU'_0$	$-1-kU'_0$
REVERCE	Θ_j	$\dfrac{\pi - \varphi}{\nu}$	$\dfrac{\delta - \pi}{\nu}$	$\dfrac{\pi - \delta + \varphi}{\nu}$
	U'_{EQj}	$1+kU'_0$	$-1+kU'_0$	$-1-kU'_0$

In [3], analytical expressions for determination of the normalized values of the voltages U'_0 and U'_{CM} are obtained. Like the initial values of the current i'_L and the voltage u'_C, they also represent function of the control parameter δ and the angle φ:

$$U'_0 = \frac{1}{k} \frac{\sin\left(\dfrac{\pi - \varphi}{\nu}\right) - \sin\left(\dfrac{\varphi}{\nu}\right)}{\sin\left(\dfrac{\pi - \delta + \varphi}{\nu}\right) - \sin\left(\dfrac{\delta - \varphi}{\nu}\right)} \qquad (4)$$

$$U'_{CM} = 2\frac{\sin\left(\dfrac{\varphi}{\nu}\right) + U'_0 \sin\left(\dfrac{\pi - \delta + \varphi}{\nu}\right)}{\sin\left(\dfrac{\pi}{\nu}\right)} - \left(1 + kU'_0\right) \qquad (5)$$

IV. LOAD AND CONTROL CHARACTERISTICS

For determination of the converter capabilities and for the purposes of its design, it is necessary the average values of the currents through the particular elements to be determined. For convenience, the following substitution is used:

$$I'_{AV\,j} = \frac{\nu}{2\pi} \int_0^{\Theta_j} i'_{L\,j}(\theta)d\theta$$

$$= \frac{\nu}{2\pi}\left[I'_{L\,j}\sin\Theta_j - \left(U'_{C\,j} - U'_{EQ\,j}\right)\left(1 - \cos\Theta_j\right)\right] \qquad (6)$$

The converter power devices conduct only within a single half cycle. The normalized average values of the currents through them for the **_DIRECT MODE_** are determined by expressions (7a) and (8a), and for the **_REVERCE MODE_** – by expressions (7b) and (8b):

$$I'_{QI} = I'_{AV1} + I'_{AV2}; \quad I'_{DI} = I'_{AV3} \qquad (7a)$$

$$I'_{QI} = I'_{AV1}; \quad I'_{DI} = I'_{AV2} + I'_{AV3} \qquad (7b)$$

$$I'_{QR} = kI'_{AV1}; \quad I'_{DR} = k\left(I'_{AV2} + I'_{AV3}\right) \qquad (8a)$$

$$I'_{QR} = k\left(I'_{AV1} + I'_{AV2}\right); \quad I'_{DR} = kI'_{AV3} \qquad (8b)$$

where I'_{QI} and I'_{DI} are the normalized average values of the currents through the transistors and the freewheeling diodes of the „input" stage; I'_{QR} and I'_{DR} – through the transistors and the freewheeling diodes of the „output" stage.

Independently from the operating mode, the normalized average values of the „input" current I'_d and the „output" current I'_0 are determined as follows:

$$I'_d = I'_{QI} - I'_{DI} \qquad (9)$$

$$I'_0 = I'_{DR} - I'_{QR} \qquad (10)$$

By means of expressions (3) ÷ (10), for a fixed value of the control parameter δ and with variation of the angle φ, values for the important converter quantities U'_0, I'_{QI}, I'_{DI}, I'_{QR}, I'_{DR} and I'_0 can be calculated. On the base of these values, different load characteristics of the converter are easily built. For the purposes of the analytical examination, such characteristics
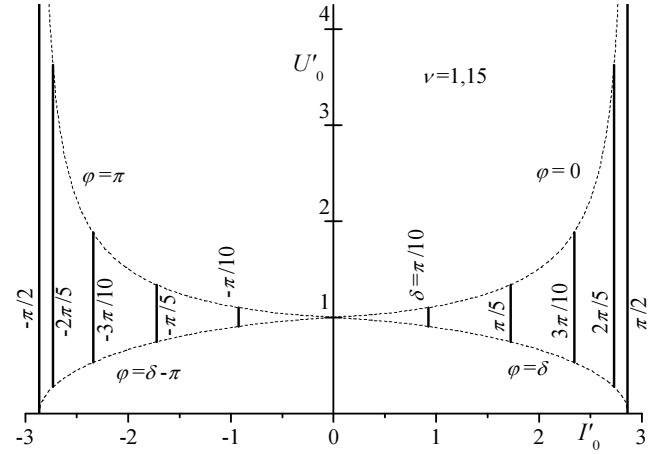

Fig. 4. Normalized output characteristics at $-\pi/2 \leq \delta \leq +\pi/2$

are obtained at frequency detuning ν=1,15 and transformation ratio k=1.

Fig. 4 presents the normalized output characteristics of the converter for values of the control parameter in the range $-\pi/2 \leq \delta \leq +\pi/2$. The dependencies of the output voltage U'_0 from the output current I'_0 are shown with thick lines. With dotted lines are presented boundary curves determining the converter operating area at ZVS. It is observed that this area is strongly restricted. Even the no-load mode ($I_0 = 0$) is possible only with $kU_0 = U_d$. Apparently, this range of variation of the control parameter δ is not recommended for operation of the converter.

Fig. 5 presents the normalized output characteristics of the converter for values of the control parameter in the range $\pi/2 \leq \delta \leq 3\pi/2$. In this case, limitations for the converter operation at ZVS are not observed.

The output characteristics (Figs. 4 and 5) show that, independently from the range of variation of the control parameter, the output voltage does not depend on the output current, i.e. the examined converter behaves as an ideal current source. Moreover, the output voltage does not change its polarity and, independently from the energy transfer direction, can significantly exceed the input one.
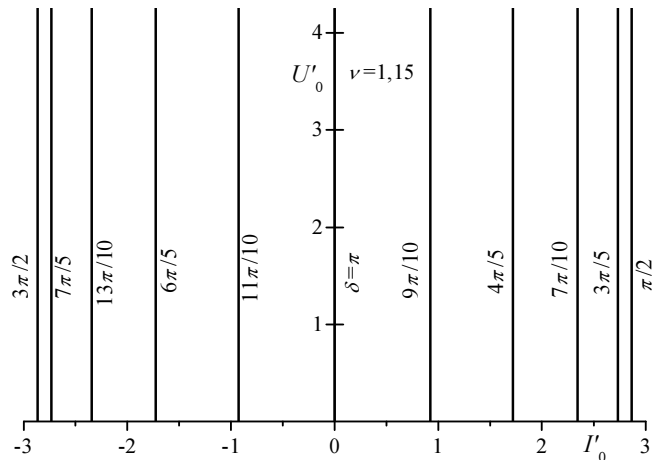

Fig. 5. Normalized output characteristics at $\pi/2 \leq \delta \leq 3\pi/2$
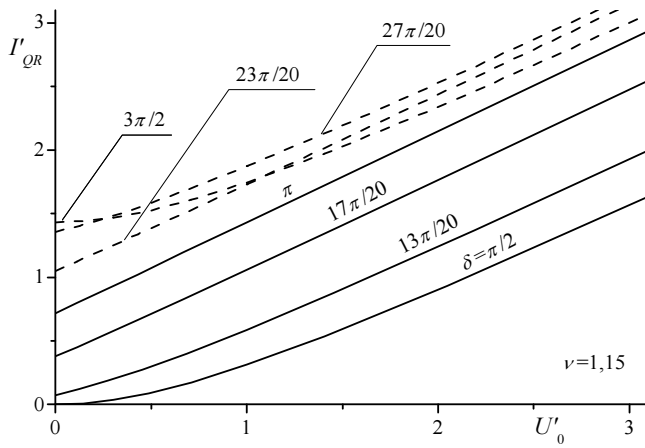
Fig. 6. Normalized average current through the „output" stage transistors – I'_{QR}

Fig. 8. Normalized control characteristics of the converter

Fig.6 presents the normalized dependencies of the average value of the current I'_{QR} through the „output" inverter stage transistors from the output voltage U'_0. Similar dependencies of the average value of the current I'_{DR} through the „output" inverter stage freewheeling diodes are shown in Fig. 7. The characteristics corresponding to the **DIRECT MODE** are presented with thick lines, and those to the **REVERCE MODE** – with dotted lines. They are obtained for variation of the control parameter in the range $\pi/2 \leq \delta \leq 3\pi/2$. For both modes, monotonous rise of the currents I'_{QR} and I'_{DR} is observed with the increase of U'_0. This shows that, independently from the energy transfer direction, the converter power devices stress is bigger for greater values of the output voltage.

Fig. 8 presents normalized control characteristics of the examined converter for several values of the frequency detuning ($v = 1,08; 1,10; 1,15; 1,20; 1,30$). According to the fact that the output voltage does not depend on the output current, they are easily obtained with the substitution $\varphi = \delta/2$ ($U'_0 = 0$). In the range $\pi/2 \leq \delta \leq 3\pi/2$, the dependencies variate monotonously, and a significant linear section can be observed.
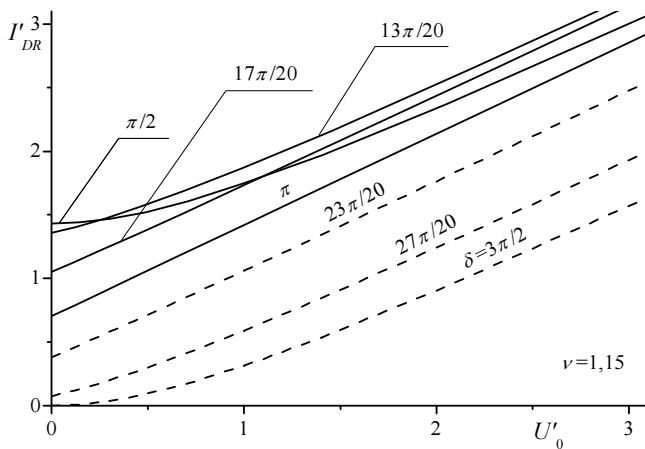

Fig. 7. Normalized average current through the „output" stage freewheeling diodes – I'_{DR}
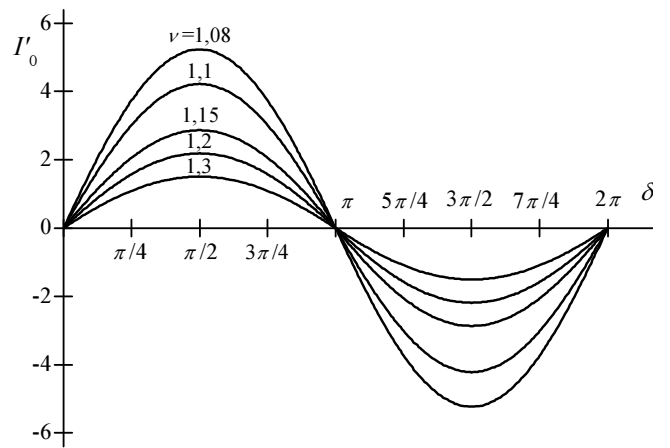
V. CONCLUSION

A bidirectional series resonant DC-DC converter operating above the resonant frequency is examined. A phase-shift control technique is used. As a consequence, its normalized load and control characteristics are built.

On the base of the obtained results, the following can be concluded:

• The considered bidirectional series resonant DC-DC converter can operate without violation of the ZVS conditions in wide range of variation of the control parameter. Furthermore, a significant linear section of the control characteristic is observed.

• With the chosen control technique, the converter behaves as a current source. Its output voltage can exceed the input one independently from the energy transfer direction.

• The converter power devices stress grows up with the output voltage increase.

The obtained results can be used for further examination and design of such converters.

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Two-Phase Switching-Mode Converter with Zero Voltage Switching Designed on CMOS 0.35 μm Technology

Tihomir Brusev[1], Georgi Kunov[2] and Elissaveta Gadjeva[3]

Abstract –**A two-phase switching-mode dc-dc converter with Zero Voltage Switching (ZVS) is presented in this paper designed on CMOS 0.35 μm technology with Cadence. The losses in the main power transistors are evaluated. The investigation results show that when ZVS technique is used, the efficiency of the whole system could be increased by about 3% compared to the standard two-phase dc-dc converter architecture.**

Keywords – **Two-phase switching-mode converter, Zero Voltage Switching (ZVS), Efficiency, CMOS technology, Cadence.**

I. INTRODUCTION

Today smart phones can transfer large data packages in a real time, thanks to the fourth generation Long-Term Evolution (4G LTE) wireless communication standard. The great functionality of modern telecommunication devices is due to the use of OFDM (Orthogonal Frequency-Division Multiplexing) modulation. The signal is transferred by several sub-carrier frequencies, which are summed at the output of modulator. Thus the spectrum in 4G LTE standard is used much more effectively [1].

On the other hand the sizes of the new mobile phones became larger, which allows increasing of the battery dimensions. Nevertheless, the time between two consecutive charges is small. The efforts of the designers are focused over the increasing of power supplies efficiency. Those circuits have to ensure the desire energy of transmitter's power amplifier (PA). The standard switching-mode dc-dc converter cannot fulfill the requirements to deliver appropriate fast dynamically changeable output voltage to drain or collector, respectively of MOS or BJT RF transistor of PA.

The power supply circuit, which provides the desire energy to transmitter's PA is called envelope amplifier. The block diagram of envelope tracking power amplifier's system is shown in Fig. 1. Envelope amplifier delivers the drain or collector supply voltage of PA's transistors [2]. It dynamically changes this supply voltage according to the variations of the PA input signal**.** The envelope amplifier tracks the PA input signal and controls the PA supply voltage according to the

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envelope of this signal. The efficiency $\eta_{ET\,PA}$ of the envelope tracking power amplifier's system is equal to [3]:

$$\eta_{ET\,PA} = \eta_{EA}.\eta_{PA}, \qquad (1)$$

where η_{EA} is the efficiency of the envelope amplifier; η_{PA} is respectively the efficiency of the PA. The run-time of wireless communication devices could be increased if envelope amplifier with high efficiency is designed.
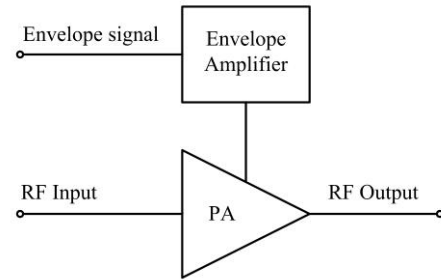

Fig. 1. Envelope tracking power amplifier's system

Most of the envelope amplifier's architectures include parallel or series connected linear amplifier and switching-mode dc-dc converter. Switching-mode converter ensures between 70% and 80% energy delivered to PA [2]. Therefore, high efficient dc-dc converter could improve significantly the efficiency of envelope amplifier. One of the features of switching-mode converters is that they are good choice only when relatively low-data rate communication signal is transferred. The tracking speed of the switching-mode converter could be increased if the single phase dc-dc converter is replaced by two-phase converter. Thus the portion of energy distributed from low efficient linear amplifier in envelope amplifier will be smaller, compared to the case when the switching-mode amplifier is a single phase dc-dc converter. This leads to improving of the overall efficiency of envelope tracking power amplifier system.

The tracking speed possibilities of standard synchronous single phase dc-dc converter and two-phase interleaved buck converter are discussed in Section II *A* of this paper. In Section II *B*, the Zero Voltage Switching (ZVS) technique is considered, which helps to reduce power losses in the main transistor of switching-mode dc-dc converters. Two-phase dc-dc converter with ZVS is designed with Cadence on CMOS 0.35 μm process. Power losses in the main power MOS transistors are considered and evaluated. The efficiency results of two-phase dc-dc converter with ZVS are evaluated and compared to the efficiencies of the standard two-phase interleaved dc-dc converter. The received results are presented in Section III.

II. SWITCHING-MODE CONVERTERS

A. Single phase and two-phase switching-mode converters

The standard synchronous single phase dc-dc converters, shown in Fig. 2, indicate high power losses in the inductor at large values of the inductor current ripple Δi_L. The two-phase converter structure helps to reduce this negative effect [4].
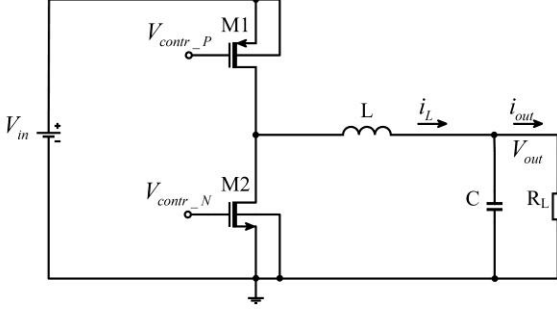

Fig. 2. Single phase dc-dc converter

The two-phase interleaved dc-dc converter architecture, presented in Fig. 3, leads to reduction of the output current ripple Δi_{out} of the circuit. The reason is that the phase sifted inductor current ripples respectively of the first and second sub-converter stage Δi_{L1} and Δi_{L2} are summed at the output.
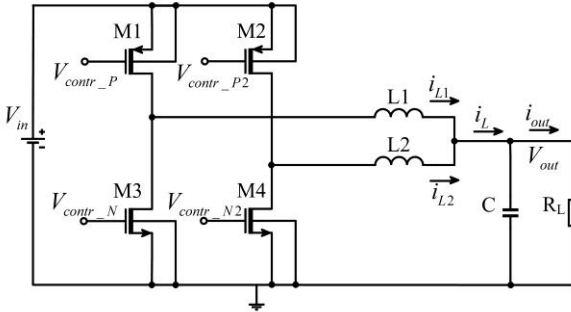

Fig. 3. Two-phase interleaved dc-dc converter

The output current ripple Δi_{out} of the two-phase interleaved buck converter with non-coupled inductors can be expressed in the form [5]:

$$\Delta i_{out} = \frac{V_{out}}{L}(1-2D)T_s, \qquad (2)$$

where T_s is the switching period of converter, L is the value of filter inductors (if $L1=L2$, which is the case of the investigated dc-dc converter architecture).

Minimum values of the output current ripple Δi_{out} can be received if the duty cycle of the converter D is close to 0.5. The inductor current ripples Δi_L of the single phase buck dc-dc converter and two-phase interleaved buck converter with non-coupled inductors have equal values, and can be expressed in the form [5]:

$$\Delta i_L = \frac{V_{out}}{L}(1-D)T_s. \qquad (3)$$

In two-phase interleaved dc-dc converters architectures the same output current ripples as those of single-phase dc-dc converters could be established with smaller values of output filter inductors respectively $L1=L2$. These phenomena could be very useful for LTE applications power supply circuit, when envelope amplifier has to be fast in order to track high frequency envelope signal. The two-phase dc-dc converter could replace the single phase switching-mode regulator in parallel hybrid envelope amplifier structure. Thus most of the energy delivered to power amplifier can be ensured from fast and high efficient switching-mode multiphase dc-dc converter. The portion distributed from low efficient linear amplifier will be smaller, compared to the case when switching-mode amplifier is a single phase dc-dc converter, improving the overall efficiency of envelope tracking power amplifier system.

B. Zero Voltage Switching

The circuit of synchronous single phase switching-mode buck dc-dc converter with ZVS is shown in Fig. 4. The advantage of those types of circuits is that the main power transistor *M1* can be switched-on and switched-off respectively at zero voltage [6].
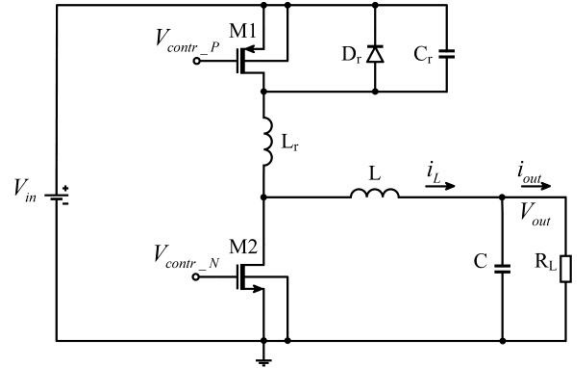

Fig. 4. Single phase dc-dc converter with ZVS

The zero voltage switch-off of the main PMOS transistor *M1* of dc-dc converter is because of the capacitor C_r. The Zero voltage switching-on state of the PMOS transistor *M1* is ensured by the diode D_r. The function of this component is to clamp to zero capacitor voltage V_c, when transistor *M1* is at switch-off state [6].

The effect of ZVS will lead to zero switching power losses of main PMOS transistor *M1*. Thus the total power losses in the MOS transistors of synchronous dc-dc converter could be decreased. They are equal to [7]:

$$P_{tot,MOS} = a\sqrt{\left(I^2 + \frac{\Delta i_L^2}{3}\right)f_s}, \qquad (4)$$

where Δi_L is the inductor current ripple, I is a dc current

supplied to the load, and a is a coefficient depending on the equivalent series resistance of the transistors, the input total capacitance of the MOS transistors C_{tot}, and the power supply V_{in}. The decreasing of total power losses in MOS transistors of dc-dc converter will improve the efficiency of the circuit. The efficiency of the buck dc-dc converter can be expressed by:

$$\eta = \frac{P_{out}}{P_{out} + P_{losses}}, \qquad (5)$$

where P_{out} is the output power of the dc-dc converter; P_{losses} are overall power losses in the dc-dc converter.

III. INVESTIGATION OF TWO-PHASE SWITCHING-MODE CONVERTER WITH ZVS

The two-phase switching-mode converter with ZVS is designed with Cadence on AMS CMOS 0.35 μm 4-metal technology. The block circuit of whole buck dc-dc converter system is presented in Fig. 5. It consists of two power buck stages, error amplifier, ramp generator, comparator and buffer stage. In the designed two-phase switching-mode converter, Pulse-Width Modulation (PWM) control technique is used.
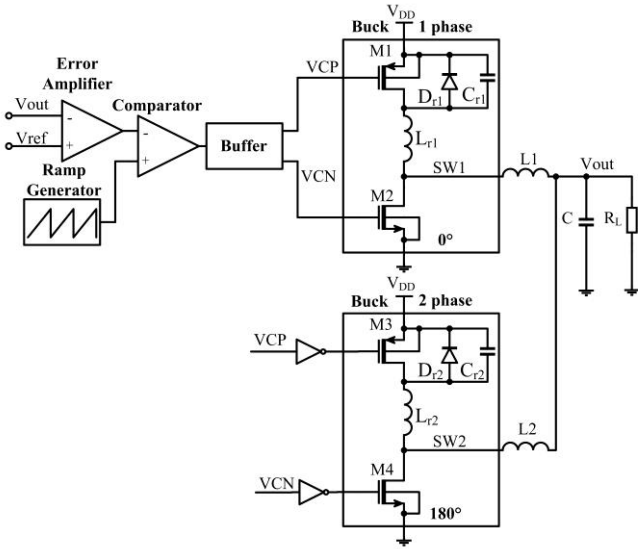

Fig. 5. Two-phase switching-mode converter with ZVS

The control signals, which regulate the main power MOS transistors of the both power buck stages, are 180° phase shifted. The supply voltage V_{DD} is equal to 3.6 V, which is a standard output voltage of lithium-ion battery. The average value of the output voltage $V_{out(av)}$ of the converter is regulated to be equal to 1.2 V. The output filter inductors $L1$ and $L2$ of the both power buck stages are equal to 125 nH. The filter capacitor C is equal to 400 pF. The switching frequency f_s of the two-phase dc-dc converter with ZVS is equal to 76 MHz. The PMOS transistors $M1$ and $M3$ in both buck power stages are represented by 6 equal "modprf" transistors connected in parallel. Their sizes (W/L) are respectively 150/0.35 [μm]. For NMOS transistors $M2$ and $M4$, which replace the diode in the standard buck dc-dc converter circuit, 4 equal connected

in parallel "modnrf" transistors are used. Their sizes (W/L) are respectively 200/0.35 [μm]. The values of resonant inductors L_{r1} and L_{r2} are equal to 10 nH. The values of resonant inductors C_{r1} and C_{r2} are equal to 50 pF. The waveform of output voltage V_{out} of the two-phase switching-mode converter with ZVS is shown in Fig. 6.
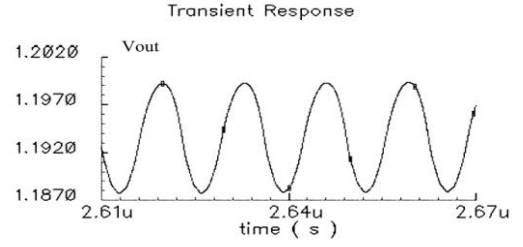

Fig. 6. The waveform of output voltage V_{out} of the two-phase switching-mode converter with ZVS

The waveforms respectively of I_{L1} and I_{L2} of two-phase switching-mode converter with ZVS are presented in Fig. 7.
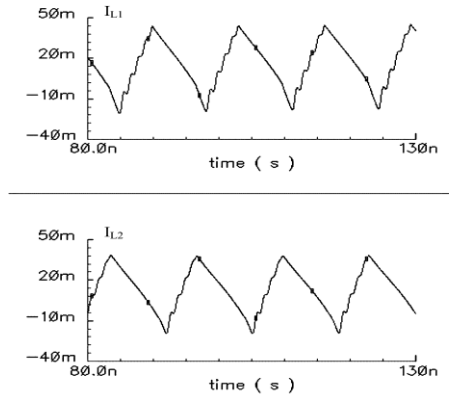

Fig. 7. Waveforms of the inductor currents I_{L1} and I_{L2} of two-phase switching-mode converter with ZVS

The waveforms of control signal VCP, which regulate the mode of operation of main PMOS transistors of the first buck stage, and the capacitor's voltage V_{Cr} are shown in Fig.8.
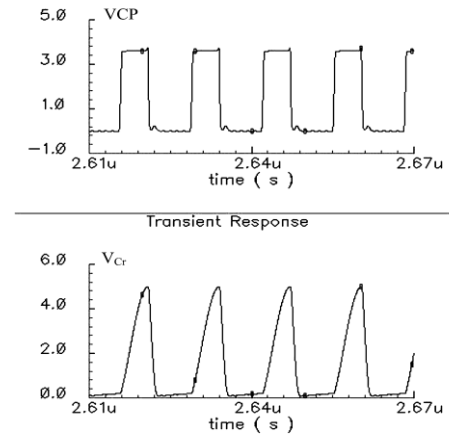

Fig. 8. The waveforms of control signal VCP and the capacitor's voltage V_{Cr}

The total power losses in main PMOS transistors (P$_{PMOS}$) of two-phase dc-dc converter, designed on CMOS 0.35 μm technology, are investigated as a function of the load R_L. The investigations are performed when the circuit works with and without ZVS. The efficiencies of two-phase switching-mode converter, respectively with and without ZVS are evaluated. The received results are presented in Table I.

TABLE I
POWER LOSSES IN MAIN PMOS TRANSISTORS AND EFFICIENCY OF TWO-PHASE DC-DC CONVERTER AS A FUNCTION OF LOAD R_L, RESPECTIVELY WITH AND WITHOUT ZVS

	R_L=10 [Ω]	R_L=20 [Ω]	R_L=25 [Ω]	R_L=30 [Ω]
P$_{PMOS}$ [mW]	21.4	13.8	11.8	8.7
P$_{PMOS}$−ZVS [mW]	19.4	11.4	9.6	6.3
Efficiency [%]	67.89	71.25	74.2	76.84
Efficiency−ZVS [%]	69.14	73.43	76.14	78.26

All the results shown in Table I are received when average value of the output voltage $V_{out(av)}$ of converter is equal to 1.2 V.
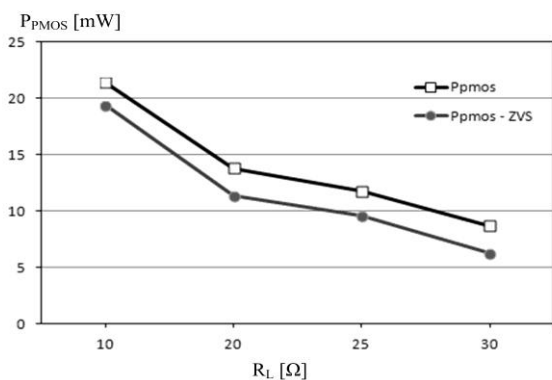

Fig. 9. Power losses P_{PMOS} of two-phase dc-dc converter as a function of load R_L with and without ZVS

The power losses of PMOS transistors of two-phase dc-dc converter are presented graphically in Fig. 9 as a function of the load R_L with and without ZVS.
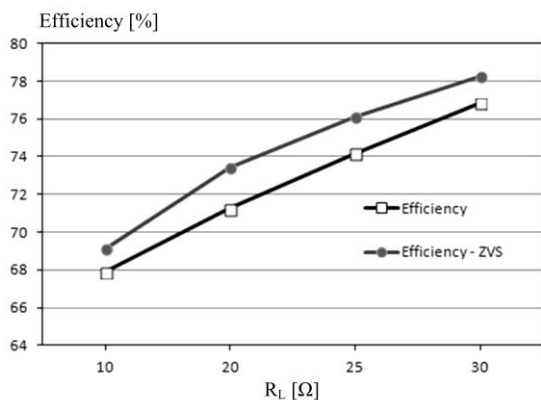

Fig. 10. Efficiency of two-phase dc-dc converter as a function of load R_L, respectively with and without ZVS

As it can be seen from the picture shown in Fig. 9, the total power losses in the main transistors of two-phase switching-mode (*M1* and *M3*) are decreased by about 11% when ZVS technique is used. The reason is that switching power losses are minimized. This effect can be seen in Fig. 10, where the efficiency results of two-phase dc-dc converter as a function of the load R_L are graphically presented. As it can be seen from the picture efficiency of the whole converter system is increased by about 3% when ZVS is used. The values of the load resistance R_L are changed between 10 Ω and 30 Ω, because this range represents the practical equivalent value of PA used as a load [8].

IV. CONCLUSION

In this paper two-phase buck dc-dc converter with ZVS designed on CMOS 0.35 μm technology has been proposed. This circuit could be used as switching-mode regulator in parallel hybrid envelope amplifier for LTE applications. The investigation result shows that efficiency of two-phase dc-dc converter can be increased by about 3% if ZVS technique is used. The reason is that the total losses in the main switch of the converter's power stage are minimized.

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Converters with Energy Dosing for Charging of EV's Li-ion Batteries

Nikolay Madzharov [1], Goran Goranov [2]

Abstract - **The scientific and the applied problems treated in the present paper are related to the development of a DC/DC power supplies with energy dosing for charging of electrical vehicles (EVs) batteries. They are a hybrid between the achievements in modern microelectronic components - frequency capabilities and low commutational losses, and the trends in the development of power conversion circuits which maintain the power or/and current constant and independent from the battery state operating of charge (SOC).**

Some converters are presented together with their modifications. Theirs operation principle has been pointed out, as well as the investigations that have been carried out. Conclusions have been drawn about the possibility of obtaining good charging characteristics when the battery parameters change during the different charging scenarios.

Keywords – **Converter, Energy dosing, Battery, Electrical vehicles, Battery state operating of charge.**

I. INTRODUCTION

The power electronic topologies for high power battery chargers can be largely classified into two categories: single phase types and two phase types [1,3,9,12]. Single phase battery chargers generally combine the power factor correction stage and the DC-DC conversion stage into one. They can be more efficient than the two phase types. However, single phase type battery chargers have a low frequency ripple in the output voltage and as a result, the switch and transformer ratings become larger [1,7,12]. The two phase types generally use a boost type converter to improve the power factor at the first stage and a DC/DC converter for the control of the voltage, current and power at the second stage. Two phase power converters use their own controllers to control the input current and the output voltage, respectively power, at the same time. They have a higher power factor and a lower harmonic distortion i.e., they have an advantage that there is almost no low frequency ripple in the output.

The other main characteristic of the charging power supplies is their universality regarding the battery parameters and good regulating possibilities. Not with standing the progress made, the methods used to regulate the output voltage of power sources, are not sufficiently smooth and envisage the use of relatively complex matching transformers, capacitors and ect.

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With a view of solving the problems in this area, DC, converters with energy dosing (ED) have been synthesized analysed and tested [1,2,9,12]. According to ED method of operation, they generate, with a specified power, an output voltage corresponding to the particular parameters of the battery [1-3].

The main purpose of the present paper is also in this direction - presentation of circuits of power supply with ED for battery charging and the preliminary investigation performed on them.

A 32 kW battery charger is implemented to demonstrate the stability and performance of the system with ED. The validity of the concept is then verified through the constant current (CC) mode and the constant power (CP) mode charge of an actual Li-ion battery.

II. DC CONVERTERS WITH ENERGY DOSING DEVELOPED FOR EV CHARGERS

The EV battery, such as electrical load, is characterized with strongly variable parameters during changing process - from idle running to short circuit. In table 1 are presented parameters of tested EV battery (Fig.1a) that contains more than a hundred pieces of AMP20m1HD-A single battery (Fig.1b), production of A123 Systems [9]. In connection with this, the charging convertor should have specific characteristics – on one hand to be able to limit and support output current and on the other hand to provide the dynamic feeding of the necessary power to the battery.

a)   b)
Fig. 1. Tested EV battery

A great number of circuits of DC/DC converters with ED are known [1,2,4-12]. Their distinctive feature is the presence of a dosing capacitor included in series in the battery loop through the interval of energy consuming by the mains. All of them provide dosing of the energy supplied to the battery, reliable work of loads changing and high commutation stability in the dynamic operating mode.

In table 2 are showed the basic circuit and respective time charts, illustrating the principle of converters with ED operating mode. It can be seen that the dosing capacitor voltage is fixed always to the value of the supplying DC

voltage. Consequently, at constant work frequency the power given in the battery will always be one and the same. For the circuits with combined recharge of the dosing capacitor, in the expression for the power takes part the coefficient **K** which is less than 1 and depend on the load parameters.

TABLE I
PARAMETERS OF EV BATTERY

Energy	18.7kWh (67.32MJ)				
Battery capacity	56.7 Ah				
Output voltage	$310 \div 374$V DC				
Charging current	$60 \div 90$A DC				
Internal resistance	$0.10 \div 0.14\Omega$				
Battery voltage U_{DCbat},V		310	330	350	374
$I_{DCbat} = 60$A		5.17	5.50	5.83	6.23
$I_{DCbat} = 75$A	R_{BAT} [Ω]	4.13	4.40	4.67	4.99
$I_{DCbat} = 90$A		3.44	3.67	3.89	NA

The DC converters with ED have the following advantages [1-4, 6, 7, 11, 12]:

-wide range concerning the load parameters and power;

-good regulation characteristics at satisfactory for the practice range and sensitivity;

-with the enlarging of the regulation depth the conditions for steady and optimum commutation of the transistors are kept, i.e. the switching is ZCS and/or ZVS;

-good electromagnetic compatibility with the mains.

TABLE II
DC/DC CONVERTERS WITH ENERGY DOSING

Circuit	Method of ED	Intervals
1) DC/DC converters with ED and capacitor recharging by load current		
		$0 \div t_1$ T_1 $t_1 \div t_2$ T_2 $t_2 \div \pi$ D **P=E²C_df**
		$0 \div t_1$ T_1, T_3 $t_1 \div t_2$ D $t_2 \div t_3$ T_2, T_4 $t_3 \div \pi$ D **P=E²C_df**
2) DC/DC converters with ED and combined recharge of the dosing capacitor		
		$0 \div t_1$ T_1, T_3, D $t_1 \div t_2$ T_1, T_3 $t_2 \div t_3$ D_1 $t_3 \div t_4$ T_2, T_4, D $t_4 \div t_5$ T_2, T_4 $t_5 \div \pi$ D_1 **P=kE²C_df**
		$0 \div t_1$ T_1, T_6 $t_1 \div t_2$ T_1, T_3, T_6 $t_2 \div t_3$ D, D_1 $t_3 \div t_4$ T_4, T_5 $t_4 \div t_5$ T_2, T_4, T_5 $t_5 \div \pi$ D, D_1 **P=kE²C_df**

Depending on the operating characteristics, the circuits of DC converters with ED can be systematized in the following groups:

-by the way of dosing capacitor recharging - combined or by the battery current;

-by the principle of output voltage regulation;

-by the presence of preparatory capacitor recharging;

-by the amount of the output impulses for one work frequency period – single-cycle and two-cycle circuits.

The comparative analysis of the results from the examinations and the obtained characteristics [2-4] give the possibility that the following recommendations for the usage of the shown in table 2 circuits can be formulated:

-at the lack of requirements to the battery current pulsations it is expedient to be used the circuits from group 1.

-at the necessity of supporting small output current pulsations, at a wide regulation range are used the circuits with combined recharging of the dosing capacitor. Theoretically, they do not have limits in the regulation characteristics;

-a DC/DC converter, combining ED and transforming, take a medial place in comparison to the examined circuits. To keep the small output current pulsations at a range of regulation K>3 it is necessary a great increasing of the commutation inductance value.

The dosing source in the shown DC/DC converters with ED is a capacitor, because of its great energy reserve and easy realization. It is also possible the use of inductance or inductance-capacitive circuit, tuned to the working frequency.

II.I. NON SYMMETRICAL DC/DC CONVERTER WITH ENERGY DOSING

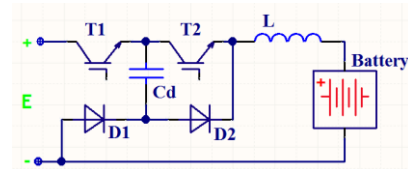Figure 2 presents a non symmetrical DC/DC converter with ED.

Fig.2. Non symmetrical DC/DC converter with ED

Control pulses are passed from the control system to T_1, T_2. In case of a battery load the circuit operating principle is as follows. When transistor T_1 is forward - biased, current flows along the circuit $(+)E,T_1,Cd,D_1,L,battery,(-),E$. When the dosing capacitor is charged up to voltage equal to E, the diode D_2 is forward - biased and the current is closed along the circuit D_2, D_1, L, battery.

By the forward-biasing of T_2 the capacitor Cd, charged up to the supply voltage E, begins discharging through T_2, L, battery, D_1, Cd. When the dosing capacitor is discharged the energy stored in the load is closed along circuit D_2, D_1, L, battery.

The expression

$$W = Cd.E^2 / 2 \, , \qquad (1)$$

is valid for the energy which is stored and given up by means of the dosing capacitor. Taking into consideration the fact that the amplitude of the capacitor charge Cd for one half-period is equal to the supply voltage Ucd=E, the power given up in the load can be determined

$$P = Cd.f.E^2 , \qquad (2)$$

where Cd is the capacitance of the dosing capacitor, f - the operating frequency of the dosing device (T_1, T_2, Cd), E - the supply voltage.

II.II. SYMMETRICAL DC/DC CONVERTER WITH ENERGY DOSING

Figure 3 presents a symmetrical DC/DC converter with ED having a decoupled dosing capacitor.
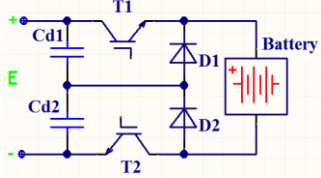

Fig. 3. Symmetrical DC/DC converter with energy dosing

The control pulses are passed from the control system to transistors T_1 and T_2. In the first half-period T_1 is forward - biased, and current flows along the circuit T_1, battery, D_2, Cd_1, the capacitor Cd_1 gets discharged and Cd_2 charged to voltages 0 and E, respectively. The total sum of the dosing capacitors Cd_1 and Cd_2 voltages is always equal to the voltage of the supply source E. When the dosing diode D_1 gets forward - biased the energy consumption from the supply source stops. The current flows along circuit D_1, battery, D_2. After T_2 gets forward-biased the current flows along Cd_2, D_1, battery, T_2 and Cd_2 gets discharged and Cd_1 charged. After that the dosing diode gets forward-biased, and the current flows along circuit D_1 - battery - D_2.

The output power in the load is determined from the expression

$$P = (C_{d_1} + C_{d_2}).f.E^2 , \qquad (3)$$

where Cd_1 and Cd_2 - capacitance of the dosing capacitors, f - operating frequency of the dosing device, E - supply voltage.

The first conclusion that can be drawn from the expressions for W and P is that when the working frequency, the input voltage and the dosing capacitors value are unchanged, the power transmitted to the battery is constant and does not depend on the battery parameters. Supporting constant power means that the output convertor voltage is matched with the battery voltage.

The second special feature of the converter is obtained by replacement the battery current expression $I_{out} = U_{out}/Z_L$ in (2) and (3). After some transformations it is obtained a correlation giving the connection between the output and the input voltage.

$$U_{out} = 2E \sqrt{\frac{C_d.Z_L}{2.T}} \qquad (4)$$

The conclusion which can be drawn is that by changing the work frequency the output converter voltage, respectively battery voltage can be supported constantly when the battery parameters and/or the input voltage are changed. In figure 4 it is shown the dependence of the output voltage in function from the frequency at different loads (battery parameters). The information from these characteristics is used for converter designing, as it gives an account of the connection between the load value and the capacitor Cd value, giving the power on one hand, and the dependence of the output voltage on the frequency and the input voltage, on the other hand.
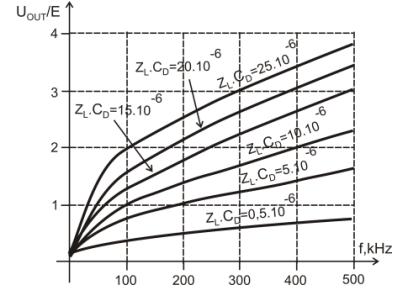

Fig 4. Regulation characteristics

The supporting and the regulation of the output voltage are realized by a feedback which changes the converter working frequency. The analytic dependence of the regulation law can be obtained as the expression for the output power is differentiated in relation to the time t. After some transformations

$$U_{out} I_{out} = 4 C_d E^2 f , \qquad (5)$$

$$U_{out} \, di_{out} + I_{out} \, du_{out} = 4 C_d E^2 \, df \qquad (6)$$

using the expressions

$$du_{out} = di_{out}(Z_L // 1/\omega \, C_F) \qquad (7)$$

and

$$I_{out} = U_{out}/Z_L , \qquad (8)$$

is obtained

$$\frac{du_{out}}{df} = 2E \sqrt{\frac{C_d Z_L}{2f}} \frac{1}{1 + \omega C_F Z_L/2} . \qquad (9)$$

This expression is the operating function of the control system and gives the law, by which it should be modified the frequency of changing the load parameters with a purpose of supporting of constant output voltage. Using this function the control system can foresee, define, compensate and obtain the needed converter output characteristics.

III. EXPERIMENTAL INVESTIGATIONS

The experimental research has been performed using non symmetrical and symmetrical DC converters with ED from figures 2 and 3, having power P=32 kW and frequency f=20 kHz. In fact they belong to the group of converters with ED and capacitor recharging by load current and have all characteristics, defined in paragraph II.

Figures 5 and 6 are presented both studied modes of battery charge at two values of the charging power, respectively current, till the charge level SOC = 90%, when the process ends. The initial points in two characteristics starts from SOC=10% and SOC = 50% level of charge.

At the beginning of the process of charge (0-500 sec) the DC converter with ED maintain constant power and gradually increase in the current value from $0.8 \times I_{DC}$ to reach I_{DC}, 500sec after the beginning of the process. The battery voltage could be calculated by following relationship:

$$U_{BAT \, f} = U_{BAT_{90\%}} - I_{DC}.R_{BAT} = [(0,9.(374 - 310)) + 310] - I_{DC}.R_{BAT} \qquad (10)$$

where $U_{BAT \, f}$ -is battery voltage after end of charging scenario.

The parameter $U_{BAT \, 90\%}$ is battery voltage at SOC = 90%.

On reaching this value the control system sends a signal to the DC convertor with ED for finish the process of charge.
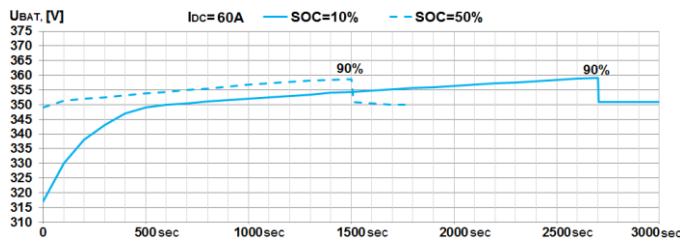

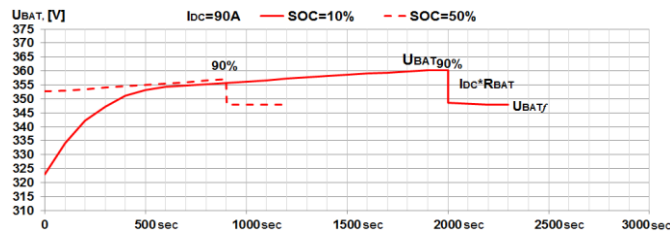Fig.5. Charging scenario at charging power 21 kW (I_{DC} = 60A) and SOC 10 and 50 %.

Fig. 6. Charging scenario at charging power 31 kW (I_{DC} = 90A) and SOC 10 and 50 %

From the tests implemented can be concluded that the charging source works most efficiently while maintaining maximum charging current or/and output power. Depending on the type of battery used, there is a maximum value of SOC, in which the charging process can be carried out – typically SOC = 80 ÷ 90%.

The obtained from the circuit analysis expressions and tests results allow to be drawn charging characteristics at different batteries. They define the area in which the converter with ED can support constant output current or/and power.

IV. CONCLUSION

This paper described the design, control and tests of a DC converter with ED, which can be used to charge the Li-ion battery bank of EVs. A 32 kW converter was designed and implemented to verify the validity of the developed operating mode of ED and control algorithm. The obtained expressions for the control system operating function giving the law for operating frequency changing with a purpose to keep the output power constant when the battery parameters are changed. It has been verified that in ED mode algorithm the charging converter works most efficiently and maintaining maximum charging current or/and output power. It can be concluded that the developed converters with ED may contribute to higher system efficiency and a longer battery life due to its lower ripple current characteristics.

On the basis of the performed analysis and tests the following advantages of the discussed circuits can be pointed out:

a) possibility for operation with almost constant power and/or current and different loads;

b) operation in modes close to idle running and short circuit;

c) transistor commutation with zero current and zero voltage;

d) easy algorithm of transistors operation;

e) high power factor in relation to the mains.

The following disadvantages can be pointed out:

a) high maximum values of the currents through the transistors and the diodes;

b) a large number of active and passive elements for some of the circuits.

The obtained results and the drawn conclusions show that the proposed DC converters with ED can be used as charging power supply sources owing to the possibility of working with a wide range of battery parameters.

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Mathematical model of thermoelectric Peltier module

Liliya Staneva[1], Ivaylo Belovski[1], Anatoliy Alexandrov[2] and Pavlik Rahnev[1]

Abstract – **Thermoelectric Peltier modules (TEM) are devices that convert electrical power in a temperature gradient. Usually in their catalogue data presents some transducer characteristics and maximum parameters, but they are insufficient to create highly efficient thermoelectric systems. The purpose of this article is to offer a relatively easy method for modelling of TEM, and the results are presented in tabular and graphic form by Matlab.**

Keywords – **Thermoelectric elements, Peltier cooler, Modelling**

I. INTRODUCTION

Thermoelectric Peltier modules (TEM) are devices which convert electrical power in temperature gradient. In their work they use the effect of Peltier, consisting of simultaneous heating and cooling of the two opposite sides of TEM [1, 2].

TEM have increasing interest due to simultaneous improving of their economic and technical parameters as well as and widely application which they get.

As a result of this the producer of TEM supplied to the market the wide assortment of modules with different thermoelectrically parameters, shape and sites [3].

Usually in the data sheets for given TEM some converting characteristics and maximum permissible parameters are shown: maximum temperature difference between the sides of the TEM – *ΔTmax,* maximum current – *Imax,* maximum supplying voltage – *Umax,* and maximum absorbed from the cool side of TEM power - Qc_{max} [4,5]

For creating of one high effective thermoelectrically system (TES), except these data it is necessary the optimal parameters of the real module to be known, as well as the base thermoelectrically parameters of the used for modules materials – coefficient of Zeebek *α [V/K]*, specific resistance of the materials –*ρ [Ω.cm]* and the coefficient of thermal conductivity *k [W/cm.K]*.

Unfortunately the producer does not show that information in the data sheets and that is why it is necessary to have a method for calculation of these parameters.

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The goal of this paper is the easy and useful method for calculation of the thermoelectrically parameters of TEM.

These are $α_m$, $ρ_m$, k_m, coefficient of conversion $η$, quality factor Z_0 and the parameters of the materials $α$, $ρ$ and k, based on the information from the producer for the limited parameters of TEM.

The results observed are presented in table and graphical mode with the help of graph editor MATLAB.

II. MATHEMATICAL ANALYSIS

A. Expression of base dependences for cooling TEM.

Next equation (1÷4) are fundamental and they are described in books and papers [6,7,8,9]:

$$Q_c = 2N\left[αIT_c - \frac{1}{2}I^2\frac{ρ}{G} - kGΔT \right],\qquad(1)$$

Where:
- N – number of thermocouples in TEM;
- G – factor of geometry expressing the relation between the surface and height of the semiconductor element;
- I – electrical current.

The voltage U is given with:

$$U = 2N\left[I\frac{ρ}{G} + αΔT \right]\qquad(2)$$

And the consummated power from TEM W is:

$$W = U.I\qquad(3)$$

Quality factor Z_0 is the parameter, directly connected with the possibility of TEM to pump thermal power:

$$Z_0 = \frac{α^2}{ρ.k}\qquad(4)$$

Definition of the parameters $α_m$, $ρ_m$ u k_m:

$$α_m = 2.α.N\qquad(5)$$

$$ρ_m = \frac{2.ρ.N}{G}\qquad(6)$$

$$k_m = 2.N.k.G\qquad(7)$$

Using equation (5-7), the equation (1, 2 and 4) can be presented as:

$$Q_c = \alpha_m I T_c - 0,5 I^2 \rho_m - k_m \Delta T \qquad (8)$$

$$U = \alpha_m \Delta T + I \rho_m \qquad (9)$$

$$Z_0 = \frac{\alpha_m^2}{\rho_m . k_m}, \qquad (10)$$

B. Calculating thermal electrical parameters of TEM.

After reading the parameters from the producer data sheet: *ΔTmax, Imax, Umax u Qc$_{max}$*, the thermoelectrically parameters of TEM – Z_0, α_m, ρ_m and k_m could be calculated.

This method uses three of the limit parameters - *ΔTmax, Imax u Umax*.

$$Z_0 = \frac{2\Delta T_{\max}}{(T_h - \Delta T_{\max})^2} \qquad (11)$$

$$\alpha_m = \frac{U_{\max}}{T_h} \qquad (12)$$

$$k_m = \frac{(T_h - \Delta T_{\max}) U_{\max} I_{\max}}{2 T_h \Delta T_{\max}} \qquad (13)$$

$$\rho_m = \frac{(T_h - \Delta T_{\max}) U_{\max}}{T_h I_{\max}}, \qquad (14)$$

Where:

- T_h is the temperature of the hot side of TEM.

After the calculation of thermoelectrically parameters of the module, this easy the thermos physic parameters of the semiconductors to be calculated, from which the thermocouples are created – coefficient of Zeebec α, specific resistivity of the materials ρ and coefficient the thermal conductivity k.

It is done with the help of equation 5÷7, but only of the number of thermocouples N and geometry actor G which are known.

For calculation of the converting coefficient η and thermal resistivity of the hot radiator R_h next equation are used:

$$\eta = \frac{Q_c}{W} \qquad (15)$$

$$R_h = \frac{T_h - T_a}{Q_c + W} \qquad (16)$$

III. DISCUSSION AND RESULTS

The algorithm which is used for calculation of thermoelectrically parameters is shown on Fig. 1.
After the initially definition of the conditions and checking for correct their import the next calculation are done:

- Physical characteristics of the chosen thermoelectric module – quality factor Z, (K^{-1}); coefficient of Zeebec α_m (V/K); the resistance of the module ρ_m (Ω) and coefficient of module resistivity k_m (W/K);
- The base physical characteristics of the used for TEM thermoelectrically elements: coefficient of Zeebec α_m (V/K); specific resistance ρ $(\Omega.cm)$ and coefficient of thermal conductivity k $(W/cm.K)$.

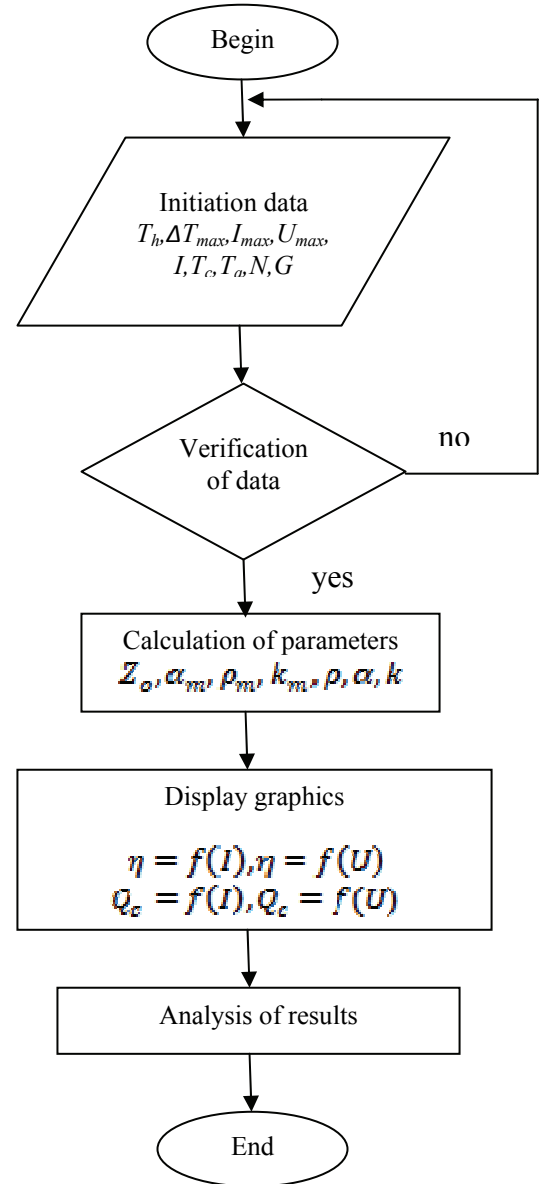*Fig. 1. The algorithm of modeling.*

The following is the presentation of the results in the table and graphical mode and their analyses.

The visualization of the results from the modeling of the thermal electrical module is performed with the help of the program product realized on the base the graphical editor MATLAB.

The program gives wide possibilities for the user, who can import high number parameters: limited parameters of TEM, shown in the producer data catalogue - $\Delta Tmax$, $Imax$, $Umax$, and well the working condition in which thermoelectrically module will be used.

They are:

- Input current I (in determined limits);
- Temperatures of the hot and cool side of the module – T_h и T_c. The hot T_h is firmly determined, but T_c is determined limits;
- The ambient temperature T_a;
- The number of the semiconductors thermocouples N;
- Geometry factor G.

Practically it can be simulated the work of every one arbitrary chosen TEM, if for all input data.

On Figure 2 the table the input/exit part of the working interface is shown.

The results, except in the table, are presented in graphical type.

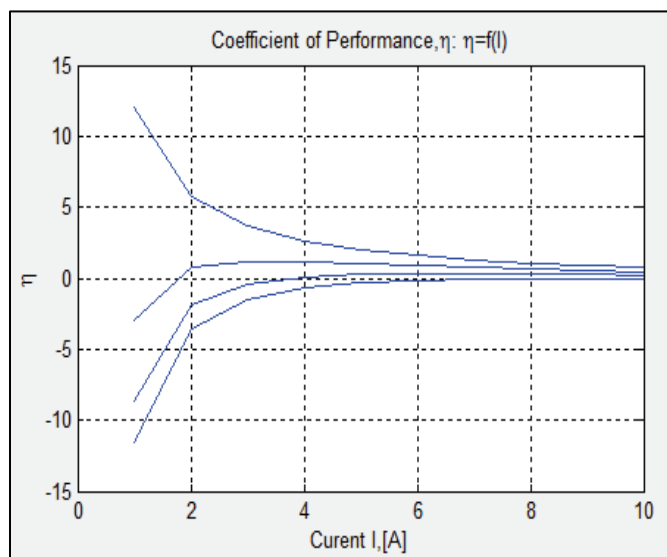The program proposes possibility four type of dependence to look at on and analyzed.

Fig. 3. Dependence of the performance coefficient η on the input current I: η = f (I).

- Coefficient of performance η as a function of the input current I: $\eta = f (I)$ – Fig.3;

- Coefficient of the performance η as a function of the voltage supply U: $\eta = f (U)$ –Fig. 4;
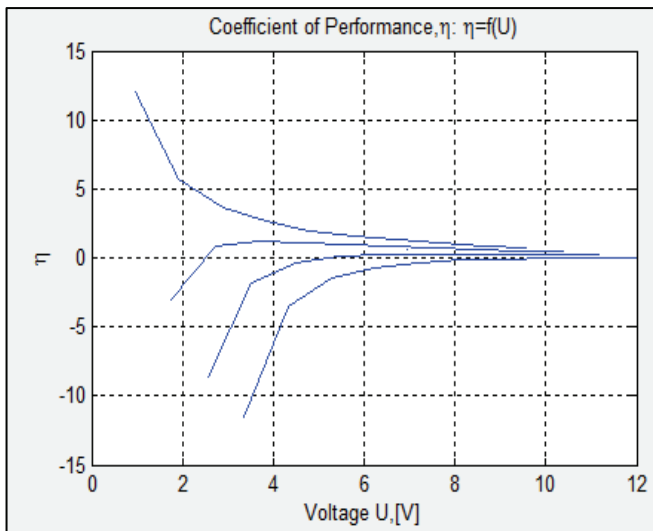
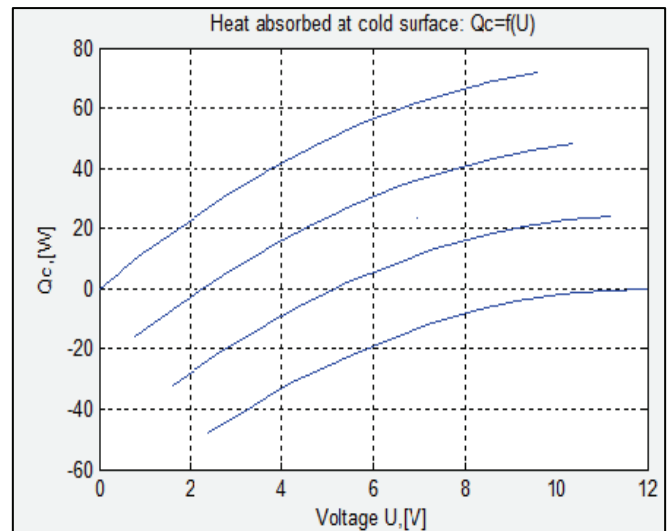Fig. 4. Dependance of the performance coefficient η on the voltage supply U: η = f (U).

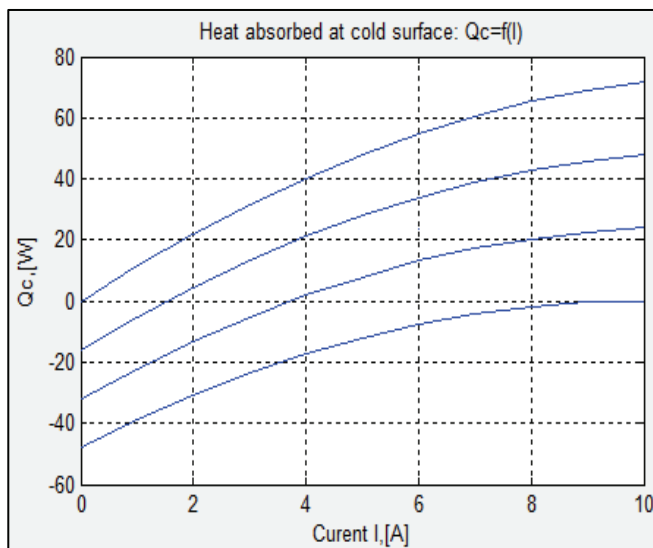Fig. 6. Dependance of the absorbed thermal power Q_c on the voltage supply U: $Q_c = f (I)$.

Fig. 5. Dependance of the absorbed thermal power Q_c on the input current.

- The absorbed thermal power Q_c from the cool side of TEM as a function of input current I: $Q_c=f (I)$ – Fig. 5;
- The absorbed thermal power Q_c from the cool side of TEM as a function of voltage supply U: $Q_c=f (U)$ – Fig. 6;

From Fig. 3 and Fig. 4 the efficiency of the given TEM can be estimated in dependence on DC mode of work.

The graphics from Fig. 5 and Fig. 6 show in which optimal values of input current and voltage the maximum values of the absorbed thermal power from the cool side of TEM could be reached.

IV. CONCLUSION

The realized mathematical model of thermoelectrically cooling module is a method with the user easily can calculate the base thermal physical parameters of TEM and for the semiconductors thermocouples, and in graphical way to report the absorbed thermal power Q_c in dependence on input current and voltage using a catalog information.

On the base of the received results it can select suitable cooling TEM in the design of thermoelectrically cooling – heating system.

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Mathematical model of control system based on programmable environment

Anatolii Aleksandrov [1], Goran Goranov [2], Pavel Hubenov [3]

Abstract – **The purpose of this article is to show consistency in implementation of the control system of a machine based on a programmable logic. It starts with a clarification of the requirements which determining its functionality and move on with calculation of a mathematical model of each block. The algorithm and the choice of the programmable environment for implementation are a topic of another article. Analysis of researched results.**

Keywords – **Logic gates, Control system, PWM, CPLD.**

I. INTRODUCTION

For reliable engineering sizing and implementation of a control system is extremely important to clarify the requirements which is based on. They are determined by industry, functionality, complexity, till the level of operators and lots of other factors but in conclusion – by the customer. In turn, requirements set the rules by which it will be designed and implemented - electric power modes, speed, management modes, to determine the nature and essence of each piece separately. The purpose of the designed machine is to drill holes and winding the thread in aluminum details.

Its principle of operation is as follows: the aluminum detail is placed in a magazine, loaded into the conveyor, transport towards a position, where the detail is preciously positioned, drilled by "Station1" for two holes, transported to the next position to the "Station2", wherein the cut thread, and exported by the conveyer. Then the cycle is repeated.

The operating accuracy of the machine depends on mostly of the accuracy of the angular displacements. There are few approaches for their realizations. The simplest block diagram is shown on Fig.1, a). An advantage of the method is easier to maintenance the system in time and at a lower cost. The disadvantage is the lack of feedback to control the speed by direct data delivery in case of faults situation. Tracking the speed of the shaft directly is impossible, and everything depends on the accuracy of microprocessor driver and the constant load. The only way to observe the statement of the motor is by consumed current. It is widely used in packaging machines with stretch film. [1, 2]

Second method includes feedback realized by three Hall

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sensors, installed at 120 °, which allows the monitoring of the speed and direction of the motor shaft. The advantage of this configuration is the timely reaction of the driver in the event of faults situation. Also, the motor speed can be controlled by managing more precise and reaction on time, even if the load is dynamic, Fig. 1, b). It is used in the management of conveyors or drives with frequent changes of direction or speed. [3, 4]
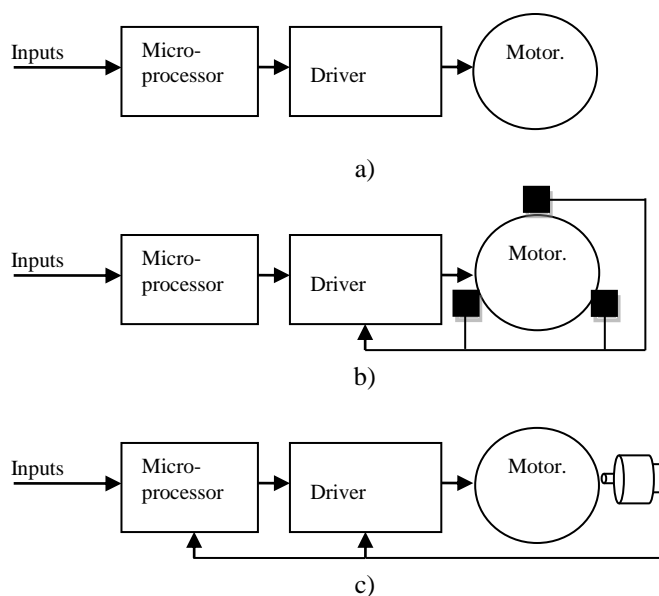

Fig. 1. Basic motion solutions

The most precise of the three configurations is shown in Fig. 1, c). The shaft is coupled with an encoder (photoelectric converter). Its function is to convert the angular displacement in a pulse sequence, i.e. pulses are corresponding to just one turn of 360 °. Basically pulses per round are multiple of 2^n. There are exceptions, such as those with resolution 200, 400 or more pulses per turnover. For precious tracking the location of the shaft is necessary installation of a sensor for a specific referent point. In this case, the microprocessor looks for this signal and launches counting pulses from the converter. For achieving this goal can be used the embedded in the encoder reset pulse, which is only one for a turnover. The disadvantage of the approaches with sensor or reset pulse, the error that occurs due to the timing of engine braking and the subsequent vibration. When positioning is critical, processor permanently monitor this pulse sequence, ready to stop the cycle of operation of the machine and put the alarm. It can be avoided by using a delay circuit ensuring a delay. The time delay method allows the signal of the sensor to be delayed within a few pulses or time respectively few microseconds. [5]

Even better positioning is achieved using absolute encoder. Differentiations from the previous one is that each position corresponds to a set of *n*-bit digital code. In this way positioning is sufficiently precise because every single position defines data which is unique. Although power supply interruption could occur, the position will be remembered and the cycle resumes without failures.

The provided data is usually in binary code 8-4-2-1 but higher noise protection can be achieved easily when output data is in Gray code. This method of control allows the realization of dynamic brake at which the processor supports the entire drive unit in a stable stationary. These are so-called servo systems. Widely applicable at positioning of robots, CNC class machines, confection cutting machines and extruders in polyethylene industry, and more. [6]

To ensure correct positioning of components, set system requirements determine the type of approach used and the specific drivers and their associated control units.

II. MATHEMATICAL MODEL OF THE BASIC MODULES

When the requirements are completely fixed, has to design the plan for algorithm design. The more detailed it is, the more easily design of as small as possible modules regarding the functionality.
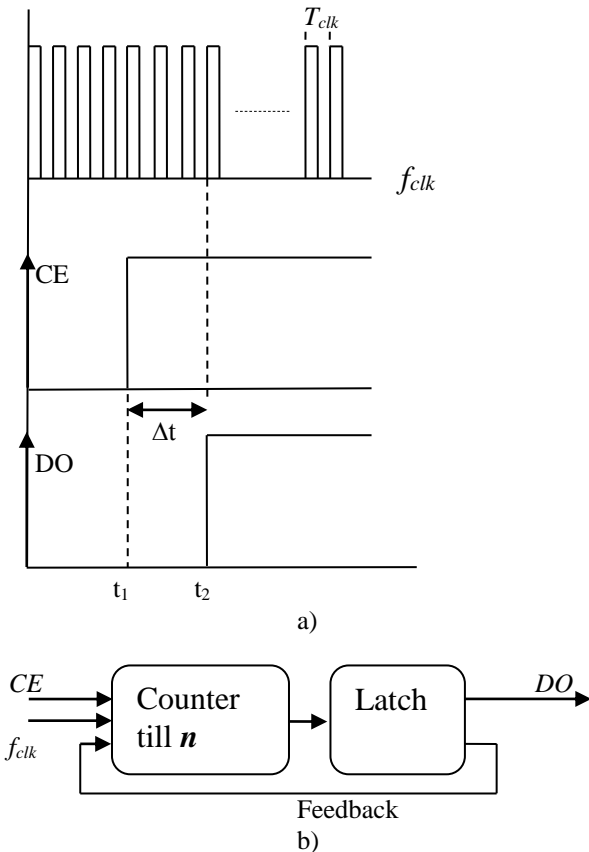

a)

b)

Fig. 2. Transition diagram and schematic of a delay line

Thus, by making easier for synthesis modules is achieved faster integration in a complex system, quick add or remove functionality and easier debugging. Using this approach, the main types of circuit solutions are simplified to next four modules - Time Delay Line, combinational scheme with X-input and Y-output (Code Converter), Digitally Controlled Frequency Generator, Pulse Width Modulation Generator.

1. Time Delay Line

The block diagram of the delay line circuit is given in Fig.2, b). It provides accurate time delay. The difference between the received input signal and delayed output one is

$$\Delta t = t_2 - t_1 = n.T_{clk} \text{ [sec]}, \tag{1}$$

where *n* is the number of periods which the counter has to count and then triggers the latch, fig.2, a). The latch itself ensures a stable and resistant statement and as per the feedback blocks the clock frequency pulses.

2. Code Converter

The second module Code Converter is shown in Fig. 3. Basically it is a combinational circuit which provides output binary data according to the input binary data. Applicable when switching relays, e.g. controlling a pneumatic distributor, a pump, a fan, etc., based on the input performance of various conditions. They could be driven by signal of active sensor, limit switch, or signal for completed cycle of a previous module within the algorithm. This kind of block has from one to lots of number of outputs depending on its application - provide simultaneously enable or disable output signal towards other modules.

a)
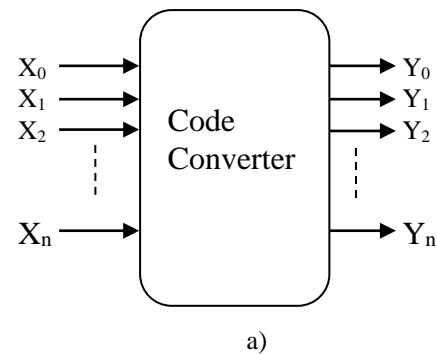
X_n	…	X_1	X_0	Y_n	…	Y_1	Y_0
$[CS_n]$		$[SS_1]$	$[CE]$	$[t+1]$	$[t+1]$	$[t+1]$	$[t+1]$
0		0	0	0		0	1
1	1	1	1				

b)

Fig. 3. Schematic and diagram of Code Converter

The state transition diagram is shown in Fig. 3, b) where in the left side are filled input magnitudes and in the right side are output ones corresponding to the adjacent input sets. The right side is the statement in the next moment *t + 1*. Left located sets could be different conditions (for example: CS_n − Control

Signal n, SS_1 – Signal Sensor 1, CE – Control Enable), which will provide signal for execution. Mostly converters owned a large number of input signals - 1 till 10 an above, but could be used only strongly defined sets. In this case, the synthesis must take into consideration that such a function is incomplete and should be threat using an extra approach to avoid unacceptable switching. They are in relationship to the statement so called "not defined" which has to be include in the synthesis. When the outputs are more than one, every single one has to be synthesized by minor members into separate own table using Karnaugh or Veitch mapping output equation, which is converted to the preferred type of basic logic units – AND-OR, NOR, or NAND. Finally, subsequently schemes for different outputs are combined into a common combinatorial scheme. [7]
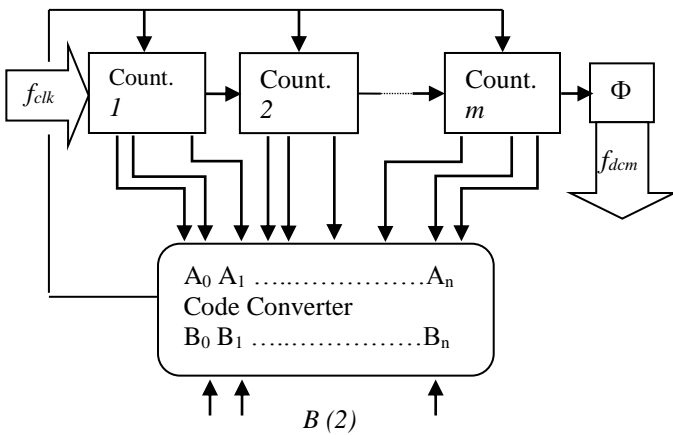
3. Digitally Controlled Frequency Generator

Fig.4. Block schematic of frequency generator

Block schematic of the generator is displayed in Fig.4. Generally, it is useful for frequency control of stepper motor's driver. The driver is allowed to control the motor by micro steps, i.e. a defined number of pulses is needed to be realized one complete revolution of the motor shaft. For example, the selected driver has a maximum number of 51200 steps per revolution, which means that a 360 degrees' rotation will be reproduced by 51,20kHz for just a second. Since this engine drives a conveyor and does not work in synchronization with another one, the requirements for it does not obligate the frequency to be exactly an integer than to be stable in time. This is the reason lead to the choice of this approach for implementing the control scheme. Otherwise could be use other method when a phase noise is observed, but the frequency is an integer and can be changed in small steps, for example 1.0 Hz.

The output frequency is determined by the formula:

$$f_{dcm} = f_{clk} / B(10), \qquad (2)$$

where number B is in binary-decimal system, but is entered in binary code to the inputs of Code Converter. [8]

4. Pulse Width Modulation Generator

The approach for pulse-width modulation is given in Fig. 5, b). As per the block diagram of the generator, the more complexity the more precision of the duty cycle is achieved and the most capacity of programmable platform is available.

The principle of operation is as follows: multiplexer provides M_2^n number of channels, each of them is active for a defined time. It is determined by l-bit counter "CN.1", which counts the pulses of clock f_{clk}. This counter provides an output signal when overflow and switches counter "CN.3" which manages the address inputs of the multiplexer.
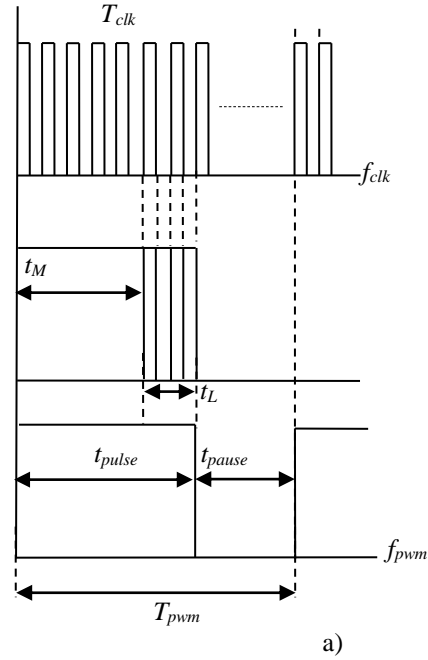
a)
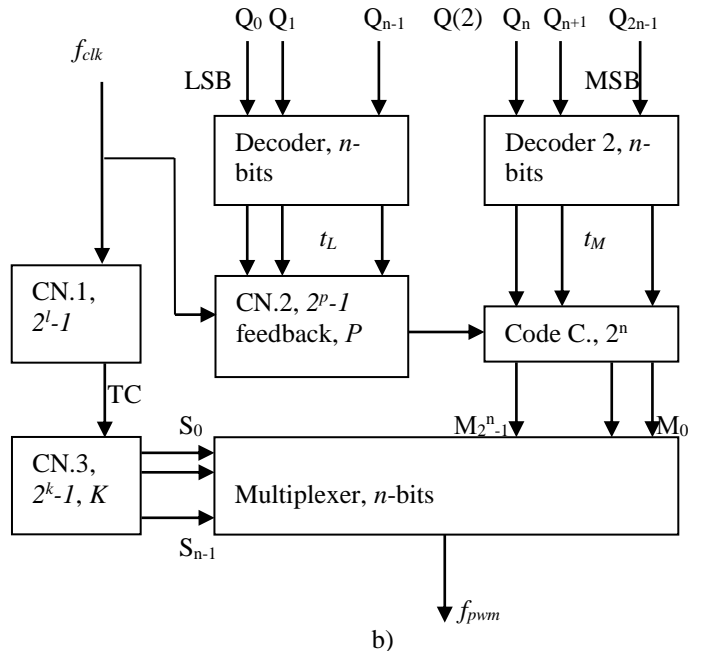
b)
Fig.5. PWM generator

To realize the logical high level from the period T_{pwm}, Fig. 5. a) is used code converter "CC" which output code is code of

Johnson, providing a high level to the inputs of the multiplexer. It is managed by "Decoder 2" and "Code C" delivers to all junior multiplexer's channels, logical high level. For the current active channel of the decoder, "Code C" receives a signal from the other decoder. After counting the pulses from p-bit "CN.2" starts logical low level of the period T_{pwm}. That period of F_{pwm} is determined by the equation:

$$T_{pwm} = t_{pulse} + t_{pause} \text{ [sec]}, \qquad (3)$$

where t_{pulse} is the time of the logical high level Fig. 5, a). This time is the sum of the other two:

$$t_{pulse} = t_M + t_L \text{ [sec]}, \qquad (4)$$

as they are received from "Decoder 2" and "Decoder 1". Both decoders are managed separately by n-bit code, but connected as per their ranking by importance – starts with the most insignificant, LSB (*Low Significant Bit*) towards the most important, MSB (*Most Significant Bit*). The time specified by the decoder for the most significant bit (MSB) is:

$$t_M = (K-1).t(K) \text{ [sec]}, \qquad (5)$$

where K is the number of the active channel of the multiplexer. Active time for each single channel is:

$$t(K) = 2^l . T_{clk} \text{ [sec]}. \qquad (6)$$

The time specified by the decoder for the least significant bit (LSB) is:

$$t_L = P . T_{clk} \text{ [sec]}. \qquad (7)$$

Here P is the number to which the external feedback of the counter "CN.2" is adjusted and then resets.

The step, or the quantum, by which the duty cycle of the pulse width modulated signal is determined is by the coefficients k and l:

$$Qu = 100 / (2^k . 2^l) \text{ [\%]}. \qquad (8)$$

Duty cycle λ is determined by:

$$\lambda = (t_{pulse} / T_{pwm}).100 \text{ [\%]}. \qquad (9)$$

The number Q, managing decoders and sets duty cycle, is the described as:

$$Q (10) = \lambda / Qu \text{ [\%]}, \qquad (10)$$

then converted into binary and is provided to inputs Q_0 - Q_{2n-1}. The condition, which must be strongly obligated to be kept in the method of realization of the PWM signal is:

$$p \le l. \qquad (11)$$

Both mentioned generators in the above are designed so as to be controlled by binary parallel code. This approach allows changing the speed of the controlled motor to be performed from minimum to maximum within a single period of the clock frequency. It is useful whether the engine has a number of different speeds.

III. CONCLUSION

The approach of the control system implemented in the drilling machine is recognized by using easy synthesis of all types of modules. It allows the system to be designed and implemented sufficiently simply, efficiently and reliably. The platform successfully responses to the requirements is CoolRunner-II, with mounted programmable logic matrix XC2C256-7TQG144C. Used matrix delivers flexible enough base for fine adjustments during the revival of the system and subsequently in its implementation as control unit in real facility.

Differenced from other types of architectures of programmable devices, where the number and functionality of the various blocks are factory pre-determined, everything here depends entirely on the designer and made synthesis. The methodology combines mathematical model and synthesis through minimization of logic functions, allows the expansion of the control system with more than one programmable matrix to remain just as easily and reliably. The implementation of functional logic elements makes this approach applicable in almost all the developments of programmable logic controllers series of leading manufacturers. The advantage is much wider audience, unlike using any other language for programming. To be continued with second article which describes algorithm and realizations of logic gates schematics.

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Electronic Module for 2D Positioner Manuel Control

Nikola Draganov[1] Totka Draganova[2] and Dragan Draganov[3]

Abstract – **Electric drives are wide used in engineering practice. Precise operation and easy control of stepper electric motors had put their application in exact position fixing. The stepper motors in combination with control can provide a flexible operation and awards an opportunity to make reliable electric drives systems. Experimental model of electronic module for 2D positioner control based on two small powerful stepper electric motors and programm-able logical matrix is presented in the report.**

Keywords – **magnetic fields control, stepper electric motors, programmable logical systems.**

I. INTRODUCTION

Stepper electric motors are often used in the practice as electric drives of different machines and equipments. Special units are used for this effect which are able to control the motor poles so that can carry out needed operations.

There are electromechanical units doing manipulations as position fixing of details, reading and writing heads which fine control is unimaginable without stepper electric motor. In some cases is not necessary to do this fixing automatic but manuel. So the operator directly assigns a direction, speed and a shifting distance.

Electric motors electronic control can be made by different manners. There are such units with discrete logic, microcontrollers and programmable logical matrixes. The last give a possibility for a flexible change of the discrete logical circuits and also to have a programming of their functions with some much possibilities – operating frequency, time constants etc.[1, 2, 3].

The aim of this elaboration is to propose, fulfill and investigate an experi-mental model of electronic module for control in two directions (2D) positioner by means of two small powerful stepper motors and programmable logical matrix. The developed unit can be applied in auto-mation, electronics and engineering practice for creating of different units for position fixing in 2D plain which are controlled by voltage level. The circuitry and experimental results of the unit which determines the direction and the rotation speed of electric motors in relation to the applied input voltage are presented.

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II. PRESENTATION

A block schematic diagram of the created experimental unit is depicted in Fig.1. It is intended for the position in 2D plain manuel control. Two small powerful stepper electric motors (SM) of the type KP39HM4-016 produced by Matsushita [4] are used. They control the motion of the metal frame in two directions. The block schematic diagram of the electronic unit is composed by three modules – set up generator-modulator (SGM), program-able logical device (PLD) and power device (PD). The control module executes double function. It assigns a motion direction of a corresponding motor (to X or to Y) and its rotation speed. SGM is created by two identical set up circuits (SC_X or SC_Y). They produce a signal to PLD which shows the rotation direction and a signal to controlled by voltage generator UFG. The rotation direction of the corresponding motor is determined by the sliding contact of the potentiometer position (control X or control Y). The resistance change of the potentiometer makes a control signal change to controlled by voltage block generator (UFG). It is a system of two channels generator for rectangular pulses. Its frequency is controlled by voltage given from corresponding set up circuit. So by SGM are made two independent pair pulses XCLK, XDIR and YCLK, YDIR with different (independent) frequencies. They give a clock signal and the rotation direction of both motors.

The LPD is the basic module. It is made on the base of a developmental system CoollRunner II, produced by Xilinx [5]. The platform consists of CPLD programmable logical matrix XC2C256 in case TQG144 and peri-pheral modules – JTAG programmer, clock generator, display, buttons, etc [5]. The programme is written down in a this block memory. It generates a defined sequence of pulses for motors correct management. After their for-ming the ruling signals come in power module (PM). Two independent each other signal pairs $X_{1'2}$ and $Y_{1'2}$ enter to a driver block (PD) input. They control the motion to X and Y. PD supplies with needed current and voltage motors coils SM_ X and SM_Y.

The set up generator–modulator (SGM) schematic circuit diagram is depicted in Fig. 2. It consists of set up circuit SC_X and controlled by voltage generator UFG. SC_X defines a motor rotation direction. It is made by means of opera-tional amplifiers IC_{1a}, IC_{1b} and IC_{2a}, IC_{2b} and connected with them elec-tronic components – resistors $R_1 \div R_{12}$, capacitors $C_1 \div C_3$, C_5 and diode D_2, D_3. This circuit generates two signals. The first is used for voltage-fre-quency generator UFG control (elements IC_{2b}, IC_{2c}, IC_{2d}, D_1, $R_{13} \div R_{17}$). The second signal defines a motor rotation direction. The Y channel control is absolutely the same. The corresponding block generates signals for control of a speed and a direction (YCLK and YDIR).

This block circuit operation is defined by sliding contact voltage of a potentiometer R_P and its comparing with standard defined. The sliding contact place defines the rotation direction. In its middle position the voltage is equal to a half of supplying voltage. The amplifier IC_{2d} works as an integrator but IC_{2b} as a comparator.
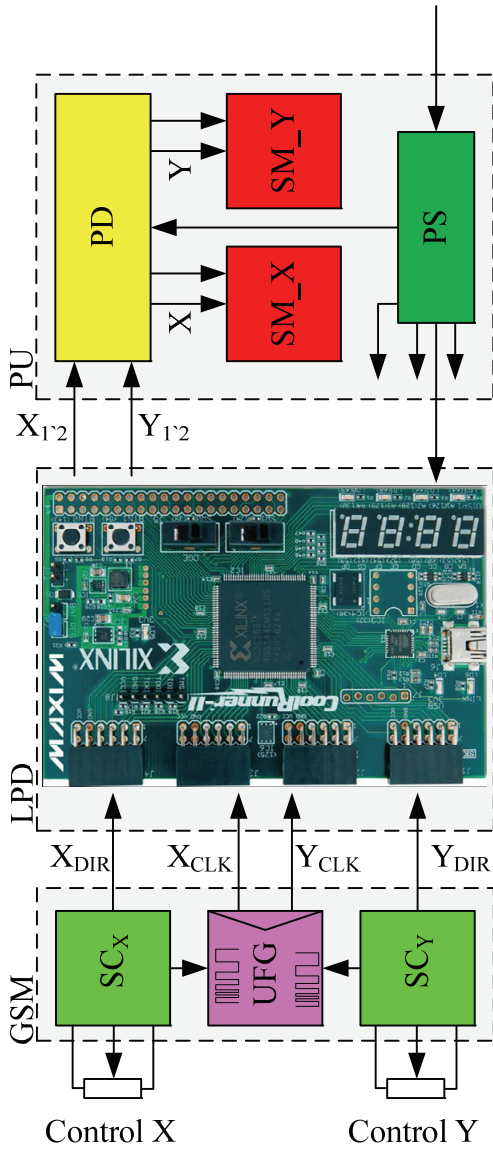
starts to generate pulse XCLK. The describing operation of module SCX timing diagrams are depicted in Fig. 2.

The received from UFG signals determine motor control speed to X and Y.

The signal levels XDIR and YDIR define their rotation direction. They are given to inputs of a programmable logical device PLD.

Fig. 1. Block structure of the electronic unit
for 2D positioner control
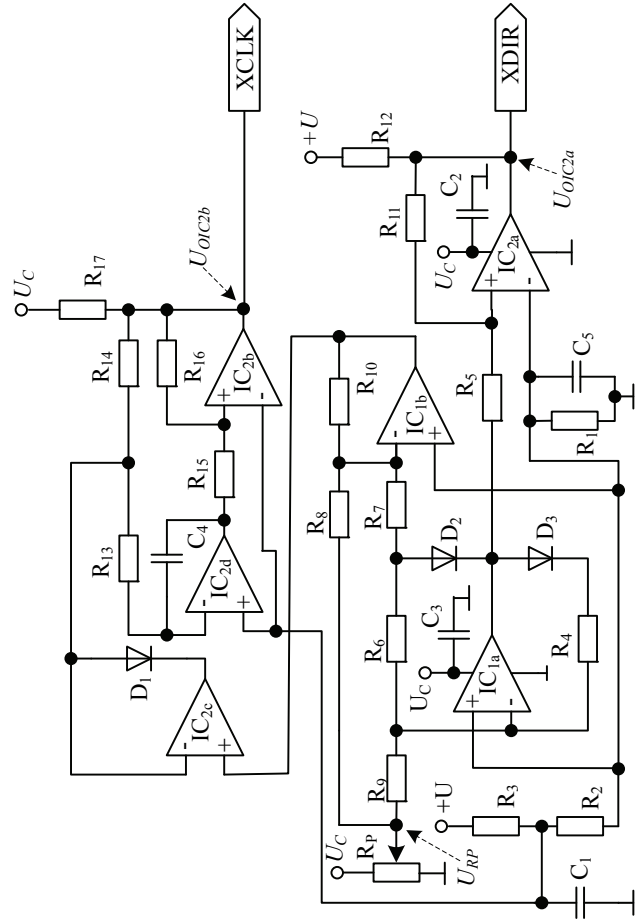
Fig. 2. Simplified schematic circuit diagram of an analog module
for X channel control

They both build together a generator which is controlled by a voltage limited by IC_{2c} and by a connected in its feedback D_1. The voltage value at which pulse generations appear is dependent on the values of resistors $R_1=10k\Omega$, $R_2=50k\Omega$, $R_3=10k\Omega$. They are so selected and define the control voltage to be equal to a half of supply. When the potentiometer is moved to any direction from the middle position the comparator IC_{2a} without delay sets up at it output a corresponding level (0 or 1) and the shifting value is determined by the voltage value at the output of IC_{1b} and it

Fig. 3. Timing diagrams describing an analog module operation
given a direction and speed rotation

TABLE I
THE CONFIGURATION OF A PROGRAMMABLE LOGICAL MATRIX PINS

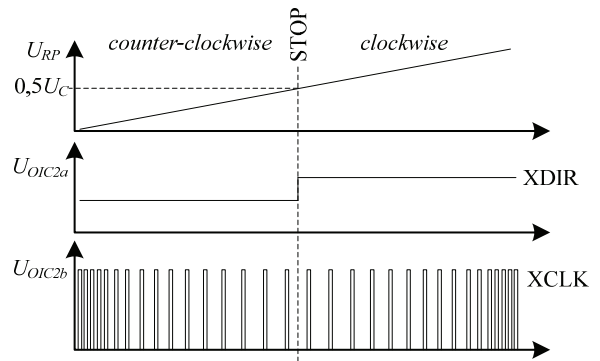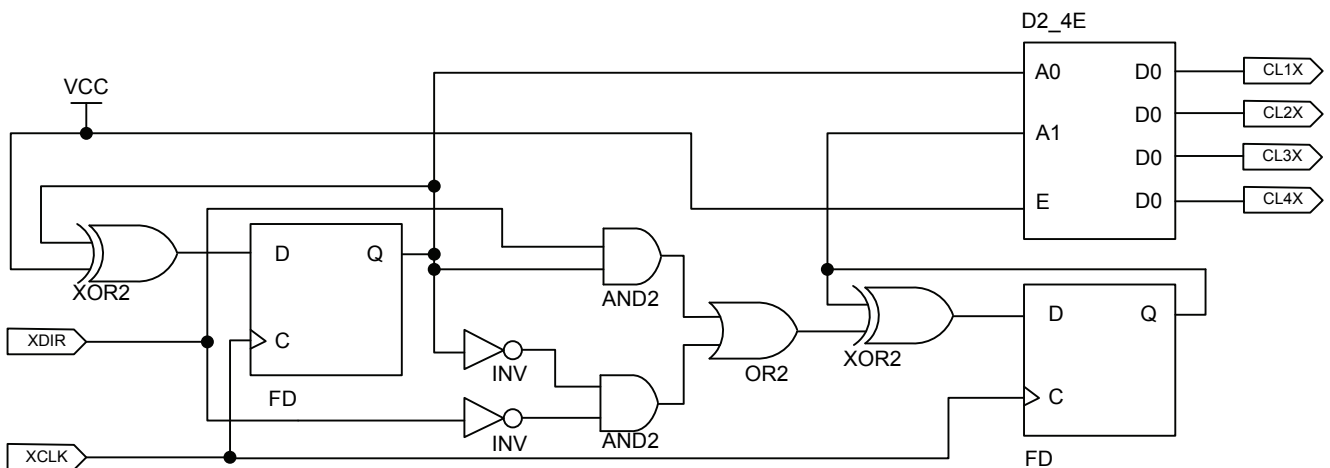| Type of Signal	Control by X direction	Control by Y direction	
	Name of Signal – pin number	Name of Signal – pin number	
INPUTS	XCLK – p124	YCLK – p39	CLOCK
	XDIR – p38	YDIR – p38	DIRECTION
OUTPUTS	CL1X – p10	CL1Y – p143	Control coil L1+
	CL2X – p7	CL2Y – p139	Control coil L1-
	CL3X – p5	CL3Y – p136	Control coil L2+
	CL4X – p3	CL4Y – p134	Control coil L2-

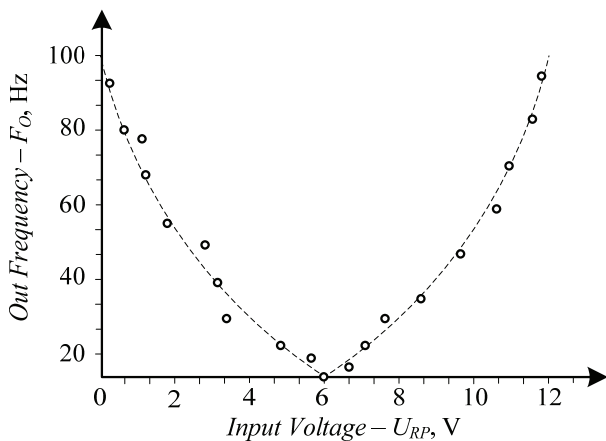Fig. 4. Programmed in CPLD circuit for control to X only

Fig. 5. Conversion characteristic of one channel in device UFG – $F_O=f(U_{RP})$

The signals from both channels are treated by PLD. For unit realization are necessary both hardware and software. The logical matrix is programmed by a software ISE Design Suit 10.1 produced by Xilinx [5]. The CPLD programming can be made by two methods.

The first is by a programme code drafting. The other used here is by a desired circuit drowing with available in section schematic prepared libraries with function-nal elements. A software conceptual electric circuit is depicted in Fig.4.

The formed in device UFG signals go to the programmable logical matrix inputs. They are configured so that the signal XCLK controls D-triggers FD (Fig. 4). A direction signal comes to logical scheme which controls the se-cond trigger so that a decimal counter has to sum up or to subtract. A modu-le PLD generates 4 signals (CL1X, CL2X, CL3X, CL4X) used for driver control of motors. The configuration of a programmable logical matrix pins in relation to input and output signals of both channels is depicted in table1 1.

The output signals for both control channels X and Y are absolutely inde-pendent. They come to driver block PD. The conceptual electric circuit of one channel in driver block is depicted in Fig. 6. The signals from CPLD are inverted by input buffers IC3. Each pair signals CL1X, CL2X and CL3X, CL4X controls MOSFET transistors (Fig. 6) in a H-bridge. One diagonal of both bridges is connected to voltage supply.

Another is connected to electric motor coil. The bridge circuit based on transistors VT1,VT2,VT3,VT4 controls a coil L1 while a bridge with VT5,VT6, VT7, VT8 controls a coil L2 (Fig.6 and table 1).
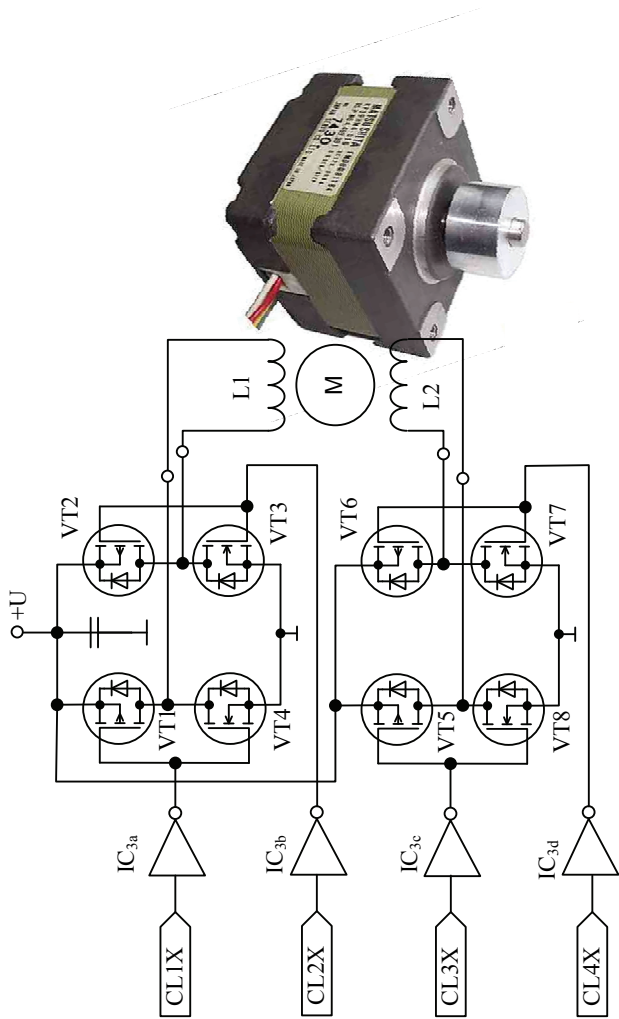

Fig. 6. Conceptual electric circuit of one channel in driver block

III. Conclusion

An experimental unit for manuel control of 2D positioner is exploited. It is made up a block circuit describing the operation of electronic unit. A con-ceptual electric circuit composed of three basic modules – set up generator, programmable logical device and power module is realized. A software for programmable logical device is created in programme medium ISE Design Suit 10.1 produced by Xilinx. The programming is made with build in deve-lopmental platform JTAG programmer. The realized unit is experimental investigated. The results are:

1. The timing diagrams in special check points having effect upon unit operation are obtained by means of electronic oscilloscope and are depicted in Fig. 4

2. A conversion characteristics of one channel of block UFG (Fig. 5) is obtained. It shows a dependence between a generator output frequency F_O change and a voltage U_{RP} supplied to its output by means of potentiometer R_P .The analysis shows that it is symmetrical in relation to the middle value of the stabilized voltage supply (1/2 U_C = 6V). The experimental character-ristic shows that controlled by voltage generator exibits nonlinearity.
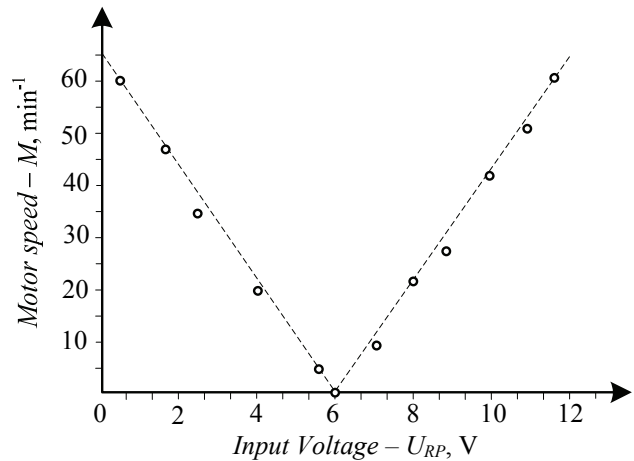

Fig.7 Experimental characteristic $M = f(U_{RP})$

3. The dependence of electric motor M rotor rotation speed on input voltage coming from potentiometer RP is investigated. The characteristic $M=f(U_{RP})$ is depicted in Fig. 7. It is symmetrical and linear. When a half of voltage is supplied the stepped motor stops. It is established the same change range of rotation sped from an input voltage U_{RP} in relation to initial value U_{RP}= 6V. This range is symmetrical to both rotation directions – from left to right at U_{RP} = 6÷12V and backwards from right to left at U_{RP}= 6÷0V the electric rotor rotation speed rises to $M = 60$ min^{-1}.

The created unit can find a wide application in research laboratories and in engineering practice by the different positioners, machines and equipments, mechanical cutter, leth, metrology etc.

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Study of Nonlinear Effects in Parallel Gyrator Resonance Circuits

Atanas Tanev[1], Ivan Uzunov[2], Marin Hristov[1], Sotir Ouzounov[3]

Abstract – **This paper investigates the behaviour of bandpass filters, realized with parallel gyrator tank, at high input signal levels. The goal is to find a in an empirical way correlation between the harmonic distortions of the gyrator amplifiers and the changes of the filter frequency response. When known, this dependency can be used during amplifier design to improve the performance of the filter and decrease its cost.**

Keywords – **nonlinear distortion, OTA-C filters, bandpass filters, gyrators, frequency response.**

I. INTRODUCTION

The optimization of the dynamic range is a significant problem in active filter design [1]. The problem in fact consists of two sub-problems, often solved simultaneously: maximizing the maximum permitted signal and minimizing the circuit noise. The maximum signal at the filter output is limited by the available voltage headroom and the acceptable level of distortions of the output signal. The methods for dynamic range optimization usually aim to equalize the output voltages of the amplifiers in the filter. However, the existing methods typically do not consider how the filter frequency response changes depending on of the amplifier nonlinearities.

The changes of the filter frequency response due to amplifiers' non-linearity are studied since a long time. The focus has been on second-order bandpass filters due to their simplicity, considering basically gyrator equivalent of the LC tank [2,3] and a single operational amplifier biquad [4,5]. Their frequency response inclines at large input amplitudes (Fig. 1) due to nonlinearities in the active elements, which leads to three main effects: 1) The frequency response is no longer symmetric; 2) Its maximum moves usually to lower frequencies; 3) Appearance of the so called "jump phenomenon" at certain nonlinearity levels. The frequency response changes with a jump at a certain frequency and the suggestion is that it is due to appearance of area, in which the response has two values (dotted line in Fig. 1).

Different techniques are applied for analysing the influence of the nonlinearities. In [2,3] analytical expressions are derived that link the level of non-linearity to the filter parameters in gyrator filters. In these studies, the operational trans-

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conductance amplifiers (OTA), used in the gyrator, are represented by equivalent large-signal value of the transconductances g_m where the g_m is impacted by the amplifier's nonlinearity. More complicated methods have been proposed for achieving better accuracy and analysis the nonlinear effects in higher order filters. For example, the harmonic balance method is applied in [4,5], while in [6,7] Volterra series analysis is used. State-space analysis of the harmonic distortions in OTA-C filters is considered in [8].
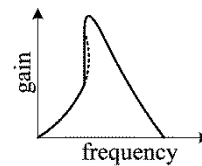

Fig. 1. Inclining the frequency response and "jump phenomenon" in second-order band pass active filters due to amplifier nonlinearities.

The review above shows that most of the existing methods for theoretical analysis of the nonlinear effects in the active filters are approximative and in most of the cases do not rely on powerful tools for simulation of electronic circuits like Cadence, PSpice, etc. Also, there are some questions that remain unclear. For example, the term "weak nonlinearities" is used without precise definition. Further, the relationship between the total harmonic distortion (THD) of the amplifiers and the variation of the filter frequency response it is not well clarified.

The goal of this paper is to study empirically these questions for one of the most popular bandpass filter – the gyrator parallel resonance circuit (gyrator tank). This is done by computer simulation of filter with different types of OTAs with different nonlinearity. The results demonstrate various effects in the frequency response and allow to estimate the limits of OTA's THD in conjunction with the tolerable changes in the filter frequency response.

II. GYRATOR PARALLEL RESONANCE CIRCUIT AND MODELLING OF OTA V-I CHARACTERISTIC

The circuit of the bandpass filter, realized as parallel gyrator resonance circuit, is shown in Fig. 2(a). The gyrator consists of g_{m1} and g_{m2} and forms the resonance circuit together with the capacitors C_1 and C_2. OTA g_{m0} at the input converts the input voltage to an equivalent current for proper operation of the tank and R is the load resistance. The general form of the small-signal filter transfer function is

$$H(s) = \frac{V_o}{V_i} = \frac{hs\omega_0/Q}{s^2 + s\omega_0/Q + \omega_0^2}. \tag{1}$$

Its angular resonance frequency ω_0, Q-factor and gain h are:

$$\omega_0 = \sqrt{\frac{g_{m1}g_{m2}}{C_1 C_2}}; \quad Q = R\sqrt{\frac{g_{m1}g_{m2}C_1}{C_2}}; \quad h = g_{m0}R. \quad (2)$$

The corresponding frequency response is symmetrical around ω_0 when logarithmic scale is used for the frequency axes. Examples for two different Q-values are shown in Fig. 2(b).
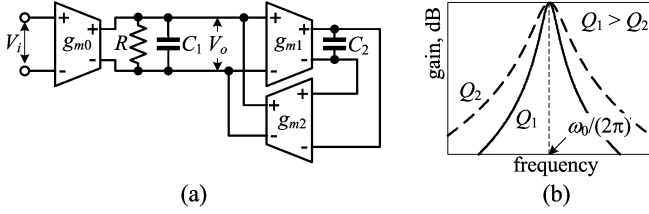

(a)   (b)

Fig. 2. (a) Circuit of bandpass filter realized as parallel gyrator resonance circuit; (b) filter frequency response at two different pole Q-factors.

The investigation is focused on the impact of the nonlinearites in g_{m1} and g_{m2} on the filter frequency response. The harmonics produced in the input OTA g_{m0} typically are filtered by the gyrator tank. They may have visible effect only when the input signal is too large and the fundamental frequency of the signal is 2 or 3 times lower than $f_0 = \omega_0/(2\pi)$. For this reason this amplifier is considered as an ideal voltage controlled current source (VCCS). Its transconductance is equal to $1/R$ in all simulations in order to have unity gain at the filter central frequency f_0.

The other two OTAs g_{m1} and g_{m2} are considered as nonlinear VCCS and their transfer characteristics $i_o(v_i)$ (i_o – OTA output current, v_i – OTA input voltage) are approximated by polynomials. Two different circuits are taken as models: the simple differential pair with dynamic load in Fig. 3(a), and a differential amplifier with linearization (Fig. 3(b)). The linearization of the second amplifier is achieved by source degeneration resistors – transistors M_3-M_6 are used for this purpose. This amplifier also uses dynamic load. A negative resistance emulated by the pair M_9-M_{10} is connected in parallel to the output for increasing the output impedance. The common-mode feedback circuit (M_{cf1}-M_{cf4}) is shown also in Fig. 3(b).

The studied circuit has been proposed in [9] and investigated in [10]. Its linearity is controllable by parameter a, equal to

$$a = \frac{(W/L)_{M1-2}}{(W/L)_{M3-6}}, \quad (3)$$

where $(W/L)_{M1-2}$ is the aspect ratio of transistors M_1 and M_2 and $(W/L)_{M3-6}$ of $M_3 - M_6$. The value of a determines the achievable linearity and the best linearity is at an optimal a.

The $i_o(v_i)$ characteristics of the amplifiers is obtained by multiple time domain simulations with a sinusoidal voltage source at the input (terminals "$+V_{in}$" and "$-V_{in}$"), which amplitude is increased gradually. The output current flows through capacitor of 10nF, connected at the output (terminals "$+V_o$" and "$-V_o$"). The frequency is 10kHz and the capacitor impedance is about 1.6kΩ, which is much less than the amplifier output impedance – i.e. the capacitor realizes an approximate short circuit. The transfer characteristics are simulated with AMS 0.35 μm CMOS process used in the education. The sizes of all transistors are $W = 10$ μm, $L = 0.35$ μm and only the widths of M_1 and M_2 are varied to achieve the desired parame-

ter a. Tail currents I_{ss} are 35μA for the circuit in Fig. 3(a) and 100μA in Fig. 3(b). Their values are chosen in order to have approximately equal g_m's (about 150μS) of both circuits. The simulated transfer characteristics are shown in Fig. 4(a). Since they almost overlap for the amplifier in Fig.3(b), the dependence of THD from the input voltage, plotted in Fig. 4(b), is used to demonstrate how the parameter a affects the linearity.
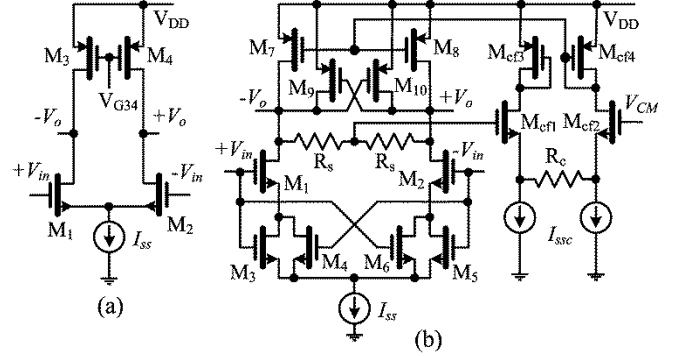

(a)   (b)

Fig. 3. Circuits used for modelling of OTA nonlinearities: (a) simple differential pair; (b) differential amplifier with linearization.
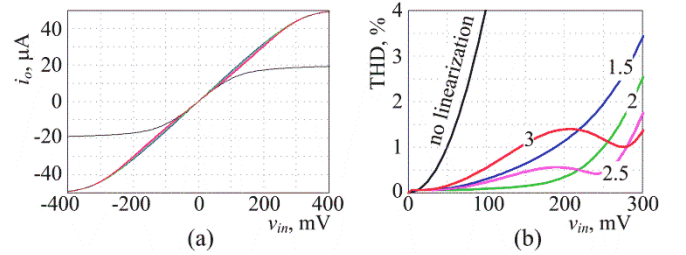

(a)   (b)

Fig. 4. (a) Transfer characteristics $i_o(v_{in})$ of the amplifiers; (b) THD of the output current vs. input voltage v_{in}. Black curves are for the circuit in Fig. 3(a); the others are for Fig. 3(b): blue – a=1.5, green – a=2, magenta – $a = 2.5$, red – $a = 3$.

The next step is to receive an analytical approximation of the characteristics in Fig. 4(a). Often is used tanh approximation, however the polynomial approximation is preferred here as more flexible, allowing to achieve of better accuracy. The OTAs are fully differential with symmetrical characteristics and the approximating polynomials are odd in the form

$$i_o = \alpha_1 v_i + \alpha_3 v_i^3 + \alpha_5 v_i^5 + \cdots \quad (4)$$

The degree of polynomial is increased gradually until achieving relative approximation error of 1% for amplitudes of v_i up to 0.5V. The polynomial for the OTA in Fig. 3(a) is: $i_o = 1.454{\times}10^{-4}{\times}v_i$ $-0.00242{\times}v_i^3$ $+0.0325{\times}v_i^5$ $-0.2694{\times}v_i^7$ $+1.296{\times}v_i^9 -3.306{\times}v_i^{11} +3.452{\times}v_i^{13}$, where v_i is in volts and i_o is in amperes. The polynomials for the OTA with linearization are of 7th degree and their coefficients are given in Table 1.

TABLE I. COEFFICIENTS OF APPROXIMATING POLYNOMIALS FOR THE CIRCUIT IN FIG. 3(B).

Parameter a	α_1	α_3	α_5	α_7
1.5	0.0001648	$-6.587{\times}10^{-5}$	-0.001995	0.004943
2	0.000158	$8.857{\times}10^{-5}$	-0.003008	0.006985
2.5	0.0001503	0.0002396	-0.003932	0.008776
3	0.0001428	0.0003765	-0.004735	0.0103

III. SIMULATED FREQUENCY RESPONSES OF THE NONLINEAR GYRATOR TANK

Since the amplifiers, forming the gyrator, are nonlinear, time domain analysis should be used for obtaining their frequency characteristics. The small-signal resonance frequency of the gyrator tank is chosen as to be 800kHz in every simulation. A sinusoidal voltage source with amplitude V_{im} is applied at the input and the maximum of the output voltage V_{om} is determined by time-domain analysis. The gain in dB for the frequency of the source is calculated as $20\log_{10}(V_{om}/V_{im})$. The frequency of the source is varied from 600kHz to 1MHz with step 1kHz and at each frequency is calculated the gain – in this way is obtained the large signal frequency response at the corresponding input amplitude.

The OTAs g_{m1} and g_{m2} are considered as nonlinear ideal VCCS, which dependencies $i_o(v_i)$ are given by the approximating polynomials received in the previous section. Both amplifiers are assumed with identical V-I characteristics. This approach allows to focus on the influence of the nonlinearity of the g_m only. It also avoids the problems with adjusting the DC voltages at the points of connection of the amplifiers, which could misbalance their V-I characteristics.

The capacitors C_1 and C_2 are equal and their values are calculated from formula (2) in order to have 800kHz pole frequency, taking the transconductances g_{m1} and g_{m2} equal to the coefficient α_1 of the approximation polynomial. In order to evaluate the effect of nonlinearities at different Q-factors the simulations are done for $Q = 4, 10, 25$. Its value is adjusted by proper choice of the resistor R in Fig. 2, changing correspondingly the value of g_{m0} to keep $h = 1$.
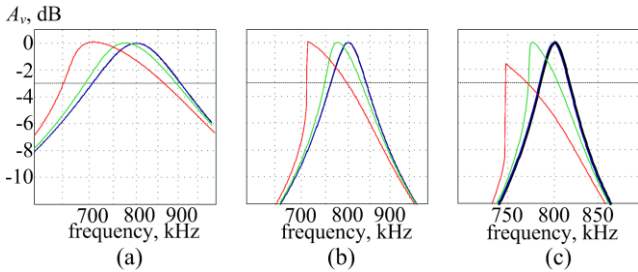

Fig. 5. Frequency responses of the gyrator tank having amplifiers without linearization (Fig. 3(a)). Colours: black – small signal (AC), blue – $V_{im} = 10$mV, green – $V_{im} = 50$mV, red – $V_{im} = 100$mV. (a) $Q = 4$; (b) $Q = 10$; (c) $Q = 25$.

The linear frequency responses, received by AC analysis under the assumption of linear amplifiers, are the ideal case and they are used as reference for evaluation the changes of the other frequency responses due to nonlinearities. For this purpose the corresponding AC frequency responses are added in every figure with black colour.

The results for gyrator resonance circuit having amplifiers without linearization are shown in Fig. 5. When the input signal is small – 10mV, THD of the amplifiers is small (~0.3% according Fig. 4(b)) and corresponding curves practically overlap the AC characteristics, i.e. the tank is still linear. Higher input amplitudes change the frequency response and

its deviation is already visible when $V_{im} = 50$mV (1% THD of the amplifiers).

Fig. 6. Frequency responses of the gyrator tank with $Q = 10$ and amplifiers with linearization. Colours: black – small signal (AC), blue – $V_{im} = 100$mV, green – $V_{im} = 200$mV, magenta – $V_{im} = 250$mV, red – $V_{im} = 300$mV. (a) Amplifiers with $a = 1.5$; (b) amplifiers with $a = 2$; (c) amplifiers with $a = 2.5$; (d) amplifiers with $a = 3$.
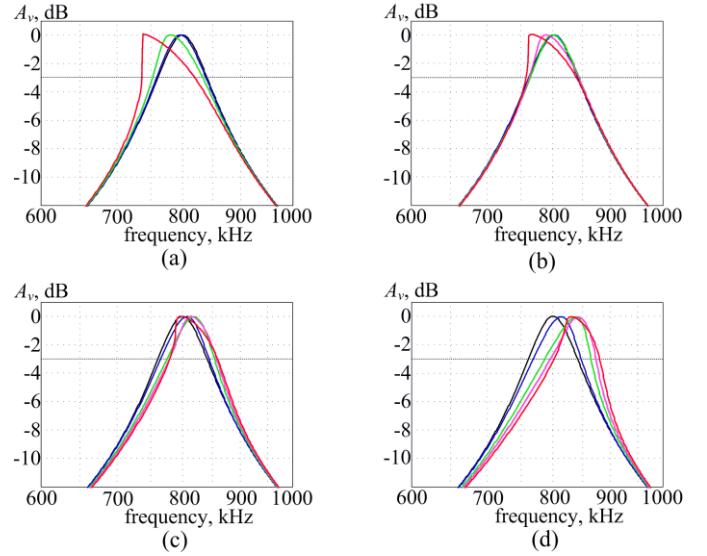

Fig. 7. Frequency responses of the gyrator tank with $Q = 4$ and amplifiers with linearization. Colours: black – small signal (AC), blue – $V_{im} = 100$mV, green – $V_{im} = 200$mV, red – $V_{im} = 300$mV. (a) Amplifiers with $a = 1.5$; (b) amplifiers with $a = 3$.

The use of linearized amplifier in Fig. 3(b) as gyrator OTAs suggests more variants, since the OTA linearity can be controlled by the parameter a. Fig. 6 shows the family of frequency responses when $Q = 10$ and $a = 1.5, 2, 2.5, 3$ (the same values of a as in Fig. 4). Similar families when $Q = 4$ and $Q = 25$ are given in Fig. 7 and Fig. 8 correspondingly.

Several observations can be done from the simulations:

1) The OTA nonlinearities affect the filter frequency response basically around the resonance frequency. The change of the out of band suppression, especially when the attenuation is above 10 dB, is not large.

2) When the amplitude increases enough, the distorting of the frequency response is large and its maximum drops down significantly below the theoretical value of 0dB – e.g. the red curves in Figures 5(c), 8(a) and 8(b).

3) Most of the frequency responses move to lower frequencies when the signal increases. However some of the curves when the parameter a is 2.5 or 3 move upward. This depends

on the curvature of the function $i_o(v_{in})$, which is represented by its derivative di_o/dv_{in}, shown in Fig. 9(a). When this derivative increases the frequency response moves upward; when it decreases the motion is opposite.
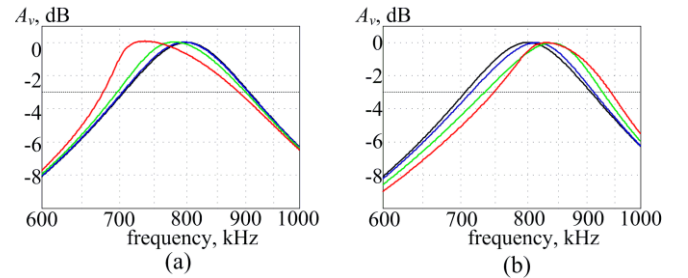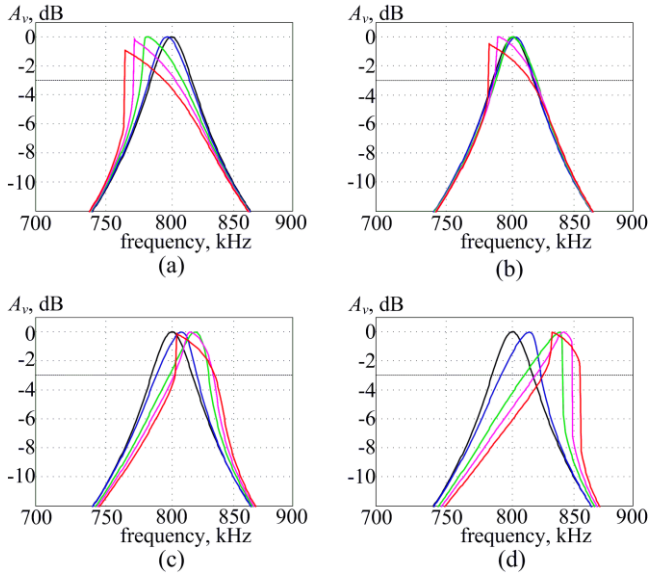

Fig. 8. Frequency responses of the gyrator tank with $Q = 25$ and amplifiers with linearization. Colours: black – small signal (AC), blue – $V_{im} = 100$mV, green – $V_{im} = 200$mV, red – $V_{im} = 300$mV. (a) Amplifiers with $a = 1.5$; (b) amplifiers with $a = 2$; (c) amplifiers with $a = 2.5$; (d) amplifiers with $a = 3$.
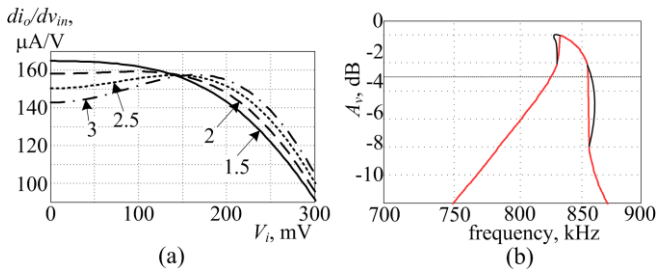

Fig. 9. (a) Dependence of the derivative di_o/dv_{in} from the input voltage of the amplifier in Fig. 3(b); (b) double inclining of the frequency response for $Q = 25$, $a = 3$, 300mV input signal.

4) The change of the resonance frequency has very small dependence from the Q factor if there is no jump in the response. For example when $a = 2.5$ and the input signal is 200mV, the maxima are at 816, 818, and 818kHz when $Q = 4$, 10 and 25 correspondingly. However the narrow bandwidth, when Q is high, makes the circuit more sensitive to the OTA nonlinearity.

5) An interesting case is the red curve in Fig. 8(d), corresponding to $a = 3$ and 300mV input signal – it has two jumps. The large input signal covers areas, in which the differential g_m first increases and after that decreases (Fig. 9(a)). This causes double inclining in the frequency response, shown with black lines in Fig. 9(b).

6) The curves shows that in the gyrator tank THD in the amplifiers above 0.5-0.6% cause undesired changes in its frequency response. However this is not strict limit and it can vary depending on the Q, area of application and type of OTA nonlinearity.

IV. CONCLUSIONS

A gyrator bandpass filters based of fully differential OTAs is investigated by computer simulation concerning the influence of OTA nonlinearity. The collected frequency responses allow to estimate a limit for THD of the amplifiers to 0.5% approximately when $Q < 10$-15. Then the resonance frequency changes by no more than 2-3% and the change of the frequency response is acceptable. It is observed also double inclining of the frequency response in some case – another interesting effects due to nonlinearity of amplifiers

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Problems and Properties of a Current Amplifier When Realized in Ultra Deep Sub-micron Technology

Simeon Kostadinov[1], Ivan Uzunov[2], Dobromir Gaydazhiev[3]

Abstract – **In this paper are described three versions of a current amplifier and each of them is realized with FETs having different channel length: 90nm, 45nm and 30 nm. Their basic properties are simulated and discussed, demonstrating the major benefit of the shortening of the channel length – extension of the frequency bandwidth. The problems arising with the shorter channels length are also considered briefly.**

Keywords – **amplifiers, current mode operation, short-channel effects, MOSFET.**

I. INTRODUCTION

The scaling of the semiconductor devices in modern CMOS technology improves the performance, lowers the price and reduces the power supply of the fabricated circuits [1,2]. While device downscaling is driven primarily by the benefits it has in digital design, it introduces new effects in transistor behavior, which makes analog design challenging. As channel lengths decrease below 1μm, second order effects, which were not taken into account for long channel FETs must be accounted for. When short channel effects become significant the traditional analytic approach in analog design is not feasible [3]. This necessitates a modification of the existing analytic design methodologies and employment of new techniques.

Shrinking the gate length is accompanied by decrease in power supply voltage, which is a major issue in analog design. However threshold voltage does not scale as much as the supply voltage, and transistors are biased at lower voltages, which results in worse transistor properties [1,4].

Current mode operation overcomes some of the problems with downscaling because it requires lower supply voltage compared to its voltage mode counterparts [4,5]. It also has some other advantages – at low power supply voltage they allow wider signal dynamic range, wider frequency bandwidth, better linearity. For these reasons, current mode designs become very popular in many high performance analog and mixed signal applications – RF front ends, data converters, oscillators, etc.

The legacy design methodology applicable for long channel devices uses theoretical circuit analysis based on expressions taking into account only first order effects. In contrast,

designing an amplifier in sub-micron technology must include the higher order effects, rendering a purely analytical approach no longer viable, since it leads to significant inaccuracies mainly related to the specific short channel effects – drain induced barrier lowering, channel length modulation, velocity saturation [1,3,4]. Even some technology specific parameters, e.g. μC_{ox}, are not constant anymore and depend on transistor geometry.

A method for design of a basic current amplifier, when short channel effects are significant is proposed in [6]. For the cases when short channel effects are moderate the design procedure gives very good matching between specification and simulation results. Further reduction of device sizes causes more and more deviation from the basic theory. The goal of this paper is investigation of these effects when the sizes approach the technology defined limits. A basic current amplifier is designed with different FET devices with different channel lengths: 90nm, 45nm, 30nm.

II. BRIEF REVIEW OF THE DESIGN METHOD

The circuit of a basic current amplifier is shown in Fig.1. The major problem in its design is the requirement of identical transconductances of M_1 and M_3 at the same drain currents. This is necessary in order to keep the symmetry in upper and lower halves of the circuit. The formulas for long channel device transconductance and drain current are [2,5]:

$$g_m = \mu C_{ox} \frac{W}{L} V_{ov}; \; I_D = \frac{\mu C_{ox}}{2} \frac{W}{L} V_{ov}^2 (1 + \lambda V_{DS}), \qquad (1)$$

where μ is the carrier mobility, C_{ox} is gate capacitance per unit area, W and L are channel width and length, V_{ov} is overdrive voltage and V_{DS} is drain-source voltage of the transistor. The widths of M_1 and M_3 should be connected with the n- and p-carriers mobilities by the relationship $W_1/W_3 = \mu_p/\mu_n$ in order to have equal g_m's of these transistors [6]. It follows from (1) and is valid for long-channel transistors only.
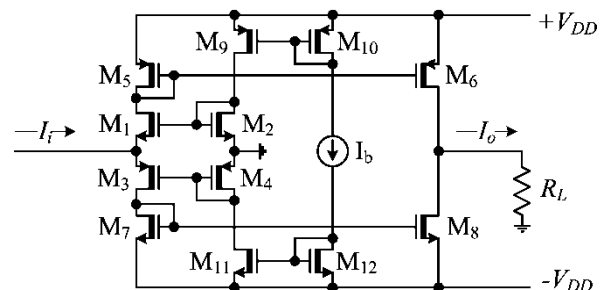
Fig.1. The circuit of the current amplifier

The above mentioned reasons do not allow to implement this relationship for short channel transistors. The design

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procedure proposed in [6] uses a graphical and analytical approach for initial design centering and then refining the device dimensions by parametric simulation. Firstly the dependences of g_m/W and I_D/W from gate-source voltage for PFET and NFET are plotted [2]. Short channel effects make these normalized curves slightly different. However the differences are small and will be compensated in the following optimization. The next steps are:

Fig.2. Plots of normalized g_m and I_D vs. V_{GS}: (a) NMOS; (b) PMOS.

1) The transconductance of the input transistors are defined by the input impedance:
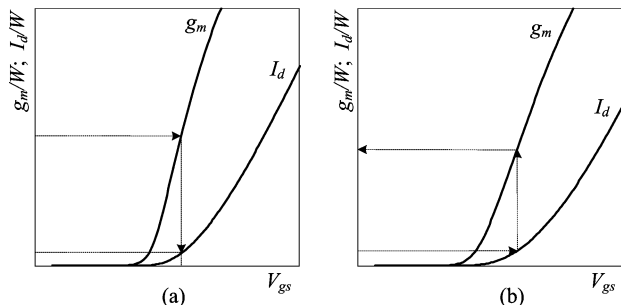
$$g_m = g_{m1} = g_{m3} = \frac{1}{2.2R_i} \qquad (2)$$

A normalized value of g_m for NMOS is chosen in the linear region of the curve (Fig. 2(a)). The width of the transistor can be determined by dividing the desired transconductance by the chosen value.

2) The normalized g_{m1} defines V_{GS} and the corresponding normalized value of I_{D1} of M_1. Since the width of M_1 is already known the required drain current of M_1 can be calculated.

3) The drain currents for M_1 and M_3 must be the same and equal to the total input branch current $- I_{D1} = I_{D3} = I_D$. Looking at Fig. 2(b) we pick a value I_{D3}/W in the region where drain current is a quadratic function of V_{GS}. This value also defines the V_{GS} and the width of M_3.

4) For the selected value of I_{D3}/W it should be verified that the corresponding g_m/W is in the linear region in Fig. 2(b). If it is not, another value of I_D/W should be chosen.

5) These steps do not guarantee the exact matching of g_{m1} and g_{m3} since the transistors are of different types. The received values will be used as initial for the following optimization based on parametric analysis, in which the values of g_{m1} and g_{m3} are equalized at the same drain current.

III. PROBLEMS ARISING WITH DEVICE DOWNSCALING

To study the changes in the amplifier parameters and behavior, it is designed in 32nm bulk CMOS technology, developed for SRAM, logic and mixed-signal applications. Three versions of the amplifier are considered: 1) realized with hpar FETs with gate length of 90nm; 2) realized with slvt FETs with gate length of 45nm; and 3) realized with slvt FETs with gate length of 30nm (the minimum allowed drawn gate length for thin oxide in the used 32nm technology). The abbreviations hpar and slvt are for different types of MOS

transistors in the Process Design Kit [7]. All three version are supposed to meet the following specifications:

- input impedance $R_i < 500\Omega$;
- power supply $V_{DD} = \pm 1V$;
- current gain A_i equal to 1, i.e. current buffer.

The design is based on the procedure outlined in the previous section. All transistors are working in strong inversion in saturation and the corresponding DC branch currents are listed in Table 1.

TABLE I
DC CURRENTS IN THE AMPLIFIER BRANCHES

Current in µA through	I_b	M_5, M_1, M_3, M_7	M_9, M_2, M_4, M_{11}	M_6, M_8
Version 1	74	72.6	73.2	98.4
Version 2	93	79.3	85.7	121.5
Version 3	115	97.6	105.4	186

Several problems were faced during the design:

1) Due to channel length modulation the current mirrors ratios depend strongly on the drain-source voltage. Then the current gain deviates from the ratio of the areas M_5/M_6 and M_7/M_8 (the theoretical value of the gain). For example, if these transistors have equal areas, the gain for Version 1 is 1.18, for Version 2 it is 1.25, and for Version 3 it is 1.3. An accurate value of current gain can be achieved by varying the channel widths with parametric analysis.

2) Decreasing the channel length relatively reduces the back-gate transconductance g_{mb} concerning the main transconductance g_m. In [6] g_{mb} is estimated as more than 10% of g_m and its contribution is reflected in formula (2) by the factor 2.2. For shorter channels g_{mb}/g_m is less than 5% and this factor should be reduced to 2.1 or even 2.

3) The threshold voltage V_{th}, which is usually considered to be constant, in fact depends on the drain-source voltage V_{ds} due to drain induced barrier lowering (DIBL effect). This is a common short channel effect in FETs. The variation of the threshold voltage is investigated by simulation for the used transistors and the corresponding plots are shown in Fig.3.
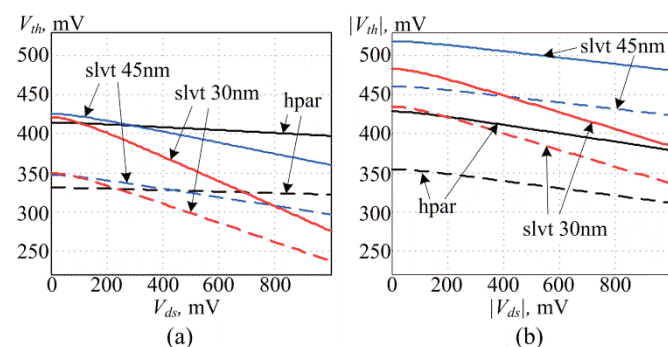
Fig. 3. Dependence of the threshold voltage from the drain-source voltage for the transistors of interest. Solid lines - with bulk effect, dashed lines - without bulk effects: (a) NMOS; (b) PMOS.

Several effects are observed in Fig.3. As expected, shorter channels have greater dependence of V_{th} on V_{ds}. Transistor type hpar is optimized for analog applications, which results in negligible difference of threshold voltages for PFET and

NFET and their deviation with V_{ds}. This is not the case for slvt FETs, which are basically intended for use in digital circuits – V_{th} has stronger dependence on V_{ds} and the difference between V_{th} of PFET and NFET is more than 20%. However overcoming the challenges in amplifier design based on slvt FETs proposes some significant benefits – small die area and operation at higher frequencies.

4) The breakdown voltages for the used transistors are low (1V) for all three types. On the other hand, threshold voltages are relatively high – up to 0.5V, while the circuit has four transistors in series in most of the branches. Both circumstances require operating at a total supply voltage, which is more than the limits of the transistors and here ±1V is used. To guarantee the safe operation it is necessary to check the voltages over transistors at different input current. The limits for the magnitude of the input currents are defined with the following procedure: a DC current source is applied at the input and its current is varied from -3mA to 3mA with DC sweep analysis. The plots of the voltages, which exceed the limits, are given on Fig. 4 for amplifiers with hpar and slvt 45nm. The corresponding plots for slvt 30nm are very similar to slvt 45nm and they are not shown. The maximum input current I_{imax} determined from the figure are: 1.2mA for Version 1 (hpar), and 1mA for Versions 2 and 3 (slvt).
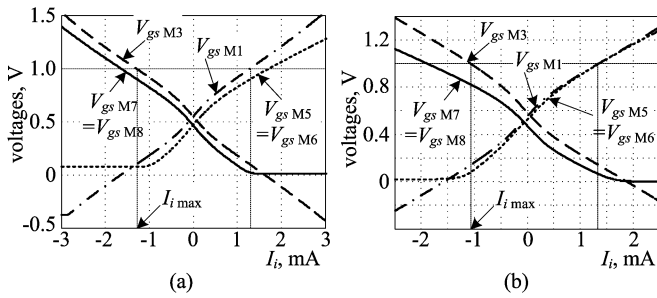
Fig. 4 Gate-source voltages, which exceed the safe operation range: (a) amplifier with hpar FETs, (b) amplifier with slvt 45nm FETs.

IV. SIMULATIONS OF THE BASIC AMPLIFIER PARAMETERS

The three versions of the amplifier are compared by several basic parameters: small and large signal current gain, input impedance, and transfer characteristic (I_o vs. I_i) and THD. The small signal parameters are shown in Fig. 5. The current gain is different for the three versions for reasons commented above. More interesting are the frequency bandwidths. The corners frequencies are: 12.03 GHz for Version 1, 25.6 GHz for Version 2 and 45.9 GHz for Version 3. For comparison, the same amplifier designed with another type of MOSFETs from the same technology – zgfets with 270nm minimum gate length [6] has corner frequency of 2.3GHz. The benefit of using short channel transistors is obvious. The input impedance is close to the designed and it keeps its value up to few GHz.

The large signal behavior is illustrated in Fig. 6. They are obtained by parametric time domain analyses using sinusoidal input current source with parameterized amplitude. Its frequency is fixed at 10 KHz - low enough to avoid slew rate

effects and suppression of the harmonics, generated in the amplifier, from its frequency response.
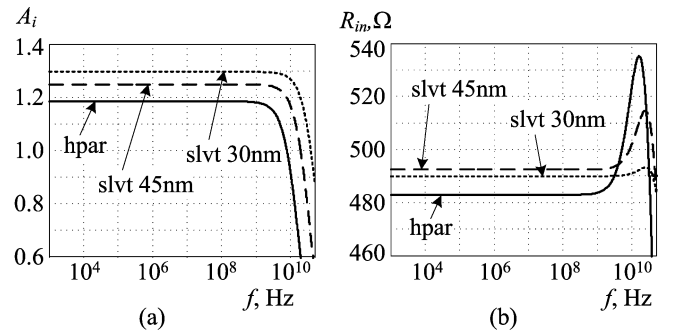
Fig. 5 Small signal characteristics of the designed amplifiers: (a) current gain; (b) input impedance.

The dependence of the amplitude of the output current from the amplitude of the input current is shown in Fig. 6(a). The curves are very close to each other due to the approximately equal current gains of all three versions and it is difficult to distinguish them. For this reason two other characteristics are added: large signal current gain $A_i=I_o/I_i$ and the THD, both as functions of the input amplitude. These characteristics show that the decreasing of the channel length increases the nonlinearity. Evidently this is the price for the extended frequency bandwidth. However, the amplifier with hpar transistors has similar THD as the amplifier with three times longer (270nm) zgfet transistors, which has 1.7% THD at I_i=1mA [6].

Fig. 6 Dependences of large signal parameters of the designed amplifiers from the input current: (a) output current; (b) large signal current gain; (c) THD.

V. Conclusion

One of the most common current amplifiers is designed with three different types of deep submicron MOSFETs from a 32nm CMOS technology: 90nm hparfet, 45nm and 30nm slvtfet. The major benefit of short 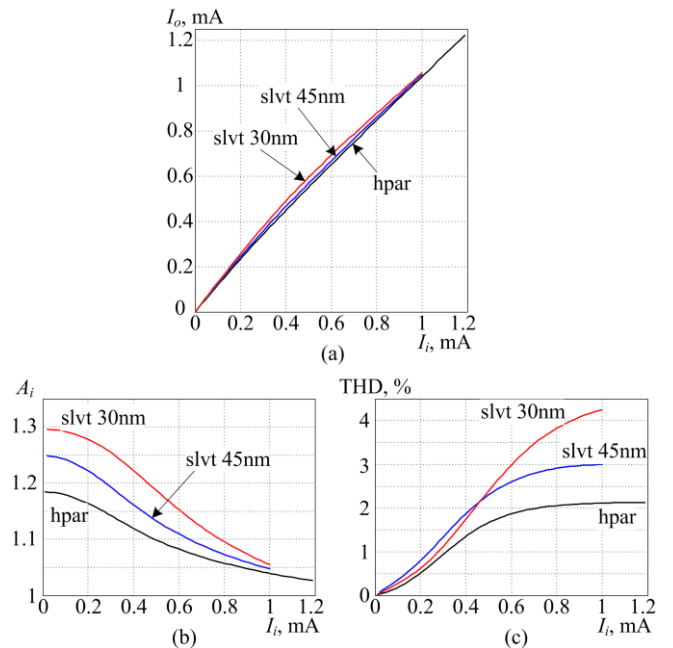channel transistors is significant extension of the frequency bandwidth – up to 45 GHz for the circuit with shortest channel transistors. The large signal behavior is also investigated and the hpar version of the circuit shows similar non-linearity compared to the same circuit with much longer transistors. Certain increase of the non-linearity is observed for the versions with shorter channel transistors (slvtfets). The maximum amplitude of the input current is lower due to the reduced operating voltages of the used transistors, but this limitation can be relaxed by using wider FETs and higher biasing current.

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Optimization and analysis ALL Digital PLL
For resonant inverter

Goran Goranov [1], Nikolay Madzharov [2]

Abstract – **The purpose of this article is to determine the optimal ALL digital PLL for control resonant inverters. Various methods of synthesis of the digital frequency are examined and compared. On the base of the results we determine which control approach is applicable. Phase detector, loop filter and digital controlled oscillator realized in programmable logic are used.**

Keywords – **Logic gates, Control system, PLL, CPLD.**

I. INTRODUCTION

The widespread use of transistor converters in various areas of practice - industry, medicine, service sector etc., imposes the new requirements to the control systems related with regulation and maintenance of certain operating modes. The implementation of the PLL functions into control systems for power converters and their investigation are presented in details in [1], [2], [3]. The use of programmable logic devices allows for the development of such systems by expanding their functionality and adaptability.

The optimization and analysis on this digital PLL gives us opportunities to work in a relatively wide frequency range and small steps for adjustment. This is also and an easy connection to other digital systems. The digitally frequency synthesis is based on programmable divide a quartz stabilized frequency to obtain a change of the output frequency in a certain range and a predetermined step. There are various methods for digital frequency synthesis - a divisor of N, direct digital synthesis (DDS), I/D - counter, fractional N, division by comparison schemes, etc. They are hardly realizable in a discrete implementation [4], [5], [6].

The analysis of digital PLL is limited to the examination of each module separately - Fig.1.

In the previous studies and researches of the author feasibility of a digital PLL, using I/D - counter and FRACTIONAL N method are affected. The conclusion is that various digital controlled generators require a substantial change in the functions of the previous blocks in the digital PLL. Often this refers to the digital filter, which is connected to the generator. Phase detector in most of the cases does not change unless you change monitoring requirements for the phase difference. Figure 1 shows a digital PLL, comprising a phase detector DPD, converting the phase difference into a signal of a specified duration, the digital filter DLF, converting the signal from the phase detector and the digital controlled oscillator DCO. In operation of the system, frequency *Fout* of the output signal of the DCO seeks to achieve input frequency *Fin* with certain accuracy. The change of the input frequency *Fin* generates an increase or decrease of the phase difference between it and the output frequency *Fout*, which leads to their alignment (*Fin = Fout*).
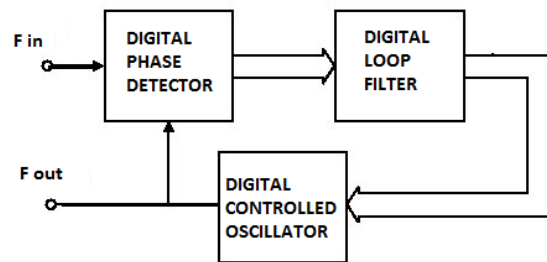
Fig. 1. ALL digital PLL

II. SYNTHESIS OF THE BASIC MODULES

Phase detector.

The most felicitous for use from the three main types of phase detectors (XOR, JK-Flip Flop and frequency phase detector) in the management scheme of the resonance inverters is the frequency phase detector. This is a detector with three states, managed by the front of the input signal. The range is $\pm\,360\,°$. From the timing diagram shown in Figure 2 we can see the advantage of the phase frequency detector. In phase difference $\varphi = 0$ signals UP and DN are also zero. Depends on the direction of the phase shift, in one of the two outputs, is obtained the pulse Кз, proportional to the phase difference.
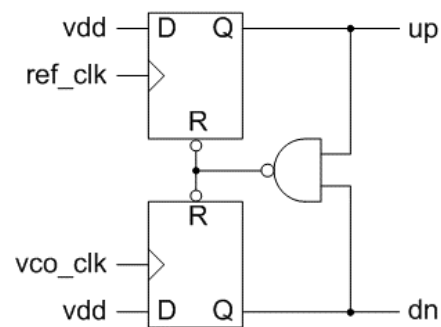
Fig. 2 a)

Fig. 2 б)

Digital controlled oscillator

FRACTIONAL - N

The block diagram representing the method consists of two main blocks for division of an integer and a fractional part - Fig. 3

Fig.3. Basic Fractional-N.

The input clock frequency f_i is used. Part of the pulses is removed in reducing impulses block. The number of the removed pulses is proportional to the ratio N, issued by the block of t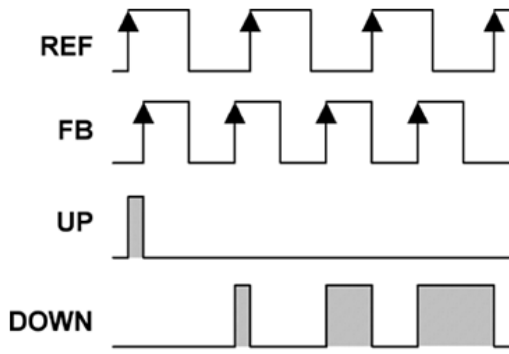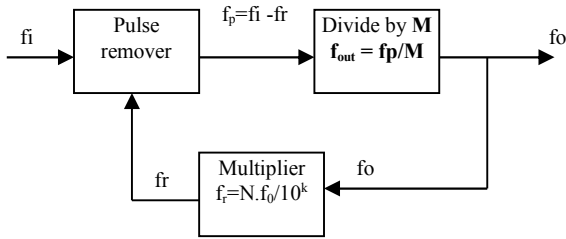he multiplier. The removal of the phase noise (asymmetry between successive pulses) is achieved most easily as "blur" in time. The division factor M is used, which is an integer - block divider of M. The output frequency is calculated by the following formula:

$$f_{out} = \frac{f_p}{M} = \frac{f_i - f_r}{M} = \frac{f_i - \frac{N.f_{out}}{10^k}}{M} \ , \tag{1}$$

from where

$$f_{out} = \frac{f_i}{M + \frac{N}{10^k}}, \tag{2}$$

$$f_{out} = \frac{f_i}{M + \frac{N}{10^k}} - \frac{f_i}{M + \frac{N-1}{10^k}}, \tag{3}$$

In the presented formulas M is an integer, K is number of decades, and N is an integer in the range of 0 to $10^к - 1$. On this basis, for the realization of FRACTIONAL - N method are needed binary decimal counters for M divider and multiplier for divisor N. If the coefficient of division M varied from 0 to 9, you will need a counter with two digits of M i.e. an amendment from 0 to 99, respectively, two counters and etc. The same goes and for the divisor N, which determines the fractional part. For example in the number of decade K=2 is obtained by dividing the frequency 1,00 to 99,99 .

The implementation of the digital Fractional-N divider for management of the resonant inverter has the following advantages and disadvantages:

➢ Works in a wide frequency range.
➢ Receives relatively low phase noise and hence little impact on the optimal operation of the power transistor converters.
➢ Easy to implement coordinating digital filter

Disadvantages:

➢ Nonlinear step of modifying the frequency - depending on the divisor.
➢ Receives relatively low phase noise and hence little impact on the optimal operation of the power transistor converters.

DDS – generator

DDS – generator is a type of generators, which is driven by a digital code (word), called the DCO. It works with digital converter filter time-digit code. On Fig. 4 is shown the block structure of this type of frequency synthesis.

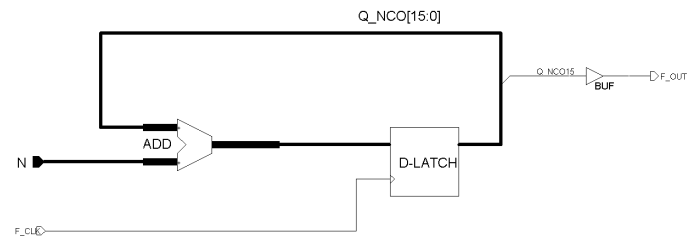*Fig. 4. DCO.*

The output frequency is given by:

$$f_{out} = f_{clk} \ . \ N/2^k \tag{4}$$

where 2^k is the sparsity of the ADD.

The amendment of f_{out} varies from 0 [Hz] to $f_{clk}/2$ [Hz] with step:

$$\Delta f_{out} = f_{clk} /2^k \tag{5}$$

Advantages and disadvantages of using DDS method for managing resonant inverters are:

➢ Working in a wide frequency range max ½ fin.
➢ A very small step of frequency variation -Δf.
➢ Easy to implement digital matched filter.

Disadvantages:

➢ The main disadvantage is the phase noise, its value reaches *1/f,* at *fout=1/2fin.*
➢ Requires large program capacity.

Increment/decrement counter

This is a bias scaler, whose amendment is managed by two entrances carry and borrow - fig.5.
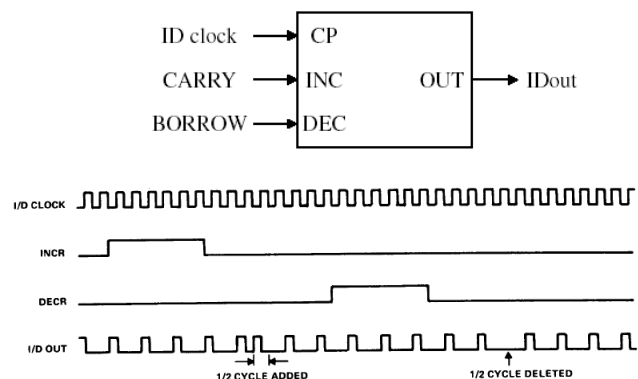
Fig. 5. I/D – counter and timing diagram

The resulting output frequency (I/Dout) of I/D counter – is ½ I/Dclk. It may be amended "up" or "down" depending on which input is received 1-0 transition. The amendment is obtained by adding or deleting ½ cycle. To reduce the phase noise can be used an additional counter (divisor N), then phase noise will be reduced by 1/N.

Advantages and disadvantages in using this method are:

➢ Relatively small step of frequency variation -Δf (tens of Hz).
➢ Small phase.

Disadvantages:

➢ Complex to implement digital filter
➢ Limited range of frequency variation
➢ Dependence on many parameters.

Loop filters.

The task of the filters is to convert the signal so that it is convenient to control the synthesized oscillator. Depending on the digital synthesized adjustable generator are used various filters. If the used generator is I/D – counter, then a filter that converts the signal phase difference from the phase detector in the number of pulses is needed. Thus plays the role of an integrator [8]. Such a filter can be realized by a reversible counter with an adjustable division ratio, called K-counter - Fig. 6. The principle is explained with tim diagrams shown in Fig. 7. The number of output pulses (transfers) is proportional to the operating time of the respective counter UP or DOWN, respectively, and the phase difference.
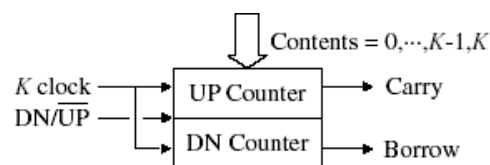
Fig. 6. Programmable frequency divider of K - counter.
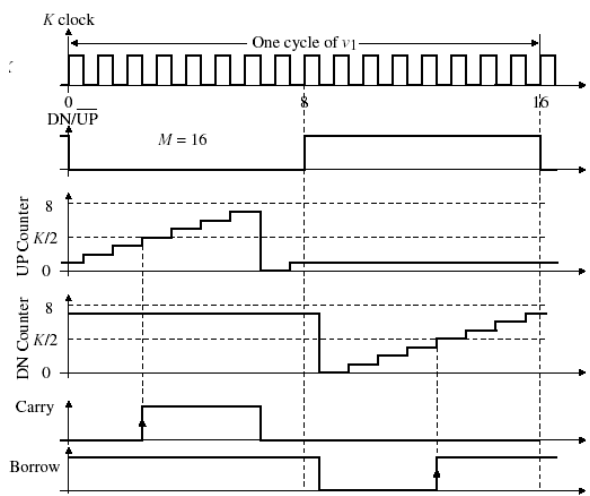
Fig. 7. Time chart of K – counter.

Another type of filter is converter of time into a digital code. The resulting code (word) N directly operates the generator - DDS or Fraction-N, changing its output frequency proportional to the code N. The condition for synthesis of the converter is $f_{clk} \gg$ EVENT
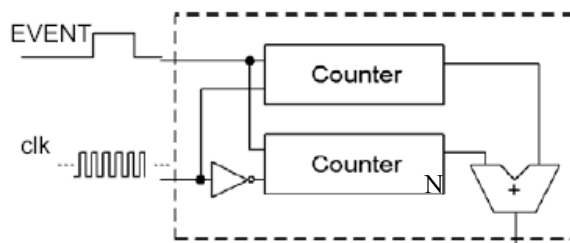
Fig. 8. Converter time numerical code.
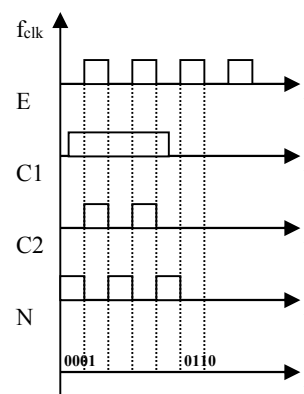
Fig. 9. Time chart of converter - time in numerical code.

Between the considered options are development and synthesized PLL scheme with DDS generator and filter T2C (time to code converter) in CPLD Xilinx CoolRunner2.

The experimental object for management is a transistor half-bridge parallel inverter, which is running with frequency above the resonance one. The input power of the converter is P = 1,6 kW. Load capacitance value is C = 1,72 μF. It is implemented with non-inductive capacitors. The load inductance - the inductor has a value L = 3,1 μH, wound copper tube with a diameter of 9 mm with 13 windings. The diameter of the inductor is 73 mm.

A study of system performance under different input power and loads has been made. On Fig. 10 a) is shown the current and voltage in resonance at low load and input voltage E = 130V and input current I = 12,3A. On the channel one of the oscilloscope is visualized the form of the current and on the channel two the form of the voltage. Both signals were observed after the transformers for feedback. It can be seen that the mode of the inverter is good, when the frequency is maintained by digital PLL. The increase of the input voltage leads to bigger power load. This will lead to its heat and therefore to change the parameters of the circle and therefore the frequency will start to decrease.
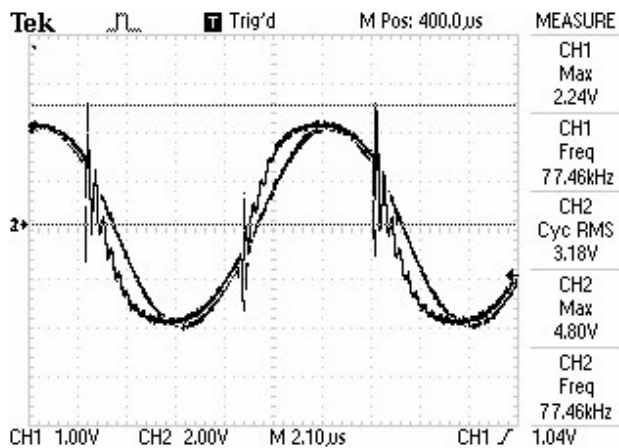
Fig. 10 - A) Voltage on the parallel circuit and the current - hollow material.
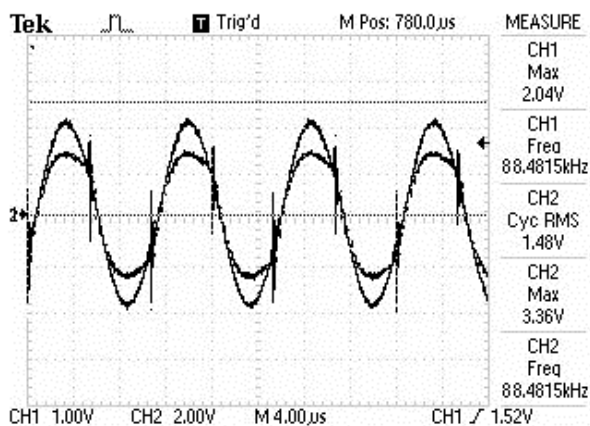
Fig. 10 - B) Voltage on the parallel circuit and the current - dense material.

At higher load (when solid material is used), the operating frequency is changed on 88,48 kHz - Fig. 10 b). Input voltage E = 122V, I = 10,7 A.

III. CONCLUSION

The analysis shows that the best results are achieved when synthesized management scheme with 16bit DDS generator is used. A 16 bit counter for filter, which converters signal from the phase detector is realized. The response time of the system as a whole depends on the sparsity of the filter and the time of integration. Time integration is proportional to the signal EVENT - phase difference. Under the process of locking frequency (resonance inverter) phase deviation is small and therefore the reaction has several clock cycles. Great importance has the supporting clocked. Although the inverter operates at frequencies from 60 to 100 kHz by using 50MHz reference frequency. Thus the influence of phase noise is minimized.

Good results are achieved also when I/D counter is used, but the digital filter is more complex and requires more programmable logic resources.

Using methods for fully digital control improved adaptability to any electronic system, provide much easier monitoring of parameters and setting of such microcontrollers.

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Design and Realization of a 12W Quasi-Resonant Flyback Converter

Zoran Zivanovic[1] and Vladimir Smiljakovic[2]

Abstract – **In this paper the design of a quasi-resonant flyback converter is presented. The operating principles are briefly explained, including the functional block diagram. The prototype has been built and experimental results are presented to support the theoretical analysis and to demonstrate the converter performance.**

Keywords – **CCM, DCM, Flyback, EMI, Quasi-resonant**

I. INTRODUCTION

The most widely used isolated switch mode power supply topology is the flyback converter. Power levels are in low to mid power range, from 1 W to 50 W or even 100 W for low current outputs. The single magnetic component is actually not a transformer but a coupled inductor that combines functions of energy storage, energy transfer and isolation. The main advantages are wide input voltage range, with multiple outputs, higher or lower than the input voltage and simplicity. Depending on the design of the coupled inductor the flyback converter can operate either in Continuous Conduction Mode (CCM) or Discontinuous Conduction Mode (DCM). However flybacks are not perfect. Major drawbacks are poor magnetics utilization and higher electromagnetic interference as a result of hard switching with high peak currents.

II. QR FLYBACK CONVERTER BASICS

A quasi-resonant converter is a distant cousin of a resonant converter. However, the waveforms are not sinusoidal like at true resonant converter, in fact they have typical flyback shape. Also QR flyback power stage does not seem any different from a classical DCM flyback. The "quasi-resonance" is effective in the dead time after the core is demagnetized. The switching occurs at the valley of the resonant ringing generated by the circuit parasitics. There is no need to add inductors and capacitors because they are already there. Soft switching results in switching loss reduction because turning the MOSFET on at the valley of the resonant ringing lowers the losses associated with the output parasitic capacitance of the MOSFET. Another advantage is a reduction of conducted and radiated electromagnetic interference. Also the jitter that results from searching for valley of the ringing spreads the frequency spectrum reducing

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electromagnetic interference.

The QR flyback converter must operate in DCM because the core must be completely demagnetized. A specialized controller detects core demagnetization and resonant valley and initiates next turn on cycle. In a conventional flyback the constant frequency oscillator initiates the next turn on cycle, so turn on can be at any point of the resonant ringing. QR controllers rely on the switching waveform for valley detection, by detecting the change in slope or a zero-crossing threshold. Some controllers modulate both the switching frequency and the primary current over the most operating range and the others modulate the switching frequency but maintain a constant peak primary current over the most operating range.

The UCC28600 from Texas Instruments (Fig.1) is QR controller operating in different modes, modulating the peak primary current proportional to load and the switching frequency inversely proportional to load.
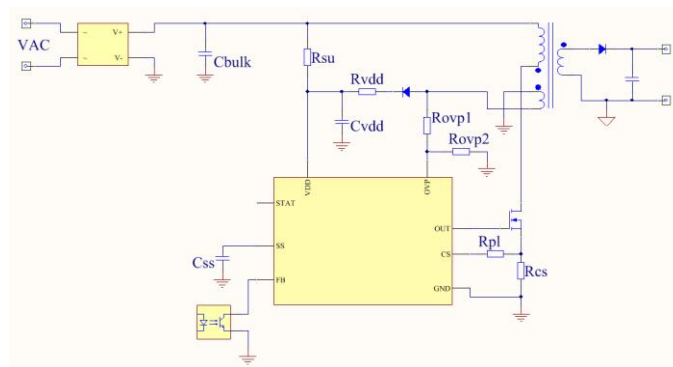
Fig.1. QR flyback converter

For loads below 10 % of rated power the controller will operate in green mode (GM) regulating the output using burst of 40 kHz pulses. The number of pulses increases until the converter is switching consistently at 40 kHz. Frequency foldback mode (FFM) is reserved for loads between 10% and 30% of rated power. The output is regulated by modulating the frequency from 40 kHz to 130 kHz, holding the peak primary current constant. Finally, for higher loads between 30% and 100% of rated power the controller will operate in either DCM, where the peak primary current is modulated but the switching frequency is clamped to maximum (130 kHz), or quasi-resonant mode (QRM), where the peak primary current and the switching frequency are both modulated.

The above boundaries of steady-state operation are approximate because they are specific design dependent. They are programed by the flyback transformer and the four resistors R_{PL}, R_{OVP1}, R_{OVP2} and R_{CS} on the Fig.1.

III. DESIGN AND ANALYSIS

The task is to design a 12 W QR flyback converter using the UCC28600 controller with careful choice of operating parameters and components. The footprint size must be around 80x40mm. Design specifications are given in Table I.

TABLE I
DESIGN SPECIFICATIONS

		Min	Typ	Max	
Input voltage	V_{IN}	160	220	264	V_{AC}
Output voltage 1	V_O		+12		V
Output power	P		12		W
Full load efficiency	η		80		%
Output ripple voltage	V_{RIPPLE}		≤120		mV
Switching frequency	f	40		130	kHz

The transformer (inductor) must be sized at the minimum input voltage, maximum power and between frequency clamps (40 - 130 kHz). Knowing that, a good choice of core for the transformer is E20/10/6, N87 material from TDK. Reinforced insulation is a must, but the effectiveness of which must be verified by dielectric strength testing.

Using a switching frequency of 80 kHz we can now calculate the maximum primary inductance using the following equation

$$L_{P\max} = \left(\frac{V_{DC\min}(V_O + V_F)N \times 0.925T}{V_{DC\min} + N(V_O + V_F)} \right)^2 \left(\frac{f}{2P_{IN\max}} \right) \quad (1)$$

We will use 650V MOSFET so the reflected voltage must be around 100V. If we adopt 110V, we can easily calculate the primary to secondary turn ratio using equation

$$N = \frac{N_P}{N_S} = \frac{V_R}{V_O + V_F} \quad (2)$$

In order to prevent the saturation of the core we must obtain inductance factor to be $A_L = 200nH/T^2$. For that value we need air-gap in center leg to be g = 0.2 mm. Because the grinding of the center leg is problematic, we will place non-conducting spacers between core halves. The spacer thickness should be half the value used for the center leg gap. In our case we have s = 0.1 mm.

Now we can calculate the number of primary turns using equation

$$N_P = \sqrt{\frac{L_P}{A_L}} \quad (3)$$

Skin depth in mm is given by the following equation

$$\delta = \frac{76}{\sqrt{f}} \quad (4)$$

As a result the wire diameter must be

$$d < 2\delta \quad (5)$$

At the end the number of secondary turns is given by

$$N_S = \frac{N_P}{N} \quad (6)$$

The results are given in Table II.

TABLE II
BASIC PARAMETERS

		---	Typ	---	
Max. primary inductance	L_P		1.2		mH
Number of prim. turns	N_P		78		
Number of sec. turns	N_S		9		
Primary peak current	I_{PPEAK}		0.5		A
Primary RMS current	I_{PRMS}		0.2		A
Secondary RMS current	I_{SRMS}		1.6		A
Max. wire diameter	d		0.42		mm

Now it is time to wind the transformer. We will use a single 0.2 mm enamelled copper wire for the primary and a triple-insulated bundle of 7 twisted wires with 0.3mm enamelled copper wires for the secondary, in order to minimize copper losses taking into account the skin effect and to fulfil demands for reinforced insulation. Using triple-insulated wire instead of layers of tape barrier between the windings we will minimize the leakage inductance which must not exceed 4% of the primary inductance. Also to minimize the leakage inductance the bias and secondary winding are interleaved between the primary halves. The bias winding is designed not only to supply the current for the controller, but also to detect the valley of the resonant ringing

Knowing specific core losses we can now calculate the loss in magnetic component (Table III). Total transformer power loss is 0.354 W. Since the thermal resistance of chosen transformer is 46°C/W the temperature rise will be approximately 17°C above ambient temperature. Satisfied with the results, we will keep the chosen core geometry.

TABLE III
TRANSFORMER LOSSES

		---	Typ	---	
Core effect. volume	V_E		1.49		cm^3
Specific core losses	P_V		0.15		W/cm^3
Core loss	P_{CORE}		223		mW
Primary resistance	R_{PRI}		1.73		Ω
Primary loss	P_{PRI}		86		mW
Secondary resistance	R_{SEC}		14		mΩ
Secondary loss	P_{SEC}		46		mW

For the output diode we will use Schottky diode despite much higher junction capacitance which can cause ringing with parasitic inductance. The rated voltage of used diode is 100V in order to accommodate the sum of the reflected

primary voltage and the output voltage including margin for the leakage inductance spike

IV. REALIZATION

AC/DC converter was built on two layer FR-4 substrate with 35µm copper with a footprint of 80x40mm. The transformer is wounded on through-hole coil former according to the calculations. Output voltage is further filtered out by the added LC filter. All electrolytic capacitors are low ESR organic polymer electrolytic capacitors.

Furthermore we have measured efficiency at various loads at various input voltages. For practical reasons we have used input voltages from 250 to $350V_{DC}$. The results are given in Fig.2. The efficiency is over 84% at full load.
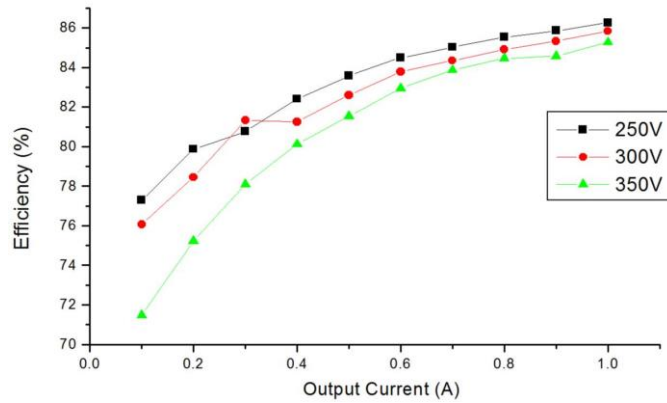
Fig.2. Efficiency as a function of load

The drain waveform of the primary MOSFET in green-mode at 0.1A output load is given in Fig.32. With raising load the converter goes to frequency fold-back mode (Fig.4). At maximum load (1A) the converter operates in quasi-resonant mode (Fig.5). All three waveforms are captured at 300V DC input.
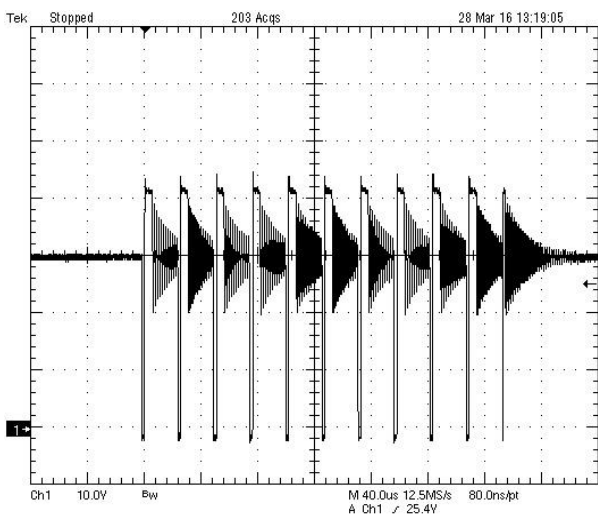
Fig.3. Drain voltage in green-mode (burst)
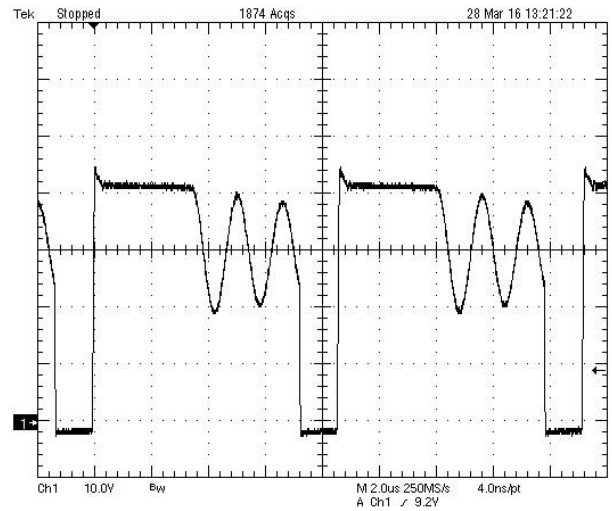
Fig.4. Drain voltage in frequency fold-back mode
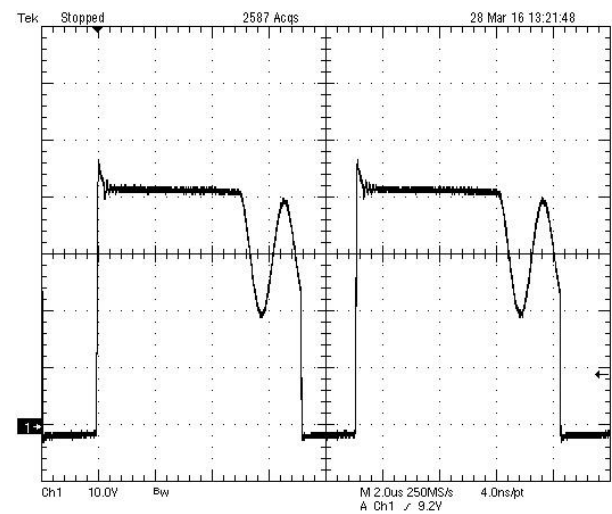
Fig.5. Drain voltage in quasi-resonant mode
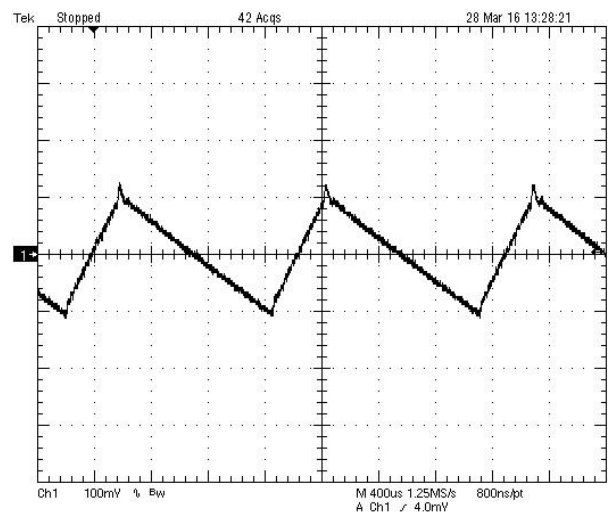
Fig.6. Output ripple in green-mode
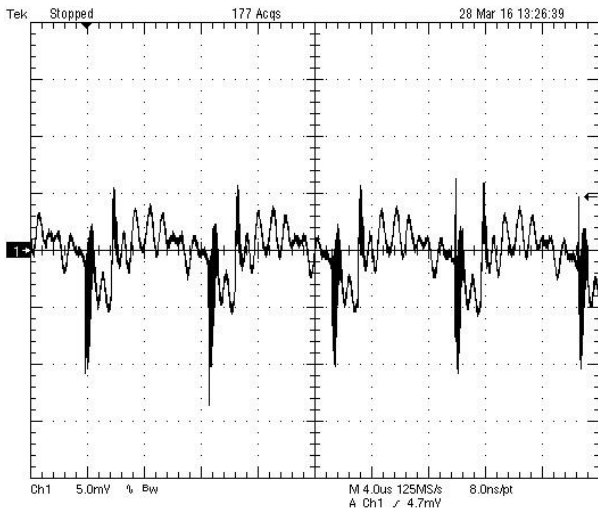
Fig.7. Output ripple in quasi-resonant mode
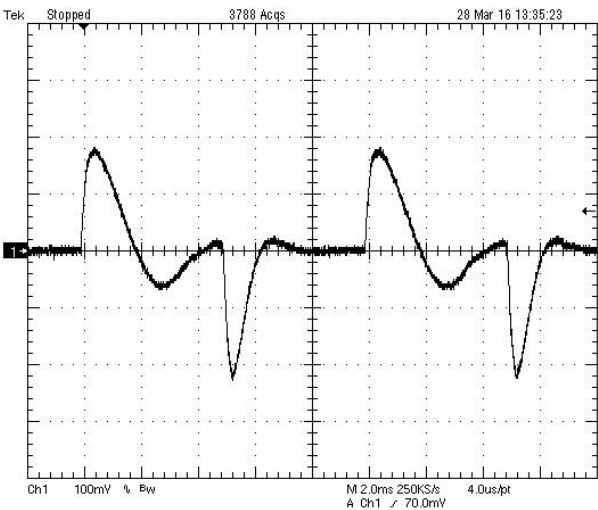
Fig.8. Output voltage load transient response
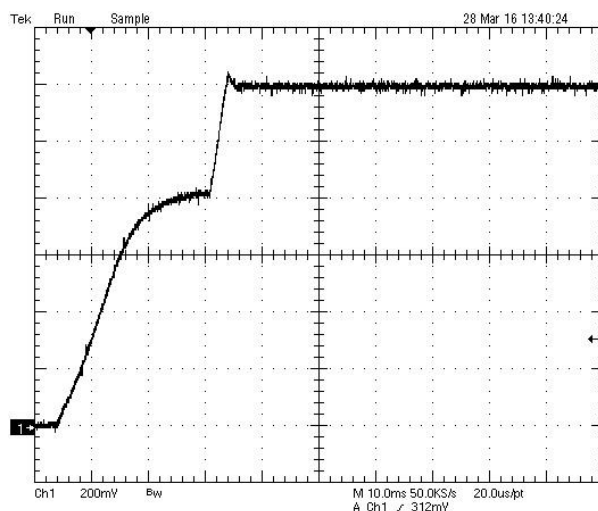
Fig.9. Output voltage rise into 1A load

The output voltage ripple in green-mode is around 230mV$_{pp}$ (Fig.6) with triangular shape. In quasi-resonant mode output ripple has more complex shape (Fig.7), but much lower level. The basic ripple is about 10 mV$_{pp}$ and the spikes are about 20 mV$_{pp}$.

Output voltage load transient response was measured with load current changed between 0.2A and 0.8A at 5ms period and at 0.5A/µs. Fig.8 shows the AC coupled output voltage under this load transient condition. As we can see over/undershoot is under 200mV.

Output voltage rise (Fig.9) was measured into the electronic load with 1A load at 300V input voltage. The rise is monotonic with small 400mV overshoot.

The picture of the converter prototype is given in Fig.10.
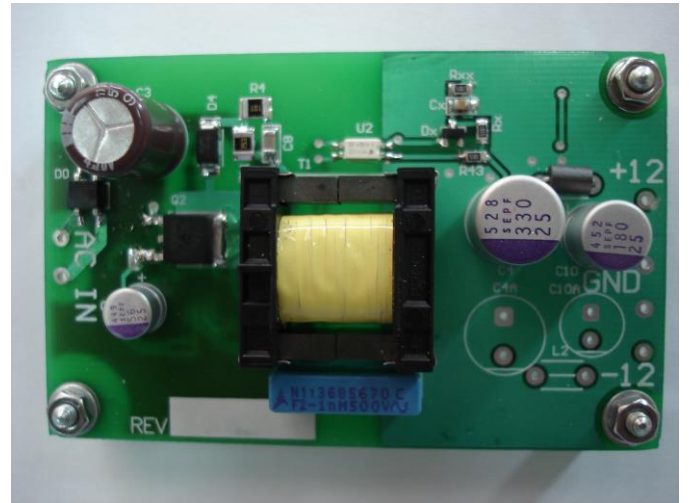
Fig.10. Converter prototype

V. CONCLUSION

In this paper the design and analysis of 12W QR flyback converter are presented. The prototype was built and tested. The results verified that the efficiency between 50% and 100% of load is over 80%. With minor changes we can make different versions of this power supply.

ACKNOWLEDGEMENT

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Problems in Assessing the Reliability of Electronic Components and Systems by Reliability Testing

Toncho Papanchev[1], Anton Georgiev[2] and Nikolay Nikolov[3]

Abstract – **This paper concerns reliability evaluation of electronic devices due reliability tests. Basic groups of tests are described. Some problems in their implementation are observed. A development in this regard is presented and guidelines for further work are outlined.**

Keywords – **Electronic Devices, Reliability, Reliability tests.**

I. INTRODUCTION

Manufacture of electronic devices has two aspects - mining and processing of raw materials on the one hand and on the other - creating a final consumer product. By increasing the reliability as an essential part of quality, the economic efficiency of the devices dramatically increases, thus compensating the lower efficiency of the commodities' conversion process.

Striving to create a competitive production imposes the extension of the classical concept of quality production, which comes down to answer questions related to the processes that follow producing of devices, such as:
- Do devices fail in the early stage of operation?
- Is the *Burn-In* process sufficient?
- Is the failure rate value acceptable in the normal operation lifecycle?
- What adjustments in the design, manufacture, operation and maintenance can lead to higher reliability?

They can be represented three levels of implementation of reliability as a concept [1]:

1. Reliability prediction - at the design stage. Reliability is assessed: - for the design - through parametrical failures; - for the elements - through sudden failure; - for the devices - through failures from defects, caused by production processes.

2. Technical (nominal) reliability – by using the data from testing of first batch samples ("zero" series) under laboratory conditions imitating the real operational once.

3. Operational reliability - according the data from real operation of mass production devices.

For electronic devices such levels are in direct correlation with the main stages of their life-cycle - design, manufacture and operation. Figure 1 shows the sequence of stages and of their constituent phases.

Creating first test samples and test series gives possibility to carry out reliability tests in order to obtain experimental data and more accurately determination of reliability parameters.

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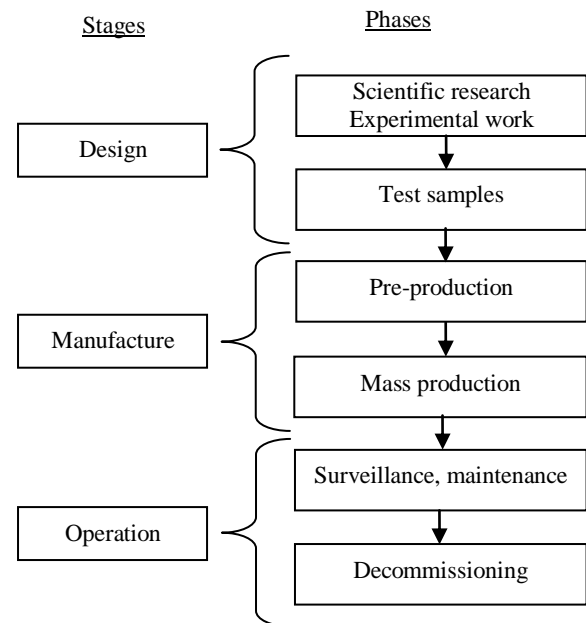
Fig.1. Life-cycle of electronic devices

The manufacturing stage consists of two phases. The first phase, called "pre-production" represents technological preparation and optimization of manufacturing processes, and also the equipment selection. Limited test series of products are produces. During the second phase, "mass production", the devices are produced in their final form, ready for field operation. Large amounts of uniform production are manufactured. It could mean, in present terms, series of several hundred to several million units of production.

Operational stage is the period of real operation of the devices and comprises the largest part of their life-cycle. During this stage the devices reveal their features, including in terms of reliability.

The reliability of electronic products throughout their lifetime is kept at the desired level by technical maintenance, including inspection, failure localization and repair, replacement parts and others. The high cost of maintenance poses questions about the optimality of the implemented procedures. The optimization of maintenance is subject to research by many scientists as Ushakov [2], Benbow and Broom [3], Moubray [4].

After a certain moment a physical and technological obsolescence of products happens. Nowadays, because of accelerated products' development and shortening the duration of the first two stages of the life-cycle the technological obsolescence often overtakes the onset of physical aging.

The assessment of reliability of the products is a procedure of successive stage-followed adjustment of reliability parameters' estimates with regard to construction, technology, manufacturing, operational algorithms, operating rules and conditions, maintenance and repair procedures, and criteria for the

occurrence of failures and boundary states.

In recent years, manufacturers achieve a significant improvement of the reliability of manufactured devices. Furthermore, a considerable part of failures are due to reasons not directly related to components and circuits, such as errors or inaccuracies in the manufacturing process, software problems, unsuitable design choices, external overstresses. This sets new issues related to precise determination of the causes of failures and difficulties associated with assessing the reliability parameters of electronic devices in terms of lack of registered failures or limited number of them.

Reliability Tests

Environmental Tests
- Environmental Stress Screening ESS
- Burn-In
- Reliability Demonstration Tests RDT
- Reliability Assessment Tests RAT

Accelerated Tests
- Accelerated Life Tests ALT
- Accelerated Degradation Tests ADT
- Highly Accelerated Life Tests HALT
- Highly Accelerated Stress Screening HASS

Fig.2. Reliability tests summary

II. RELIABILITY TESTING

A. Summary

Figure 2 presents classification of reliability tests, prepared under the criterion "conditions of the tests." Accordingly, tests can be divided into three groups:

- *Environmental tests* are held in conditions similar or identical to the most common in the real working conditions; they could be performed within normal operating conditions, but close to the border values of the main factors determining normal working conditions;

- *Accelerated tests* are held in conditions beyond the specified normal operating conditions.

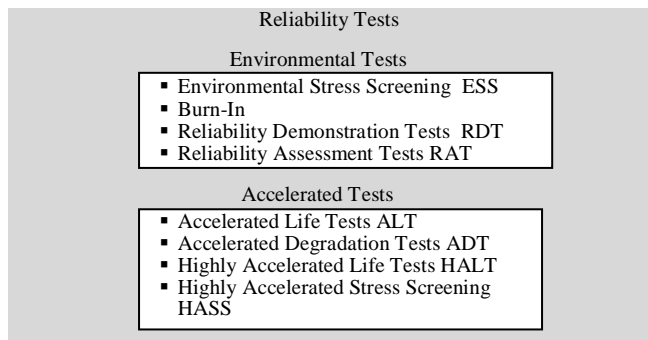In economic terms it is crucial the time needed to collect the necessary information that provides the data for assessing the products' reliability. This is the reason further in the article to be examined in details the third group of the above classification - accelerated tests.

The fast development of electronics in the last decade has imposed a shortening of the time from development to the realization of electronic products. Aiming for evaluating the reliability in short time raises the need to develop sufficiently precise and convenient for practical application test methods, which to ensure for a short time correct assessment of the main indicators of reliability – mean time to failure *MTTF*, failure rate λ, availability R(t), mean time between failure *MTBF*, etc. Under proper planning and precise execution, the accelerated tests provide reliable information to determine the potential mechanisms of occurrence of failures and modeling of the distribution law of failures of electronic products. The application of reliability testing of electronic systems and components in the initial phases of their lives is crucial to meeting the requirements for reliability in the later phases of production. Elsayed [5] describes the process *TAFT* for

elimination of design defects in the initial samples by testing, analyzing data collected, removal of registered weaknesses and re-testing. This process is generally represented by the term "Reliability growth".

In many cases, the accelerated tests are the only applicable approach to assessing reliability. They can be used for:
 a) reliability assessment electronic products and the quality of materials used;
 b) identifying types of failures, their localization in the devices under test (*DUT*) and taking actions to prevent them;
 c) electro-thermal training to remove items with hidden defects (*Burn-In*);
 d) predicting the performance of the device under real operational conditions and its behavior under extreme load stresses and external impacts.

B. Environmental tests

When stress values are close to the environmental conditions, such tests are named environmental stress screening *ESS*. In *ESS*, all the products are tested with the aim to speed up and find out the hidden defects as earlier as possible in the production cycle, making their removal cost-effectively. Such tests could be combined with systems for measuring and automation control [6], to extend the benefits beyond the usual objectives of each approach.

A special kind of reliability tests represents technological training of electronic products. In the literature it is known as electrothermal training or "*Burn-In*". *MIL-STD*-883 [7], has defined it as "... test performed to monitor or separation of the devices having internal defects or defects caused by deviations in the production process that led to failures dependent on the duration of operation and load." Burn-In provides an interesting opportunity in terms of evaluating the reliability of manufactured electronic devices due to the application a stress (thermal or electrical) on all products. This makes it possible to trace the impact on the devices not only as an originated failure or lack of it, but as changes in certain controlled informative indicators. The use of Burn-in tests in this type of classification would save costs for additional tests. Difficulties could arise due to lower stress levels and shorter duration of Burn-In tests, which limits the range of dispersion of informative indicators for classification, respectively accuracy of the final reliability classification results.

Environmental tests are also used to demonstrate the compliance of the actual assessments of reliability parameters of the devices with the specified once, regarding the requirements - reliability demonstration tests *RDT*. An example of such an approach is represented by Yadav [8]. *RDT* are usually held within normal working conditions of the devices. Similar tests are applied due delivery-and-acceptance procedures – reliability acceptance tests *RAT*. The results of these tests provide information that is used for decision about acceptance or rejection of the series of products of which was formed the tested sample.

C. Accelerated reliability tests

Highly accelerated life tests *HALT* can be performed with two different goals - to define the limits of the operating conditions of tested products, and to express and analyze all

possible failures in products. *HALT* in electronic products is carried out by applying stress factors temperature and vibrations and is used most frequently for analyzing problems in the functioning of the circuit boards. Subject to certain restrictions, such tests can be used in modeling of processes in power electrical engineering, such as lightning protection [9]. The same stress factors, but with a smaller stress values are applied in highly accelerated stress screening *HASS*, to confirm the ability of the products to function properly under cyclic loading. The main difference between the two tests is the object of study - *HALT* explore usually test samples and series prior mass production, while during *HASS* are tested samples of the mass production of the devices. *HASS* provide opportunities to 'catch' changes in the quality of the production process.

Devices, in which the aging process is manifested at an earlier stage, are tested by accelerated aging tests *ADT* [10].

The application of accelerated tests is studied and systematized by many scientists as Nelson, in his remarkable work "Accelerated Testing. Statistical Models, Test Plans, and Data Analysis" [11], Ushakov [2] and many others. Many publications and methodologies present the application of accelerated tests in different versions aimed at achieving a sufficiently precise estimates of indicators of reliability [12][13][7][14]. Escobar and Meeker, in an extended report, review many types of accelerated tests in order "to outline some of the main ideas behind the accelerated tests" and to formulate "proposals for potential contributions to which statisticians could help to the development the methods and models of accelerated tests" [15]. In another article Meeker draws attention to the problems associated with the selection, planning and implementation of accelerated tests [16]. The great variety of techniques gives engineers multiple reliability analysis tools through accelerated reliability tests, and their task is to choose the most appropriate in accordance with applied tests and available preliminary information.

D. Test planning

When tests are performed for the first time on certain products, planning is done on the basis of known theories of optimal, best plan and plan with restrictions (compromises) [11]. Prior knowledge, collected due tests on products, similar in functionality or composition, is used to initially determine the range of change in stress factors, the duration of the tests and sample size. However, there is enough uncertainty that makes plans tentative, and may lead to surpluses or shortages of required information. The possibility of further optimization of tests, through dynamic assessment of the results, is not sufficient studied. The results of such optimization can be expressed in additional spending cuts of time and money while keeping the accuracy of the final results within acceptable limits. *IEC* 61649 [17] presents set of requirements for conducting accelerated tests. Many developments in the planning and optimization of accelerated tests are presented in the scientific literature [2][17]. Test parameters usually are determined in advance on the basis of preliminary studies of conducted tests on similar devices, normative documents and optimization procedures. An important characteristic of the tests is a manner of recording the moments of occurrence of failures – exactly or roughly. If there is continuous control, by man or machine, on all tested devices, any failure is recorded at the exact moment of occurrence and there are no errors in assessing the parameters of reliability, caused by uncertainty of timing of failures. The registration of exact times of failure occurrences is difficult to realize, sometimes impossible, especially in data collection during the operation. The information about failures usually does not contain the precise moment and data can be of the following type - censored data (left or right), grouped (interval) data or reported only at the beginning and end of the test duration. It often happens to be handled with different data types in a research. While censored data of different types and exact data are object of a number of studies, the interval data is less common in the science literature.

Recently the accelerated tests are associated with tasks for evaluation of indicators describing various aspects of the reliability of devices. This determines the variety of combinations of types and combinations of stresses applied, ways for stress application and other conditions. The scientific literature describes accelerated tests, applied on electronic products, with different plans and mathematical formalism [18][19][20].

III. PROBLEMS OF ASSESSING THE RELIABILITY OF ELECTRONIC DEVICES OVER THE DIFFERENT STAGES OF THEIR LIFE CYCLE

The products' reliability depends on the decisions taken during the period of design and production. Therefore, it can be concluded that reliability is the property of the product, which is modeled and built into it and requires the investment of considerable resources and time. So considered, the process of „embedding" of reliability outlines many problems. Below are presented only two of them and the ensuing conflicts:

First problem - "materialization" of the term "sufficient reliability" for each particular product.

Second problem - decision of how to achieve the level of "sufficient reliability" in every product manufactured.

First conflict - Time: Growing competition shortens the overall length of all life stages of products: design - testing - production - operation - technological obsolescence - design of completely new product or release of devices with enhanced options. This naturally requires cutting the time spent on reliability testing and analysis of the devices.

Second conflict - Price: The wide variety of products with similar, even identical characteristics requires seeking the solutions that ensure low prices of the output product. This is reflected in the reduction of planned spending on research of reliability.

Wrong decisions lead to losses, resulting not only in unforeseen costs for warranty service, but also in reduced sales and revenue from the negative impact of the customers' dissatisfaction. The effect extends more globally; negatively affect the reputation of the manufacturer, putting question mark over its survival in a highly competitive landscape of electronic products. From the customer's perspective and in a "good" case scenario the insufficient reliability means more periods of inactivity and spending more time and money for maintenance. When it comes to manufacturers, this directly affects their current and prospective revenues. In a "worst"

case scenario, however, the consequences can be expressed with the destruction of material facilities, injuries or loss of human lives. Murthy analyzed some aspects of the above cases in a series of publications [21][22][23]. The complex nature of these problems and conflicts does not allow the formulation of a clear decision, and requires operating in an uncertainty in many ways.

IV. CONCLUSIONS AND FUTURE WORK

The problems of dynamically optimization of accelerated tests, aiming to increase the efficiency of tests by using ongoing assessment of their informativeness, are the subject of research by the authors of this publication. Algorithms are examined in Burn-In and accelerated tests [24][25]. The following issues are encountered, which are subject to further work:

1. Insufficient ability to determine the indications of classification of devices after *Burn-In*.

2. Significant complexity and the need arises to establish limits for efficient use – cost/effect.

3. It was reported, during tracing of conducting the accelerated tests, a difficulty in establishing a set of indicators defining the right moment for termination, replacement or continuation of a test. It is obtained a divergence of the chosen indicators goodness-of-fit r^2 and error function Ej, therefore it is necessary work to identify additional markers for decision making.

With regard to tests on highly reliable devices and registration of a little failures and interval data, an approach " Interval Weibayes" was proposed [26]. Further work is focused on combination of effective strategies for reliability-oriented maintenance and systems for continuous monitoring, in order to develop an approach for detection of approaching failure conditions, with the limitation of "false alarms".

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Indices for Reliability Assessment of a Star Structured Complex Electronic System

Nikolay Nikolov[1], Anton Georgiev[2] and Toncho Papanchev[3]

Abstract – **This paper concerns reliability assessment of a star structured complex electronic system. The common approaches to reliability indices selection and reliability requirements determination are presented. Some specific reliability indices and basic dependences valid for reliability assessment of a star structured electronic system are presented and described.**

Keywords – **Structural reliability, Reliability indices, Reliability of complex systems.**

I. INTRODUCTION

A complex electronic system (CES) usually comprises a large number of functional units and blocks (i.e. system elements) interconnected in such a way that the system is able to perform a set of required functions including its basic system function as well as all auxiliary functions. The system elements, together with the links between them form the system structure. Often the CES layout is shaped in line with a network topology. For SCADA (Supervisory Control and Data Acquisition) systems most often this is a centralized star topology [5].

The system and its elements have operational modes including normal operating modes, test modes and contingency modes induced by failures, faults or operator errors.

In reliability perspective each particular CES structure determines the system reliability characteristics.

The system reliability assessment is a very important task standing in front of reliability engineers during the system design process and also during the system lifespan [1]. Such assessment is able to be performed on the base of a set of reliability indices selected in such a way that it becomes possible the system reliability characteristics to be fully revealed.

II. SELECTION OF RELIABILITY INDICES FOR RELIABILITY ASSESSMENT OF CES

Selection of a proper set of reliability indices for reliability assessment of a complex electronic system (CES) is a task strongly depending on the type and the purpose of the system and also on the common functional requirements to it.

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The indices for reliability assessment of CES can be divided on operational and technical ones depending on the degree of system defragmentation [2]. The operational indices characterize the system from customer point of view, as the technical ones carry some more technological sense.

The technical indices are suitable for to be evaluated statistically. These are necessary for reliability assessment of system elements, i.e. subsystems.

Selecting the reliability indices for reliability assessment of a CES, the rules listed below is advisable to be followed:
- The total number of indices have to be the minimal one;
- The applications of complex reliability indices, presenting combinations of criteria have to be avoided;
- The reliability indices chosen have to carry a simple physical sense;
- The reliability indices chosen have to make possible performance of analytical reliability estimation during system design process;
- The reliability indices chosen have to allow a statistical evaluation of it, based on the reliability tests results or system operational data;
- The reliability indices chosen have to make possible quantitative reliability limits to be set-on.

III. REQUIREMENTS REGARDING RELIABILITY OF A CES

For to declare reliability requirements technical objects at three different levels have to be distinguished. These are systems, subsystems and components.

A. Requirements Regarding System Reliability

Determination of reliability requirements to a CES can be achieved, following three approaches. It might be based on:
- Expert advice, design engineer experience and practice;
- Prototype analysis, or statistical data for a CES similar as purpose, structure and/or component base to the current one;
- Reliability level which is optimal for the current system.

The latter approach is applicable only in case when:
- The system function is measurable by usage of the same units of measure as the expenditure of its production;
- Reliable data for components reliability are at the disposal;
- The system structure, system functioning and maintenance process are fully determined.

In this case the system function can be maximized, as follows:

$$F_k(R) = E_k(R) - C_k(R) \qquad (1)$$

where R is a system reliability index depending on the k-th variant of the system structure S_k chosen and also on the reliability of elements of the i-th kind - r_i, or:

$$R = R(S_k, r_i, k = 1,...,m, i = 1,...,n) \qquad (2)$$

where m is the number of system structure variants; n is the number of system components; $E_k(R)$ is the system function of k-th system variant as a number – value, valid for reliability level R; $C_k(R)$ are expenses for reliability level equal to R of k- th system variant to be ensured [3].

For each fixed k a solution can be found, based on the condition below:

$$\frac{\partial E_k(R)}{\partial R} = \frac{\partial C_k(R)}{\partial R} \qquad (3)$$

After that the variant of the highest absolute value have to be chosen from among of the optimal solutions $E_k(R)$.

In cases when the complex effect of the system function is incommensurable with the expenditures, only the former two approaches for system reliability requirements determination are applicable.

B. Requirements Regarding Subsystems Reliability

Normally the requirements regarding subsystem reliability are set-up when the system reliability requirements are already at the disposal.

1. Uniformly division approach.

If the system consist of a number of N elements, which are similar or identical in complexity and structure it is possible a reliability index given (R) to be equally divided in accordance with the rule below:

$$E_k = \sqrt[N]{R}, \qquad i = 1,...,N. \qquad (4)$$

In this case MTTF for the i-th subsystem is approximately equal to:

$$T_i = NT, \qquad i = 1,...,N, \qquad (5)$$

where T is the average system MTTF given.

2. Proportional division approach.

If n_i is the elements number of i-th subsystem, then:

$$T_i = \sqrt[a_i]{R}, \qquad i = 1,...,N, \qquad a_i = n_i \left(\sum_{1 \le i \le N} n_i \right)^{-1} \qquad (6)$$

If the failure rates of the elements (or prototypes) of the j – th type λ_j are known, then this approach is able to be modified by substitution in Eq.(6) of a_i by:

$$a_i = \sum_{1 \le j \le M} \lambda_j n_{ij} \left(\sum_{1 \le i \le N} \sum_{1 \le j \le M} \lambda_i n_{ij} \right)^{-1} \qquad (7)$$

3. Optimal division approach.

In case when at the time of general system reliability requirements (R) set-up the system structure (S) is known as well as the techniques for subsystems reliability improvement, i.e. functions $R_i(C_i)$, where C_i are the resources spent for provision respective subsystem of desired reliability, it becomes possible an optimal reliability requirements division to be found in two cases as follows:

  a. At the maximum of the system reliability index, when the total resource C^0 is limited:

$$\max_C \left\{ R(S, R_i(C_i)) \middle| \sum_{1 \le i \le N} C_i \le C^0 \right\}, \ C = (C_1, C_2,...,C_N) (8)$$

  b. At the minimum of the system maintenance spends, when the reliability index value given R^0 is achieved:

$$\min \left\{ C(S, R_i(C_i)) \middle| R^0 \right\} \qquad (9)$$

C. Requirements Regarding Components Reliability

The reliability requirements for electronic components usually are set-up by experts, or these are based on reliability data obtained during prototypes testing.

IV. RELIABILITY ASSESSMENT OF A STAR STRUCTURED CES

A. The Star Structure as a Monotonous Structure

Some systems, including the star structured systems, have specific characteristics in regard to system reliability. Their reliability characteristics monotonous worsen when the reliability characteristics of system elements are getting worse[7]. The structure of such systems is called monotonous structure.

A simple logical system analysis is necessary to be performed in order to be identified a monotonous structure as such one.

Let introduce a logical random variable, which can take two different values, as follows:

$$x_i = \begin{cases} 1, & \text{if the } i-th \text{ element is functioning}, \\ 0, & \text{if the } i-th \text{ element is failed} . \end{cases} \qquad (10)$$

The probability that the i-th system element is in a workable condition is determined as a math expectation:

$$p_i = Mx_i \qquad (11)$$

An n-component vector, denoted as

$$X = (x_1,...,x_n),$$

would characterize the system condition. When the system structure is fixed, the system condition depends on the condition of its elements (n in number). In case when a failed element is occurred, the vector takes the form:

$$X_i = \left(x_1, x_2, ..., x_{i-1}, x_{i+1}, ..., x_n\right) \qquad (12)$$

or it becomes an (n-1)-component vector. The i-th component is missing. Generally for all missing components is valid

$$i \in \alpha,$$

and the number of vector components is equal to

$$n - |\alpha|.$$

The system condition can also be described by a logical random function. In this case this will be a structural system function. This takes the value as follows:

$$\varphi(X) = \begin{cases} 1, \text{ if the condition } X \text{ is equal to workable system condition}; \\ 0, \text{ if the condition } X \text{ is equal to non-workable system condition}. \end{cases}$$

The probability about the system to be in a workable condition is determined as a math expectation of the structural system function:

$$h = M\varphi(X) \qquad (13)$$

This index can be expressed by reliability indices of system elements, as follows:

$$h(p) = h(p_1, ..., p_n) \qquad (14)$$

The system structure is assessed as a monotonous one in cases when the equations listed below are valid for the current system. These are:

$$\varphi(1) = 1, \text{ where } 1 = (1,1,...,1); \qquad (15)$$
$$\varphi(0) = 0, \text{ where } 0 = (0,0,...,0); \qquad (16)$$
$$\varphi(X) \geq \varphi(Y), \text{ if } X > Y \qquad (17)$$

The latter equation aggregates a number of n conditions of the type

$$x_i \geq y_i, \quad for \quad i = 1,...,n,$$

and at least one of it have to be strictly fulfilled.

Taking into consideration the arguments expressed so far it becomes clear that a star structured systems have to be assessed as a monotonous one. This conclusion gives the opportunity a logical structural reliability analysis to be performed in regard to a star structured CES.

The reliability function of such system can be presented as:

$$h(p) = p_i M\varphi(X_i, \quad x_i = 1) + q_i M\varphi(X_i, \quad x_i = 0) \quad (18)$$

where

$M\varphi(X_i, \quad x_i = 1)$ is the probability the system to work proper under condition that the i-th element is absolutely reliable.

$M\varphi(X_i, \quad x_i = 0)$ is the probability of the same, but under condition that the i-th element is definitely failed.

The reliability system function can also be similarly expanded in regard to two system elements i-th and j-th

ones[6]. In this case the system reliability function takes the form as follows:

$$\begin{aligned} h(p) = &\, p_i p_j M\varphi\left(X_{ij}, \, x_i = 1, \, x_j = 1\right) + \\ &+ p_i q_j M\varphi\left(X_{ij}, \, x_i = 1, \, x_j = 0\right) + \\ &+ q_i p_j M\varphi\left(X_{ij}, \, x_i = 0, \, x_j = 1\right) + \\ &+ q_i q_j M\varphi\left(X_{ij}, \, x_i = 0, \, x_j = 0\right) \end{aligned} \qquad (19)$$

The latter equation gives the opportunity to assess the structural reliability of a star structured CES by taking into consideration the peculiarity of the star topology, i.e. non-equality of elements positioned at different hierarchic levels of this structure. It becomes obligatory the system reliability function to be expanded in regard to these system elements, which stand at the structural hierarchic levels higher that the lowest one, or by the other words which are not peripheral system elements. Their influence and impact on the system reliability can be fatal, because a failure of each of it can cause a failure of a system branch or a total system failure (when the system element at the highest level failed).

B. The Star Structured CES as a System with an Additive Factor of Effectiveness

The structure of some specific electronic systems (star structured systems are also included) consists of functional redundancy [4]. This makes the system able to functioning even in case when one or some partial failures are been occurred. Then the system continues to work with decreased quality and efficiency of functioning, but it is not totally failed.

For qualitative assessment of functioning of such systems it is advisable a quantitative index to be introduced, i.e. quality of system functioning. This takes into consideration the influence and also the impact of partial failures on system functioning. The effectiveness of system functioning is a quantitative characteristic of quality and quantity of work performed by the system.

Star structured CES are systems which are characterized by a relatively simple effectiveness factor. Each peripheral element of such system brings its separate and independent contribution to the effectiveness of the entire system. These systems are known also as systems with an additive effectiveness factor. Such behavior is typical for most of the SCADA systems.

If the contribution of the i-th element to the system effectiveness is φ_i, then the system effectiveness of a system intended for short term of operation at a time t, would be:

$$E = \sum_{1 \leq i \leq n} \varphi_i r_i(t) \qquad (20)$$

where $r_i(t)$ is the probability the i-th element to be in a workable condition at the moment of t.

Consider a CES which is built up in line with a centralized star topology [8]. The system structure also can be described as a star within a star. This is shown on Fig.1. The system is

spread over two sites of service. The system structure consists of a number of $n+1$ elements and three hierarchic levels. One of the system elements is positioned at the I-st (the highest) hierarchic level, two elements are at the II-nd level and a number of $n-2$ peripheral (end) elements are positioned at the III-th (the lowest) level. A number of $m-2$ of it are installed at the first service site and the rest of it (a number of $n-m$), are respectively installed at the second site of service.
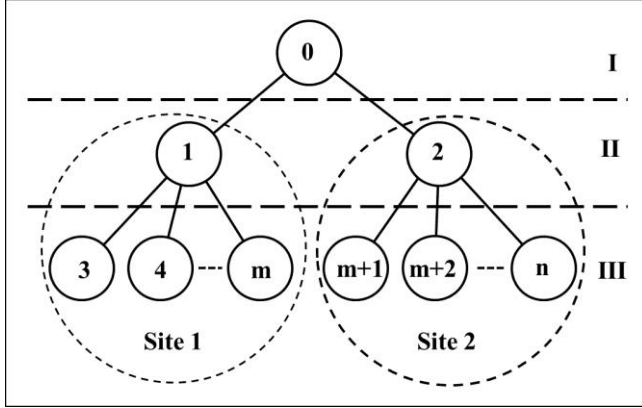

Fig.1. Star structured CES topology

Obviously the peripheral elements would be able to function effective only in case when the elements positioned at the I-st and II-nd level are in a workable condition. If K_i is availability of the i-th element, then for the system effectiveness is valid:

$$E = K_0\left(K_1 \sum_{i=3}^{m} K_i \varphi_i + K_2 \sum_{i=m+1}^{n} K_i \varphi_i \right). \quad (21)$$

In case when all peripheral elements at a site of service are similar, or identical and bring an equal contribution to the system effectiveness (which is typical for most of the SCADA systems), the system effectiveness can be presented as:

$$E = K_0\left[K_1 (m-2)\varphi_1 \sum_{i=3}^{m} K_i + K_2 (n-m)\varphi_2 \sum_{i=m+1}^{n} K_i \right] (22)$$

Consider the same system but intended for a long term operation. Let the contribution of the i-th element to the system effectiveness is $\varphi(t)$. In case of a failure at the moment $t \leq t_i \leq t_0$, for the system effectiveness is valid:

$$E(t, t+t_0) = \sum_{i=1}^{n}\left[r_i(t, t+t_0)\varphi_{0i} + \int_{t}^{t+t_0} f_i(x_i)\varphi_i(x_i)dx_i \right], (23)$$

where φ_{0i} is the contribution of i-th element to the entire system effectiveness if it was in a workable condition during the time interval $(t, t+t_0)$.

Now it is possible to determine the effectiveness of the SCADA system already described. Let it was intended for a long term operation. The failure rate of the i-th system element is denoted as λ_i. The reliability function of each element allows an exponential distribution. In this case the average system effectiveness at a random moment of time t, can be determined as:

$$E(t) = e^{-\lambda_0 t}\left[e^{-\lambda_1 t} \sum_{i=3}^{m} \varphi_i e^{-\lambda_i t} + e^{-\lambda_2 t} \sum_{i=m+1}^{n} \varphi_i e^{-\lambda_i t} \right]. \quad (24)$$

The equation above gives the opportunity to determine the system effectiveness by the specific failure rate and also by the individual contribution factor of each system element.
The latter depends not only by the element function but also by the characteristics of the object served.

V. Conclusion

The main problem in reliability assessment of a star structured CES appears to be the evaluation of the contribution of each peripheral element to the entire system effectiveness, even in cases when this contribution is similar or identical for all peripheral elements or only for these installed at the same site of service. These might be estimated upon an expert advice for each specific CES application. The rest reliability indices like the elements availability and the elements failure rate can be evaluated using data obtained by testing of prototypes, or might be estimated upon data for similar or identical elements at disposal. It is also possible for this purpose to be used data obtained during operation of the same or similar elements for long enough time. Based on this it becomes possible to estimate system effectiveness for a star structured CES for each specific application.

Acknowledgement

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Using Wireless Interfaces in a Smart Home Model

Valentina Rankovska [1]

Abstract – **In this paper the application of wireless interfaces in embedded systems for monitoring and control is examined. A model of smart house is synthesized, applying wireless interfaces, designed for educational purposes. The core of the system is Arduino board with a possibility of remote Android based control.**

Keywords – **Embedded Systems, Wireless Interfaces, Smart Home Model, Arduino.**

I. INTRODUCTION

The architecture and the features of embedded systems develop continuously - they are becoming more diverse in composition and functions, more flexible, adaptable and reliable.

Their development through the years can be summarized to the following three phases:

- In the early days of occurrence and development of the microprocessor systems they are single- or multiple-board systems, based on microprocessors, memories and peripheral units - timers, parallel, synchronous and asynchronous serial interfaces, etc. as separate ICs.

- The occurence of microcontrollers in the early 70s of the last century leads to increased reliability, speed, flexibility, miniaturization.

- Nowadays, together with the growing variety of microcontrollers with enhanced features and parameters, on one hand the number and type of the peripheral intelligent programmable devices grows increasingly - sensor units, actuators, etc., and on the other control is not limited only to the use of microcontrollers as control devices.

Wireless interfaces allow building networks consisting of heterogeneous in nature components. In the process of controlling the intelligent programmable modules, collection and processing of information from them and other activities, easily can be incorporated a variety of "standard" mobile devices such as smartphones, tablets, laptops and more.

In general the methods and tools for monitoring, control, collection and processing of data using wireless interfaces evolve rapidly and are used in all spheres of life: building automation, industrial applications, automotive and medical industry and many others.

Wireless communication offers a flexible and reliable approach to object control, obtaining information on its parameters and state, receiving data and organize them in a database, etc.

There are various forms of wireless communication based

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on different frequency bands, modulation methods and protocols, which are briefly presented in Part II.

A smart home model implementing wireless interfaces is presented in part III.

The model is intended for educational purposes in Microprocessor Circuits and Embedded Systems for the Bachelor degree students in Electronics in the Technical University of Gabrovo.

II. A SHORT SURVEY ON WIRELESS INTERFACES

As wireless interfaces provide a range of advantages in data transfer in modern embedded systems, more and more devices that have the ability to connect wirelessly with others are produced. That is why the terms "Internet of Things" and "Wireless Connectivity of Things" are presently widely spread. [1], [2], [3], [4]

Using the infrared range for data transfer is implemented long ago, for instance as a remote control of various devices. But due to a number of advantages it gained a rapid development and is widely used to connect various devices such as PC and peripherals.

Advantages:
- Infrared signals are easily generated and identified;
- As the generated signals are out of the limits of the visible spectrum, it is easy to apply optical filters, excluding totally the visible light and therefore the interference;
- High level of channel safety;
- Low price of the hardware and also lack of law regulation.

Drawbacks:
- Need of direct visibility and therefore ability for short distance connection. That limits its application in implementing larger networks;
- The data transfer is peer to peer.

Bluetooth interface is especially made to replace the cable connections at office and home appliances. Frequencies in the 2,4 - 5 GHz range are used, a frequency band initially reserved for industrial scientific and medical (ISM) purposes. Nowadays it is widely used for data transfer in local wireless networks. The Bluetooth specification is maintained by Bluetooth Special Interest Group (SIG), founded in 1998.

Main features:
- Low power radio connection – typical power consumed about 1 mW;
- Typical range – 10 m;
- Data baud rate, initially 1 Mb/s, bu for instance Bluetooth 2.0 - to 3 Mb/s at distances to 100 m;
- Simultaneous connection with up to 8 devices.

The advantages of the Bluetooth technology are reduced size of the equipment, simple usage, safety of the data transferred, and good maintenance of the standard.

Some disadvantages are the comparatively high power consumption and impossibility to organize complex configuration networks.

Unlike other wireless technologies, where the aim is to provide high data transfer rate, long distances, etc., *ZigBee* (IEEE 802.15.4) [3] is created with opposite requirements for small range, low price, low power consumption, low data transfer range and low size of the equipment used, and also low requirements to the software. It uses the standard „Low-Rate Wireless Personal Area Networks - LR-WPAN - IEEE 802.15.4". Like Bluetooth, the radio band ISM is used.

It is suitable especially for home automation systems and some measurement and control systems together with using not expensive microcontrollers. The data transfer rate is comparatively low and the power consumption - minimal. Main application areas are as follows: receiving data from moving or rotating parts of conveyers, robots, etc., industrial systems for monitoring and control, wireless connection with sensors, tracing the route of the movement and location of property and equipment, security systems, etc.

The ZigBee standard, like Bluetooth, uses the baud transfer range of 2,4 GHz. The largest baud rate is 250 kbit/s. Although it provides typical data transfer distance 10 m, there are no requirements to the transmitter power. The most common transmitters are 1 mW (to 10 m), 10 mW for distance to 80 m indoors and to 1 km at line of sight. Increasing the distance can be achieved using antennas with a special design.

Minimized power consumed is a result of the fact that the slave devices are in idle state most of the time. They get active for short periods of time only to confirm their presence in the network.

Implementing ZigBee networks with various topologies could be configured – star, tree, mesh.

Connecting the components of an embedded system to Internet, including via Wi-Fi, results in additional advantages as the user can access the network components almost from everywhere [5]. Furthermore no special knowledge and skills are required to configure the network.

The main advantages of the Wi-Fi are the following:
- No licensed radio range is used and no law regulation for individual users;
- Quickly developing area, which allows usage of more and more devices communicating via such interfaces;
- Relatively low price;
- Roaming is possible, which allows the user with mobile devices to move from one access point to another;
- There are different levels of data encryption to protect traffic, etc.

A brief comparison of wireless interfaces for embedded systems according to different criteria is given in Table 1 and Table 2 [1], [3].

TABLE I

	Wi-Fi	Bluetooth	Bluetooth LE	ZigBee	Sub GHz
Internet-Connected Device	Best	OK	OK	Poor	Poor
Smartphone Accessory	OK	Best	OK	Poor	Poor
Range	OK	OK	OK	OK	Best
Low Power Consumption	OK	OK	Best	OK	Best
High Data Rate	Best	OK	Poor	Poor	Poor
Interoperability Between Vendors	Best	Best	OK	Poor	Poor

III. THE SMART HOME MODEL

The smart home model is a suitable complex example to study various components of embedded systems - control devices and actuators, sensor modules, interfaces for data exchange and in particular the interface "man-machine". It also provides wide opportunities for implementation and testing of a number of modern wireless interfaces.

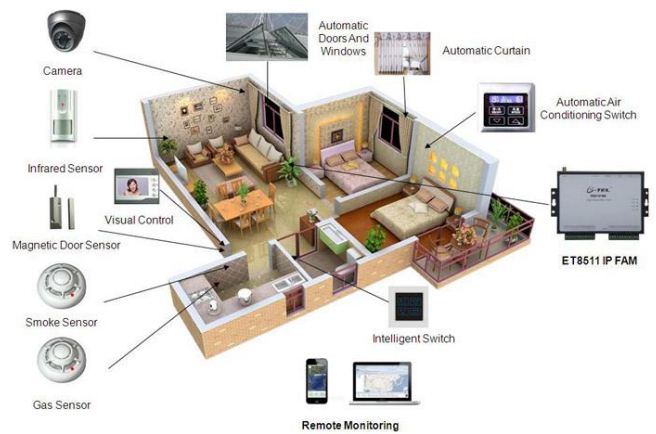An example of such a system is shown in Fig. 1 [6].

Fig. 1. A smart home example

The main criteria, defining a building as "smart", are the following [6]:
- Input system, which receives information through a corresponding receiver. This can be done in four ways: by sensors (in real time), internally stored and recovered data, manually entered (programming and reprogramming) by the users and available online (Internet).
- Processing and analysis of information - performed by control system;
- Output system which responds to input data in the form of some actions;
- Response time requirements;
- Self-teaching ability.

The following stages can be identified in the development and services of the smart home:

1. First stage – the components are autonomous devices which communicate with other devices in home. These first devices are: bought and installed (and a part of) a home security system; a home cinema system or Do It Yourself (DIY). Using a variety of communication technologies, they usually do not communicate with each other directly but with their controllers.

TABLE II. A COMPARISON OF THREE LEADING WIRELESS TECHNOLOGIES

Parameter, m	Bluetooth/IEEE 802.15.1	ZigBee/ IEEE 802.15.4	Wi-Fi/ IEEE 802.11
Distance, m	~ 10 (50-100)	10	~100
Baud rate, Mbit/s	0.723	0.250	1-2 to 54
Max number of devices in the network	8	245	unlimited
Power consumption, mW	10	1	50
Operational time supplied with 2 baterries AA	-	6 months in standby mode	-
Price/complexity, conditioned units	10	1	20
Main purpose	A connection PC - peripheral devices	Wireless sensor networks	Wireless Ethernet extention

2. The second stage is the Internet connectivity - once connected with Internet the devices could be controlled via a smartphone or other mobile devices.

3. In the third stage these smart devices can communicate and exchange information between each other, without necessity of a human intervention. [7]

The wireless interfaces begin to be widely applied during the second and third stage.

The architecture of the smart home model is shown in Fig. 2.
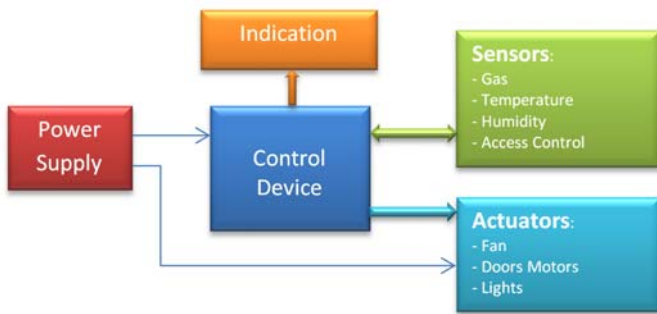
For now the following functions have been implemented:

Fig. 2. The architecture of the smart home model

• Access control with Radio Frequency Identification (RFID);
• A garage door control via Bluetooth interface;
• A smoke senor;
• Detecting of presence and turn on / off lights;
• Measurement, indicating and regulating the environment temperature;
• Humidity measurement and indicating;
• Remote control of indoor devices via Bluetooth interface
• LCD indication.

The model components - the control unit and the sensors and actuators have been selected taking into account the compromise between low cost and desired features, because it is intended for educational purposes [8].

The open hardware development board Arduino Uno is chosen as a control unit (Fig. 3) [9]. It is suitable because of its compact size and low cost. It is based on the 8-bit RISC

Atmel microcontroller – ATMega328. The microcontroller includes 32 KB Flash program memory, 2 KB SRAM data memory, 2 8-bit and 1 16-bit timer/counter, RTC, 8-channel 10-bit ADC, serial interfaces (USART, SPI, IIC), etc.

Arduino is a good choice for educational and hobby purposes, as it can be used as a ready to use core for an embedded system:

• A possibility is provided to power supply and program the microcontroller and peripherals via USB from a PC, and also independently - from a separate connectors for power supply and in-circuit serial programming;
• Clock frequency;
• Reset circuit;
• Expansion connectors accessing all the general purpose input/output pins of the microcontroller. It is possible easily to connect various peripheral modules to them and also to put on the Arduino board and connect so called shields with various purpose produced by many companies.

In future improvements including web-based control Arduino Uno could be used with an Ethernet shield or to be easily changed with another compatible development board, for instance Arduino Leonardo.

The access control is implemented using radio-frequency identification (RFID) module, which is intended for access control, personal identification, home automation, etc. A mini-RFID module has been chosen, with 125 kHz frequency, distance for reading to 35 mm. It is used for reading passive RFID tags, cards, etc.

For the remote control of devices such as garage door, lights, etc. bluetooth interface is implemented by the inexpensive module HC-05. Some features: 2.4GHz ISM band, supports baud rates 2400 -1382400, default COM setting: 9600, N, 8,1.

The doors of the room and the garage are closed/opened by small motors.

Mini PIR sensor HC-SR505 is implemented *to detect motion* for distance to 3 m, induction angle: <100 degree cone angle and induction distance - 3 meters.

Temperature and humidity are measured by sensor module DHT-22 with accuracy: humidity +-2%RH (max +-5%RH); temperature <+-0,5 Celsius; resolution: humidity 0.1%RH; temperature 0.1 Celsius.

With increasing/ decreasing the temperature a fan is switched on/ off and also its speed changes when changing the temperature range.

The sensor MQ-2 module is useful for detecting gas leakage - LPG, i-butane, propane, methane, alcohol, hydrogen and

Fig. 3. Arduino Uno Development board

Fig. 4. Ardudroid application

smoke for home and industrial applications.

To remotely control some devices via bluetooth interface and Android based device, like tablet, smartphone, etc., the free application Ardudroid is used (Fig. 4) [10]. It allows a direct control of the development board pins - digital, analog and serial interface.

IV. CONCLUSION

The implementation of wireless interfaces in embedded systems for various applications is presented.

A Smart Home model is designed. It is used in teaching "Microprocessor Circuits" and „Embedded Systems" for the Bachelor degree students in Electronics in the Technical University of Gabrovo. The model can be used to study the various components of embedded systems, in particular the wireless interfaces. It is convinient because, unlike other hardware development tools used in the laboratory classes, it includes several devices interfacing wireless in one project.

The further development of the project includes remote monitoring and control via web-based interface (Ethernet and Wi-Fi), and the development of additional modules to the system.

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