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POWER EFFICIENT WALLACE TREE MULTIPLIER USING FULL SWING GATE DIFFUSION INPUT TECHNIQUE

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ABSTRACT

This paper proposes the design and gate level implementation of a low power and area efficient 8-bit Wallace tree multiplier design using Full Swing Gate Diffusion Input Logic technique. The proposed design, developed using 45nm process technology was compared with its equivalent design, developed using conventional CMOS technology. The proposed multiplier presented significant advantages in terms of power, delay and area. Power and delay analysis of the proposed multiplier was performed for varied gate oxide thickness and three process technologies - 130 nm, 70nm and 45 nm. The design was subjected to parametric variations, such as gate oxide thickness and channel length. The results conclude to two major inferences. Firstly, in applications that demand low power, the proposed Full Swing Gate Diffusion Input Logic Wallace tree multiplier will be an ideal replacement for conventional CMOS multiplier, owing to reduced power and area. The proposed multiplier offers 26.21% reduction in power, 12 % reduction in delay and 36% reduction in area when compared to its equivalent CMOS version. Secondly, as transistor dimensions reduce, parametric variations become more significant. This analysis will aid in drastic reduction of parametric yield loss.

Keywords: GDI, FSGDI, power, wallace, multiplier, CMOS, delay, area, integrated circuits.

INTRODUCTION

The semiconductor industry focuses on integrating billions of transistors onto a single chip. Integrating transistors with similar characteristics is highly critical as feature sizes of transistor are reduced. Decrease in feature size in VLSI technology has created high significance in analysis of process parameter variations and is a primary design issue for analog designers. Moreover, parametric variations that arise during VLSI fabrication process causes variations in performance of circuit and also leads to parametric yield loss [1]. Hence, with decreased feature sizes, the prediction of behavior of a circuit based on process variations is ranked on a top priority scale [2].

Adders and multipliers are the fundamental building blocks of an ASIC. Low power realization of adders and multipliers leads to the development of a power efficient ASIC. Researchers have focussed on various gate level techniques to realize power, delay and area optimized designs. Traditionally, CMOS pass transistor and transmission gate based logic styles have dominated gate level implementation of circuits [3]. The distinct advantages of CMOS logic styles are low static power dissipation and high noise immunity. The alternative design topology that offered, low power when compared to static CMOS was pass transistor logic style. However, the issue of reduced voltage swing was the primary concern in realization of pass transistor designs. Gate Diffusion Input Logic (GDI) [4-7] is a special case of pass transistor logic that uses both n-MOS and p-MOS pass transistors. Figure-1 portrays the schematic representation of a basic GDI cell [5]. Three inputs drive the terminals of a basic GDI cell-Gate of PMOS and NMOS, Source of n-MOS and p-MOS. The output is driven at the Drain terminals of n-MOS and p-MOS.

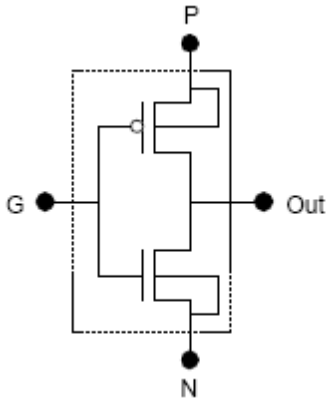

Figure-1. Basic GDI cell.

Table-1 shows the simple Boolean functions that are realized using basic GDI cell [5].

Table-1. Fundamental Boolean functions using GDI cell.

Inputs			Out	Function
N	P	G		
'0'	B	A	$\bar{A}B$	F1
B	'1'	A	$\bar{A} + B$	F2
'1'	B	A	A + B	OR
B	'0'	A	AB	AND
C	B	A	$\bar{A}B + AC$	MUX
'0'	'1'	A	$\bar{A}$	NOT

The gates implemented using GDI and modified GDI technique [8] yielded reduction in power when

compared with conventional CMOS technique. GDI based full adder in varied architectural styles was implemented [9]. However, GDI offered reduced voltage swing at the output of GDI gates. This issue was resolved in Full swing Gate Diffusion Input (FSGDI) technique [10]. Full swing was obtained at the output of the FSGDI gates because of the Swing Restoration (SR) transistors. The schematic of functions F1 and F2 using FSGDI cells is shown in Figure-2. Depending on the inputs, the SR transistor pulls the output to either V_{DD} or GND, thereby obtaining full voltage swing. Hence, FSGDI can comfortably be cascaded to realize complex combinational circuits.

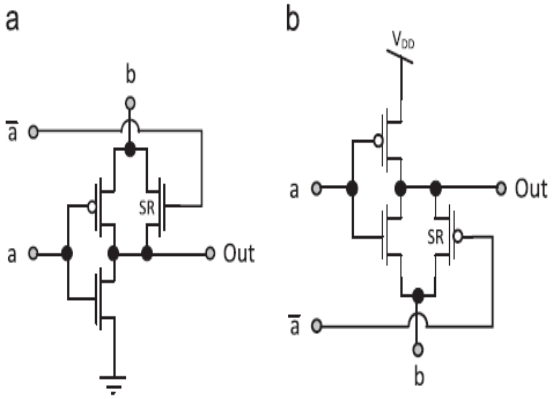

Figure-2. F1 and F2 cells using FSGDI technique.

An efficient realization of multiplier depends on the basic cell - adder. Power efficient GDI based adders have evolved ever since the inception of GDI technology [11-15]. Design of GDI based Viterbi decoder [16], Magnitude comparator [17] and memory structures [18] have also been presented by researchers exploiting the advantages of GDI.

FSGDI technique presents a promising future for low power designs. Hence, it is highly essential to analyse the effect of process variations [19] on FSGDI circuits. The prime process parameters are channel length, channel width, gate oxide thickness, mobility and doping intrinsic concentrations. This paper proposes the design of 8-bit Wallace tree multiplier using FSGDI technique and the design is analysed for varying device parameters.

PROPOSED FSGDI WALLACE TREE MULTIPLIER

Wallace tree multiplier is an efficient hardware that is based on column compression technique. The delay is proportional to logarithm of word length of multiplier operand [20]. Consequently Wallace tree multipliers, which possess irregular structure is faster than array multipliers. At gate level, the architecture is conventionally developed using CMOS technology. However, FSGDI combinational circuits offer low power when compared with combinational circuits designed using CMOS technology. The reduction tree of the proposed 8x8 unsigned FSGDI Wallace tree multiplier is shown in Figure-3. Every single dot represents a partial product, which are consequently reduced further by FSGDI full adders and FSGDI half adders.

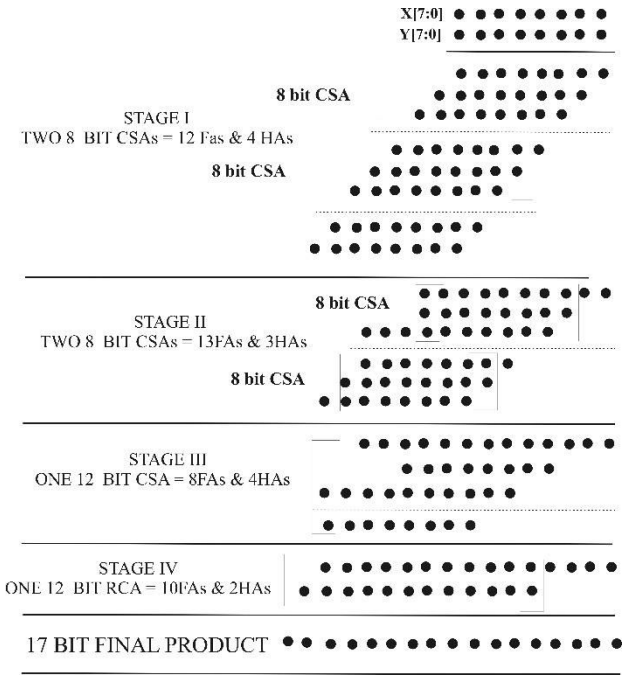

Figure-3. Proposed 8x8 bit unsigned FSGDI Wallace tree multiplier.

FSGDI circuits are designed using Shannon's theorem [3]. The equations for Sum and Carry for a 1-bit Half Adder are shown in Equations 1 and 2.

$$\text{CARRY} = AB$$
$$= A.F(1,B) + \overline{A}.F(0,B)$$
$$= A.B + \overline{A}.0 \quad (1)$$
$$\text{SUM} = A \oplus B$$
$$= \overline{A}B + A\overline{B}$$
$$= [A.F(1,B) + \overline{A}.F(0,B)]$$
$$= A.B + \overline{A}.B \quad (2)$$

The equations for Sum and Carry for a 1-bit Full Adder are shown in Equations 3 and 4

$$\text{CARRY} = AB + BC + CA$$
$$= A.F(1,B,C) + \overline{A}.F(0,B,C)$$
$$= A.(B + C) + \overline{A}.(B.C)$$
$$= A.[B.[F(1,C)] + \overline{B}.[F(0,C)]] +$$
$$\overline{A}[B.[F(1,C)] + \overline{B}.[F(0,C)]]$$
$$= A.[B.1 + \overline{B}.C] + \overline{A}.[B.0 + B.C] \quad (3)$$

$$\text{SUM} = A \oplus B \oplus C$$
$$= A.F(1,B,C) + \overline{A}.F(0,B,C)$$
$$= A.(\overline{B \oplus C}) + \overline{A}.(B \oplus C)$$
$$= A.[B.[F(1,C)] + \overline{B}.[F(0,C)]] +$$
$$\overline{A}[B.[F(1,C)] + \overline{B}.[F(0,C)]]$$
$$= A.[B.C + \overline{B}.\overline{C}] + \overline{A}.[B.\overline{C} + \overline{B}.C] \quad (4)$$

Equations 1 and 2 are realized at gate level using FSGDI technique, to obtain FSGDI half adder as shown in Figure-4. Similarly, equations 3 and 4 are realized at gate level using FSGDI technique, to obtain FSGDI full adder as shown in Figure-5.

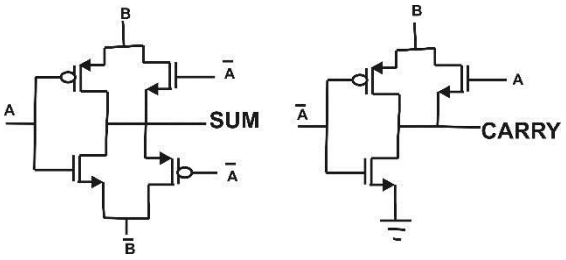

Figure-4. FSGDI half adder.

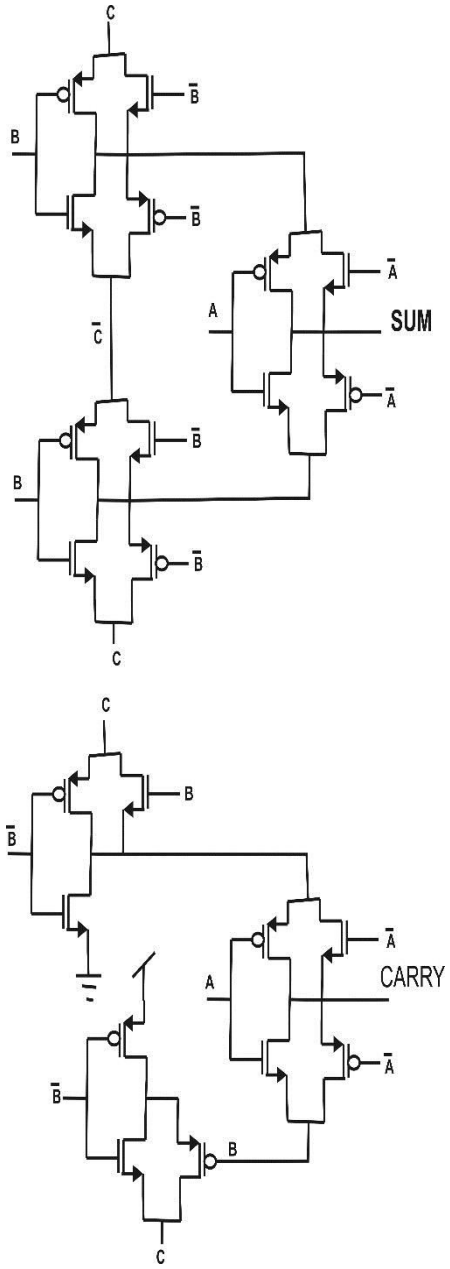

Figure-5. FSGDI full adder.

COMPARISON OF FSGDI AND CMOS WALLACE TREE MULTIPLIERS

FSGDI Wallace tree multiplier shown in Figure-3 is designed in Tanner EDA tool using 45nm technology library Standard sized transistors $(W/L)_n = (120nm/45nm)_n$ and $(W/L)_p = (120nm/45nm)_p$ are used. PMOS transistors are sized twice the size of NMOS transistors. The circuit was operated at a supply voltage of 1.5V. The functional verification of the proposed multiplier was performed. The simulation waveforms of some of the bits of the multiplier product is shown in Figure-6.

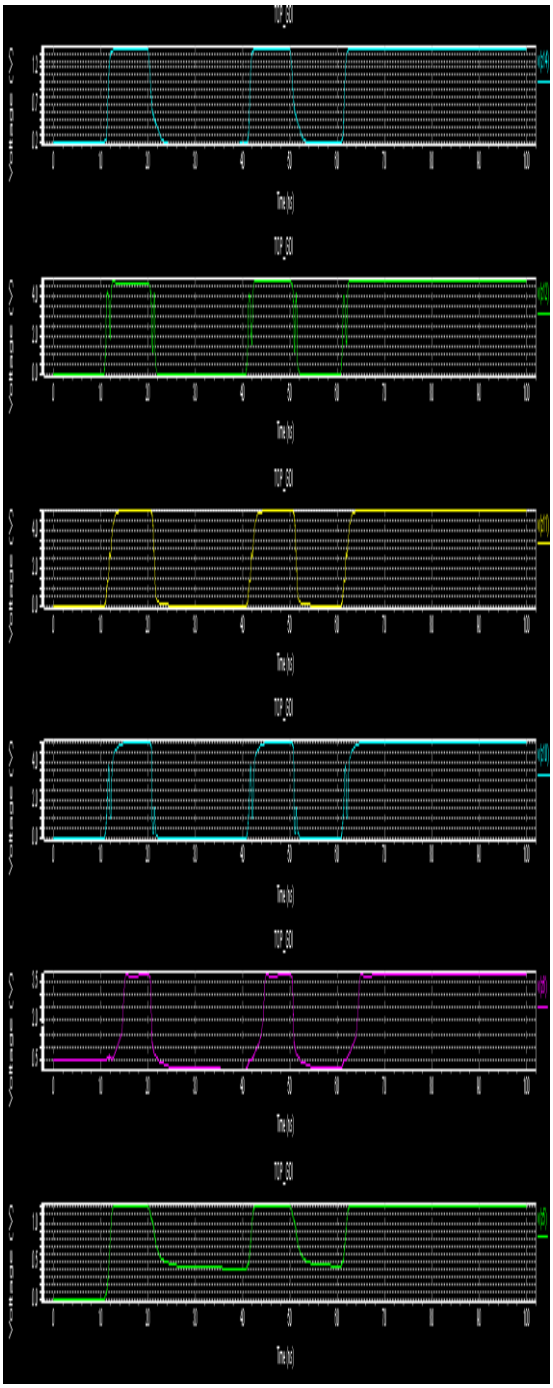

Figure-6. Simulation waveforms of FSGDI Wallace tree multiplier.

The equivalent Wallace tree multiplier using CMOS was designed. The proposed FSGDI and CMOS Wallace tree multipliers are compared on metrics such as Power, Delay, Power Delay Product (PDP) and Area to evaluate the performance of the proposed multiplier. The results are summarized in Table-2.

Table-2. Power, delay, power delay product (PDP) and area of FSGDI and CMOS Wallace tree multipliers.

Modules		Power	Delay	PDP (Power Delay Product)	Area (Number of transistors)
Half adder	FSGDI	346 nW	2.24 ps	0.77 aWs	7
	CMOS	608 nW	1.94 ps	1.18 aWs	12
Full adder	FSGDI	610 nW	2.24 ps	0.99 aWs	22
	CMOS	884 nW	3.12 ps	1.36 aWs	34
Wallace tree multiplier	FSGDI	532 µW	30.41 ps	16.17 aWs	1145
	CMOS	721 µW	34.56 ps	24.91 aWs	1792

The results depict that the submodules FSGDI full adder and half adder offer 31% and 43% reduction in power when compared with its equivalent CMOS version. FSGDI multiplier offers 26.21% reduction in power when compared with its equivalent CMOS version.

The average propagation delay of FSGDI modules was comparatively greater than its CMOS versions. FSGDI full adder and half adder offer 28% and 13% decrease in delay when compared with CMOS version. FSGDI multiplier offers 12% decrease in delay when compared with its equivalent CMOS version.

Power delay product (PDP) is an optimal estimate to evaluate the performance of the circuit. PDP of FSGDI multiplier is reduced by 35%, which is the major performance metric of FSGDI Wallace tree multiplier.

The second significant advantage of FSGDI multiplier is the decrease in area, which is contributed by the reduction in number of transistors. FSGDI multiplier offers 37% reduction in area when compared with its CMOS version. The result in terms of performance metric is shown in Figure-7.

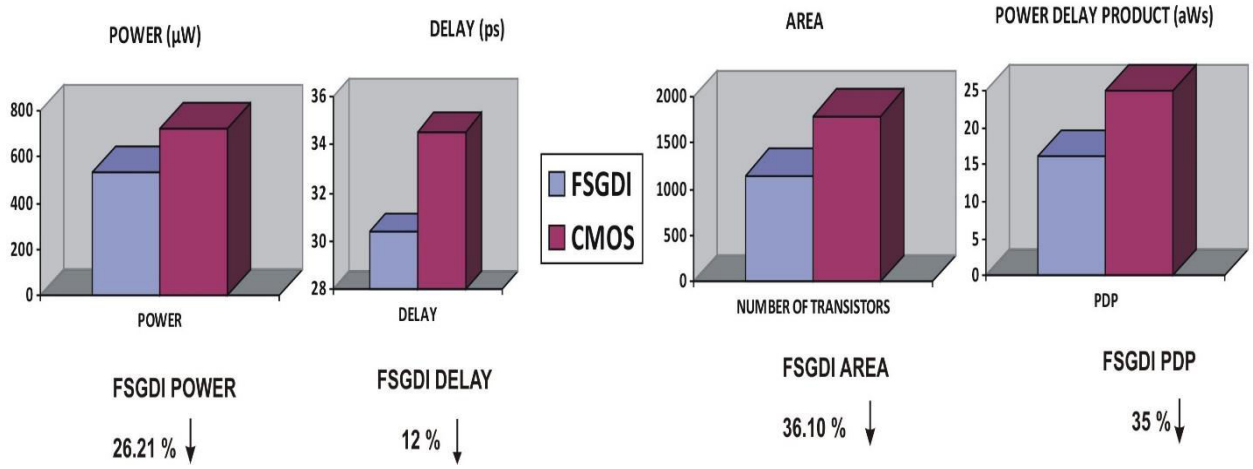

Figure-7. Comparison of power, delay, Power Delay Product (PDP) and area of FSGDI and CMOS Wallace tree multipliers.

The decrease in power, delay and area of the proposed multiplier puts forth a promising future for FSGDI designs. The reduced number of transistors reduces the load capacitance, which decreases the RC delay. Reduced load capacitance reduces the power dissipation as given by Equation 5.

$$P = \alpha C_L f V_{DD}^2 \quad (5)$$

In FSGDI circuits, the output node is necessarily not always connected to the supply rails V_{DD} and GND. This reduces the current drive on the transistors, thereby reducing the power dissipation.

EFFECT OF VARIATION OF DEVICE PARAMETERS ON FSGDI AND CMOS WALLACE TREE MULTIPLIERS

Gate level designs of VLSI circuits rely on the MOS model libraries provided by the semiconductor industry. It is highly essential to analyse the performance of the design for varied MOS parameters. The significant material parameters of MOS models are channel length, mobility, gate oxide thickness, threshold voltage and oxide

charges. The variations of these parameters are characterized by the MOS model technology files.

Simulation of the proposed multiplier for varied Channel length and Gate oxide thickness is performed to provide a statistical measure of performance of the multiplier. As channel length decreases, propagation delay also reduces as given by Equation (6)

$$t_{pd} \approx \frac{4C_L V_{DD}}{k_n(V_{DD} - V_t)^2} \quad (6)$$

$$where\ k_n = \frac{W_n}{L_n}\mu_e C_{ox}$$

Decrease in channel length, reduces load capacitance as given by Equation (7) [7]

$$C_L = C_{ox}\left(L.W_n + L.W_p\right) + C_{parasitic} \quad (7)$$

As C_L is lowered, power dissipation and propagation delay also decreases as given by Equation (5) and (6).

Simulation of multiplier for deviation in gate oxide thickness was performed for three different technologies 130nm, 75nm and 45nm. The variations in power and delay for 130nm, 75nm and 45nm technology are illustrated in Tables 4, 5 and 6, respectively.

Table-3. Variation in power and delay due to deviation in gate oxide thickness for 130nm fabrication process technology.

$t_{ox\_n(m)}$	$t_{ox\_p\ (nm)}$	Deviation in t_{ox_n} (%)	Deviation in t_{ox_p} (%)	Deviation in power (%)	Deviation in delay (%)
2.54	3.26	-20.63	1.87	-2.39	-2.45
2.688	3.09	-16.00	-3.44	-2.23	-2.12
3.12	3.15	-2.50	-1.56	-0.47	-0.67
3.108	3.97	-2.88	24.06	-0.62	-0.4
3.2	3.2	0.00	0.00	0.00	0.00
3.282	3.23	2.56	0.94	0.61	0.52
3.319	2.85	3.72	-10.94	1.30	1.70
3.3625	3.007	5.08	-6.03	1.54	2.54
3.403	2.58	6.34	-19.38	2.31	3.36
3.443	3.37	7.59	5.31	1.87	4.29
3.714	3.35	16.06	4.69	4.60	5.12

Table-4. Variation in power and delay due to deviation in gate oxide thickness for 75nm fabrication process technology.

$t_{ox\_n(m)}$	$t_{ox\_p\ (nm)}$	Deviation in t_{ox_n} (%)	Deviation in t_{ox_p} (%)	Deviation in power (%)	Deviation in delay (%)
1.2723	1.7354	-20.48	2.08	-3.18	-3.28
1.3584	1.6527	-15.10	-2.78	-2.24	-2.28
1.464	1.6713	-8.50	-1.69	-1.16	-1.26
1.5834	2.1257	-1.04	25.04	0.12	0.18
1.6	1.7	0.00	0.00	0.00	0.00
1.6426	1.7317	2.66	1.86	1.21	1.35
1.6576	1.5263	3.60	-10.22	1.75	1.65
1.6875	1.5978	5.47	-6.01	2.45	2.56
1.7212	1.3743	7.58	-19.16	3.54	3.64
1.7425	1.784	8.91	4.94	4.70	4.81
1.864	1.7724	16.50	4.69	6.71	7.12

Table-5. Variation in power and delay due to deviation in gate oxide thickness for 45nm fabrication process technology.

t_{ox_n} (nm)	t_{ox_p} (nm)	Variation in t_{ox_n} (%)	Deviation in t_{ox_p} (%)	Deviation in power (%)	Deviation in delay (%)
0.5465	0.71	-20.48	2.08	-14.20	-16.20
0.5923	0.6461	-15.10	-2.78	-10.57	-11.32
0.6731	0.643	-8.50	-1.69	-1.64	-2.63
0.6872	0.865	-1.04	25.04	-0.59	-1.42
0.7	0.7	0.00	0.00	0.00	0.00
0.7284	0.7184	2.66	1.86	1.84	1.94
0.717	0.6212	3.60	-10.22	2.78	2.76
0.739	0.667	5.47	-6.01	3.69	4.69
0.7542	0.5673	7.58	-19.16	4.74	5.62
0.7734	0.7487	8.91	4.94	5.17	6.27
0.872	0.773	16.50	4.69	10.84	11.28

Tables 4, 5 and 6 specify the NMOS gate oxide thickness (t_{ox_n}), PMOS gate oxide thickness (t_{ox_p}), percentage variation in t_{ox_n} and t_{ox_p}, percentage variation in power and delay for 130nm, 75nm and 45nm process technologies respectively. Figure-8 and Figure-9 shows percentage change in power and delay respectively, of FSGDI Wallace tree multiplier with deviation in gate oxide thickness.

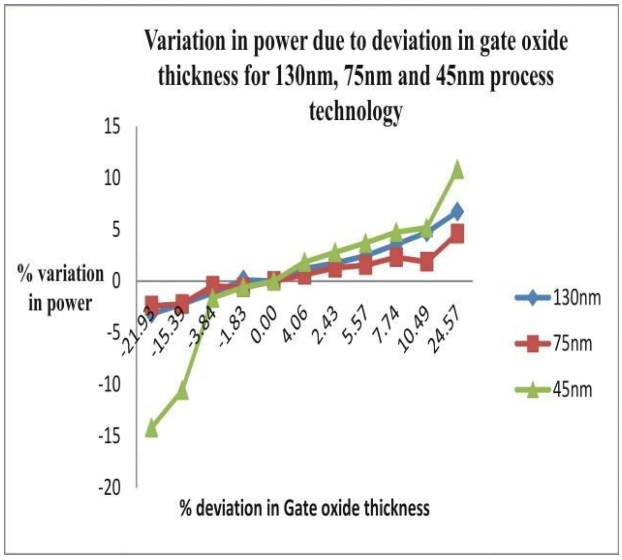

Figure-8. Percentage change in power with percentage deviation in gate oxide thickness (tox_n).

It is observed that the variation in power ranges from -2.39% to 4.60% for 130 nm technology, from -3.18% to 6.71% for 70 nm technology and 14.20% to 10.84% for 45 nm technology. The variation in delay ranges from -2.45% to 5.12% for 130 nm technology, from -3.28% to 7.12% for 70 nm technology and 16.28% to 11.24% for 45 nm technology. It is observed that as transistor size reduces the change in performance due to change in process variations become more significant.

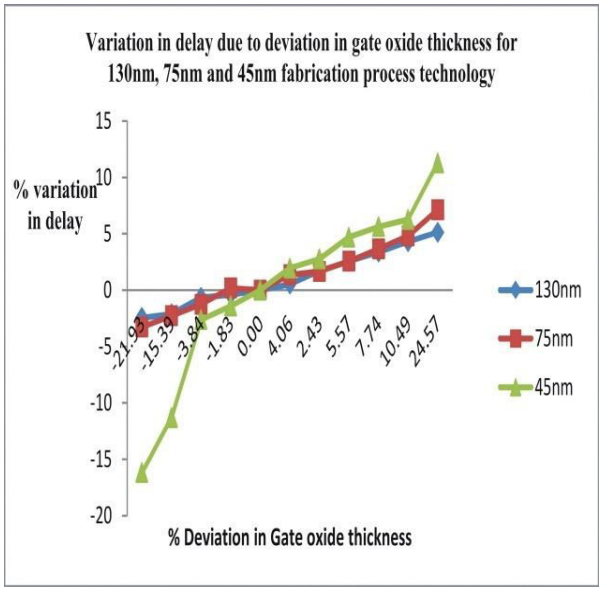

Figure-9. Percentage change in delay with percentage deviation in gate oxide thickness (tox_n).

CONCLUSIONS

FSGDI offers a promising future for low power VLSI design due its significant advantages of reduced power and area. This paper has proposed the design and implementation of FSGDI Wallace tree multiplier, which is a beneficial alternative to its equivalent CMOS design.

It is highly essential to statistically evaluate designs to eliminate parametric yield loss. Hence, FSGDI Wallace tree multiplier was subjected to variations in process parameters such as channel length and gate oxide thickness. The analysis of process variations shows that, as transistor dimensions shrink, process variations become more significant and increases the variations in power and delay.

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