Self-aligned imprint lithography for top-gate amorphous silicon thin-film transistor fabrication

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(Received 12 February 2010; accepted 3 June 2010; published online 28 June 2010)

We developed self-aligned imprint lithography (SAIL) for top-gate amorphous silicon (a-Si) thin-film transistors (TFTs). Our SAIL process enables a device pattern definition in a single imprint step that uses a three-level mold. The various levels of the mold are defined by a stepwise opening of a chromium hardmask and subsequent dry-etching. For TFT fabrication we imprint, and consecutively etch the imprint resist levels and device layers. The imprinted top-gate a-Si TFTs have nickel silicide source/drain self-aligned to the gate with mobilities of $\sim$0.4 $cm^2/V\,s$. © *2010 American Institute of Physics*. [doi:10.1063/1.3457446]

Active-matrix thin-film transistor (TFT) backplanes are the building blocks for electronic systems on large-area and flexible substrates, which may range from displays to x-ray sensor arrays to electronic paper and e-textiles.[1–3] Fabricating devices on large, flexible substrates requires overlay alignment of successive device layers on surfaces that undergo nonuniform dimensional changes, from thermal shrinkage, deformation, or mechanical strain.[4] The need for precise alignment has encouraged the introduction of self-aligned photolithographic processes for the fabrication of amorphous silicon (a-Si) TFTs.[5,6]

To keep the cost of large-area circuitry on flexible substrates low, eventually roll-to-roll (R2R) processes based on imprint lithography must be used.[7,8] These require even more advanced approaches to self-alignment. A particularly attractive technique is the self-aligned imprint lithography (SAIL) introduced by Mei *et al.*[9,10] SAIL is applied to conventional bottom-gate transistors, which dominate TFT backplanes. Top-gate TFTs with competitive performance have been demonstrated recently.[11] With their minimal overlap between gate and source/drain (S/D) electrodes and potentially short channels, these offer an attractive alternative for high-speed, low-power TFT circuitry,[12] and make step coverage less demanding.[13]

Therefore we introduce a SAIL process for the fabrication of top-gate TFTs that can be employed in R2R processing on large, flexible substrates. First we describe the mold design and fabrication. Then we fabricate top-gate a-Si TFTs by SAIL.

In SAIL, a multilevel mold encodes the geometric information of all device layers, including their alignment, in a three-dimensional imprinted mask. Each elevation is the equivalent of a photolithographic mask. Thus all mask levels are transferred in a single imprinting step. SAIL has an additional advantage; any deformation or distortion of the substrate during processing will equally affect all device layers and the imprinted mask, preserving layer-to-layer alignment. SAIL will eventually enable the fabrication of devices with submicrometer channel lengths on large, dimensionally unstable substrates.

A mold creating a three-level resist topography is sufficient for the definition of our top-gate TFT structure by SAIL, which means a reduction by one level from bottom-gate devices. Layout and fabrication steps of the three-level mold are summarized in Fig. 1. The mold material is a 1.1-μm-thick silicon dioxide (SiO_2) layer, deposited on a 1.1-mm-thick Corning 1737 glass slide by plasma-enhanced chemical vapor deposition (PECVD), and then coated with

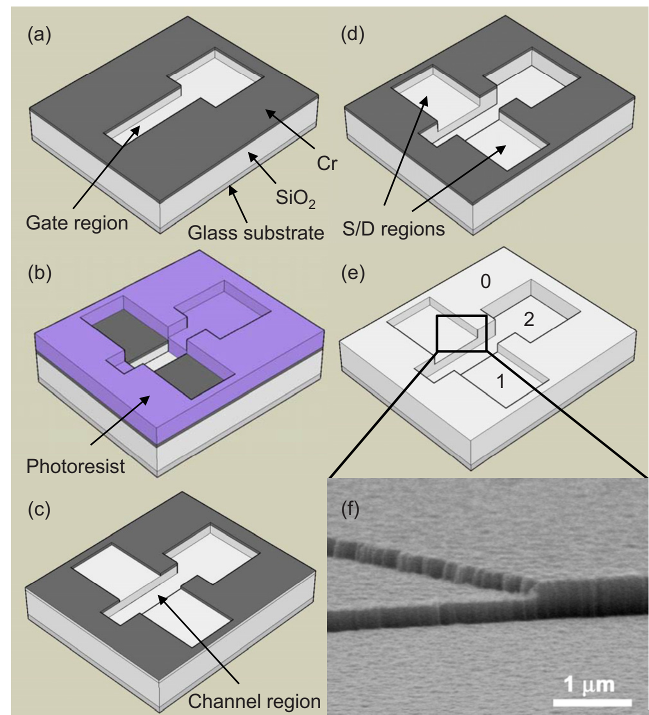

FIG. 1. (Color online) Three-level mold fabrication. Source (S) and drain (D) structure is self-aligned to the gate structure for the pattern definition of the top-gate a-Si TFT. The mold blank is a 1.1-μm-thick SiO_2 layer on a glass substrate covered by 60 nm Cr. (a) First photolithography and RIE step defines the gate. (b) Second photolithography defines S and D. (c) Removal of photoresist (note that the Cr layer defines now both S/D and gate). (d) Second RIE step etches S/D and gate structures simultaneously. (e) Removal of Cr layer by wet-etching to expose final three-level mold. (f) Scanning electron microscopy image of the three levels on the mold at the S/D and gate cross-over, as indicated by the black rectangle in (e).

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60 nm thermally evaporated chromium (Cr). The three-level relief of the mold is realized by a stepwise, wet-chemical removal of Cr areas defined by photolithography and subsequent reactive-ion etching (RIE) of the exposed SiO_2. The first pattern transfer defines the gate structure [Fig. 1(a)]. The SiO_2 is etched with a CF_4:H_2 plasma, optimized for vertical sidewalls.[11] The first etch depth is d_1. The second photolithography defines the S/D areas [Fig. 1(b)]. During the RIE transfer of this second mask layer to an etch depth d_2, the Cr free regions defined in the first lithographic step remain unprotected [Fig. 1(c)]. Thus, after the second etch step, the structures defined by the first pattern transfer are etched to a total depth of d_1+d_2 [Fig. 1(d)], where d_1 and d_2 are typically 350 nm each. This Cr hardmask approach guarantees perfect alignment (=self-alignment) of S/D to gate boundaries. Finally, the remaining Cr layer is wet-chemically etched off the mold surface [Fig. 1(e)]. The scanning electron micrograph in Fig. 1(f) shows the three levels of the mold, demonstrating the cross-over of the gate and S/D structures with vertical sidewalls and gapless intersection. Prior to imprinting, the mold surface is made hydrophobic by spin-coating the BGL-GZ-83 antisticking layer, which facilitates an easy, nondestructive release of the mold from the resist.[14] The mold is now ready for use.

We start SAIL device fabrication by depositing the TFT stack on a 1.1-mm-thick Corning 1737 glass slide by PECVD. The device layers are deposited without breaking the vacuum in a four-chamber PECVD system at pressure and temperature of 500 mTorr and 250 °C, respectively. First the 100 nm intrinsic a-Si channel layer is deposited from SiH_4. Then the 180 nm SiN_x gate dielectric layer is deposited from a gas mixture of SiH_4:NH_3. Finally, 40 nm Cr gate metal are thermally evaporated.

A NX-2000 nanoimprinter imprints the three-level mold at about 14 bar into a spin-coated, photocurable resist, followed by UV exposure. The three-level resist topography defines the field insulator, S/D, and gate regions. Homogeneous imprints, each containing 256 TFT structures, are achieved over the entire mold area of 1.5×1.5 in.^{2}.

Pattern transfer into the deposited TFT stack starts with the etching of the residual resist layer at level 0, exposing the field insulator [Fig. 2(a)]. The ability of anisotropically etching the resist is of crucial importance to keep pattern fidelity during SAIL processing. Therefore we use the silica-based NXR-2010 resist (Nanonex) and a CHF_3 plasma at low gas flow, pressure and power. TFTs are isolated by RIE of all three device layers, using the remaining resist levels 1 and 2 as etch mask [Fig. 2(b)]. First the Cr layer is removed by a short O_2 descum and a subsequent Cl_2:O_2 plasma etch, followed by a 4 min water rinse to reduce metal chloride content on the exposed SiN_x surface.[15] Then the SiN_x layer is etched in a CF_4:O_2 plasma. Finally, the a-Si is plasma etched in SF_6 and CCl_2F_2.

For S/D and gate stack definition (Cr gate metal and SiN_x gate dielectric), the imprint resist is thinned down by a CHF_3 plasma to expose the Cr layer in the S/D area [Fig. 2(c)]. Now the Cr layer is removed by using level 2, containing the gate information, as etch mask [Fig. 2(d)]. Note, that SAIL needs no further pattern definition step for S/D to gate alignment. After stripping the imprint resist, the SiN_x that covers the a-Si in the S/D area is etched by using the Cr gate as hard etch mask [Fig. 2(e)]. To prevent underetching of the

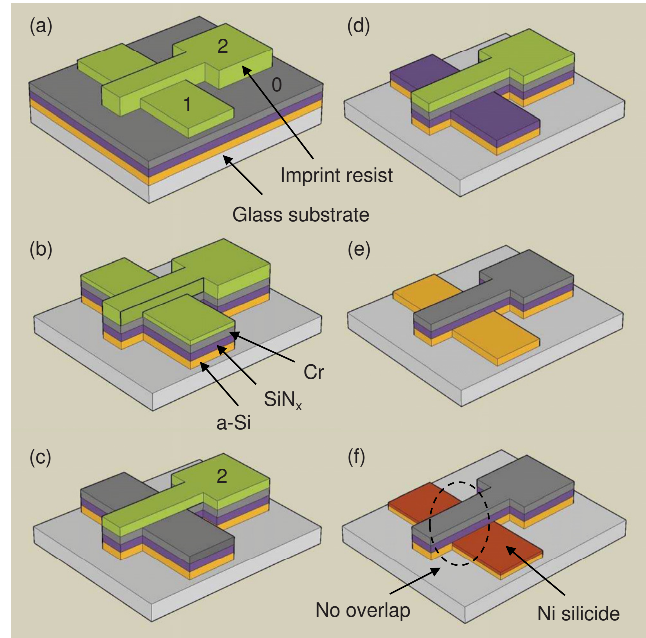

FIG. 2. (Color online) TFT fabrication by SAIL. The top-gate a-Si TFT has Ni silicide S/D self-aligned to the gate. (a) Three-dimensional imprinted mask on top of the TFT stack after residual resist layer etch at level 0. (b) Electrical separation of TFTs (=field insulation) by RIE. (c) Thinning of the imprint resist to expose level 2. (d) Etching of Cr layer in S/D area. (e) Removal of imprint resist and anisotropic SiN_x etch. (f) Blanket deposition of Ni, silicidation step and selective removal of unreacted Ni to expose the finished TFT.

SiN_x gate dielectric, the CF_4:H_2 plasma is optimized for vertical sidewalls.[11] Underetching breaks the electrical contact between S/D and the accumulation layer in the channel. Finally, a 30 nm nickel (Ni) layer blanket is deposited. It reacts to Ni silicide with the intrinsic a-Si of the S/D area during an anneal step at 280 °C in N_2 ambient for 1 h 30 min. The unreacted Ni is removed in a wet-etch of HNO_3:HCl:H_2O =1:5:3 [Fig. 2(f)]. Due to the vertical SiN_x gate dielectric sidewalls, the Ni silicide S/D electrodes are perfectly aligned (=self-aligned) to the gate. Ni was chosen because the silicidation temperature of 280 °C is compatible with several plastic substrates for flexible electronics.[16–18]

The top-gate TFTs are Schottky-contact devices. Such devices, fabricated by standard photolithography, were characterized and described in detail in Ref. 11. Our SAIL defined transistors have gate widths (W) and lengths (L) ranging from 10 μm to 160 μm and 5 μm to 80 μm, respectively. The inset of Fig. 3 shows an optical micrograph of the top-gate TFT. The dc transfer characteristics of an a-Si top-gate TFT with W/L=80 μm/40 μm is shown in Fig. 3. The drain and gate currents, I_{DS} and I_{GS}, are plotted versus the gate voltage V_{GS} at drain voltages of V_{DS}=0.1 and 10 V. The device exhibits the characteristics typical of an enhancement mode MOS transistor with an I_{ON}/I_{OFF} ratio of $\sim5\times10^4$. From the transfer characteristics measured at V_{DS} =10 V a linear mobility of ~0.4 cm^2/V s is obtained. The voltage shift in the transfer curves evident from Fig. 3 suggests substantial charge trapping at the SiN_x/a-Si interface. Most likely the charges are trapped at defects that may have been introduced during PECVD of the SiN_x insulator atop the a-Si channel layer, or during the plasma etch processes for device definition. The current noise is a consequence of gate leakage current along the insulator sidewalls. Device

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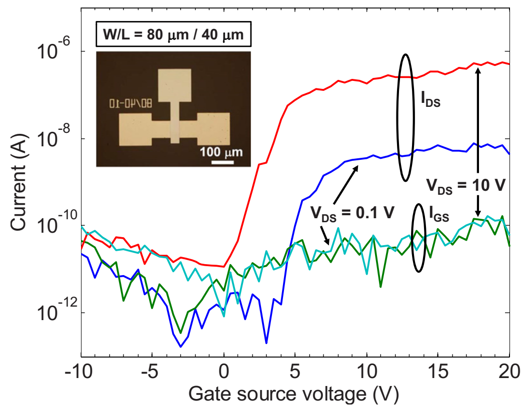

FIG. 3. (Color online) Room temperature dc transfer characteristics [drain source current (I_{DS}) and gate source current (I_{GS}) vs gate source voltage (V_{GS}) measured at drain source voltages V_{DS} of 0.1 and 10 V] for a top-gate a-Si TFT fabricated by SAIL. Inset shows an optical micrograph of a top-gate TFT with W/L=80 μm/40 μm.

yield was about 20%. While Fig. 3 clearly demonstrates the feasibility of SAIL for top-gate a-Si TFT fabrication, the device performance must be improved for practical application. At present we are studying an alternative material for gate insulator, with the goal of reducing defect density and edge current, and thereby increase TFT performance and yield.

We have designed and fabricated a multilevel imprint mold in a two-step photolithography and RIE process. We use this mold for SAIL fabrication of top-gate a-Si TFTs with Ni silicide S/D self-aligned to the gate. The inherent self-alignment of sequentially patterned device layers by SAIL and the low processing temperatures make the presented process transferable to a fabrication on flexible plastic substrates. The concept of encoding multiple structural information into a single imprint mold for dimensionally unstable substrates clearly expands the perspective of imprint lithography.

This work was partially supported by the NILquantumdot project of the NILaustria project cluster (FFG project number 815803, www.nilaustria.at) through the Austrian NANO Initiative (bmvit and FFG, www.nanoinitiative.at). E.L. thanks the Austrian Fellowship Organizations of the University of Linz for financial support of her research stay and gratefully acknowledges the hospitality at Princeton University.

[1] R. A. Street, R. L. Weisfield, R. B. Apte, S. E. Ready, A. Moore, M. Nguyen, W. B. Jackson, and P. Nylen, Thin Solid Films **296**, 172 (1997).
[2] Y. Chen, J. Au, P. Kazlas, A. Ritenour, H. Gates, and M. McCreary, Nature (London) **423**, 136 (2003).
[3] H. E. A. Huitema, G. H. Gelinck, J. B. P. H. van der Putten, K. E. Kuijk, C. M. Hart, E. Cantatore, P. T. Herwig, A. J. J. M. van Breemen, and D. M. de Leeuw, Nature (London) **414**, 599 (2001).
[4] I.-C. Cheng, A. Kattamis, K. Long, J. C. Sturm, and S. Wagner, J. Soc. Inf. Disp. **13**, 563 (2005).
[5] J. I. Ryu, H. C. Kim, S. K. Kim, and J. Jang, IEEE Electron Device Lett. **18**, 272 (1997).
[6] I.-C. Cheng, A. Z. Kattamis, K. Long, J. C. Sturm, and S. Wagner, IEEE Electron Device Lett. **27**, 166 (2006).
[7] S. H. Ahn and L. J. Guo, Adv. Mater. (Weinheim, Ger.) **20**, 2044 (2008).
[8] S. Y. Chou, P. R. Krauss, W. Zhang, L. Guo, and L. Zhuang, J. Vac. Sci. Technol. B **15**, 2897 (1997).
[9] P. Mei, W. B. Jackson, C. P. Taussig, and A. Jeans, U. S. Patent No. 7056834 B2 (June 6, 2006).
[10] H.-J. Kim, M. Almanza-Workman, A. Chaiken, W. Jackson, A. Jeans, O. Kwon, H. Luo, P. Mei, C. Perlov, and C. Taussig, IMID/IDMC '06 DIGEST, invited paper (2006).
[11] Y. Huang, B. Hekmatshoar, S. Wagner, and J. C. Sturm, IEEE Electron Device Lett. **29**, 737 (2008).
[12] J. P. Lu, P. Mei, J. Rahn, J. Ho, Y. Wang, J. B. Boyce, and R. A. Street, J. Non-Cryst. Solids **266–269**, 1294 (2000).
[13] S. Martin, C.-S. Chiang, J.-Y. Nahm, T. Li, J. Kanicki, and Y. Ugai, Jpn. J. Appl. Phys., Part 1 **40**, 530 (2001).
[14] The BGL-GZ-83 antisticking layer was developed at Profactor GmbH. During spin-coating of the fluorinated solution, the solvent evaporates and a thin, hydrophobic layer is formed on the mold surface. Further information can be obtained from Profactor GmbH (http://www.profactor.at/en/nano/produkte-verfahren-lizenzierbares/bgl-gz-83.html).
[15] D. Y. Choi, J. H. Lee, D. S. Kim, and S. T. Jung, J. Appl. Phys. **95**, 8400 (2004).
[16] W. A. MacDonald, J. Mater. Chem. **14**, 4 (2004).
[17] K. Long, A. Z. Kattamis, I.-C. Cheng, H. Gleskova, S. Wagner, and J. C. Sturm, IEEE Electron Device Lett. **27**, 111 (2006).
[18] K. H. Cherenack, A. Z. Kattamis, B. Hekmatshoar, J. C. Sturm, and S. Wagner, IEEE Electron Device Lett. **28**, 1004 (2007).

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