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Automatic control of AC bridge-based capacitive strain sensor interface for wireless structural health monitoring

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ABSTRACT

Thin film-based flexible strain sensors have various advantages for structural health monitoring (SHM) because of their capability to sustain large deformations and cover large area of structural surfaces, making them ideal candidates for applications to complex geometries and structural crack monitoring. The authors previously developed a flexible strain sensor technology based on a soft elastomeric capacitor (SEC) for SHM and investigated an alternating current (AC) bridge-based method to transform the strain-induced dynamic capacitance changes in the SEC into analog voltage signals. Previous experiments have verified the capability of the SEC and the AC bridge-based signal converter for structural strain sensing applications. However, careful manipulation requirement for precise AC-bridge balancing, signal amplification control, and shunt calibration limits its practical use for full-scale SHM in field conditions. This study addressed such limitations with critical updates in both hardware and software with fully automated features for high-sensitive capacitive strain sensing. Newly developed hardware and software are fully controlled with a low-cost microcontroller ATmega328p in an automated way. A series of lab tests validated the prototype's performances in the capacitive strain sensing, outperforming an off-the-shelf wired capacitance measurement system (about 34% lower measurement noise), and confirmed that automatic control features worked as designed.

1. Introduction

Large area strain sensing has received significant attention in the structural health monitoring (SHM) research community due to its distinct advantage over conventional foil-type strain gauges. A conventional foil-type strain gauge typically covers a few to tens of square millimeters, hence cannot effectively reflect mesoscale structural behaviors [1–4]. Indeed, traditional small-size sensors have difficulties in distinguishing between global and local structural property variations when the sensors are applied to large systems, such as bridges, buildings, and wind turbines. In this regard, large-area sensing technologies have been widely investigated for SHM applications. The large sensing coverage can better represent mesoscale structural behaviors with distributed dense sensor networks [2,5,6]. Various large-area sensors have already been developed, including carbon nanotube-based sensors [7], resistive sensor sheets [8], printable conductive polymer [9], and soft elastomeric capacitive (SEC) sensors [2]. These sensors allow covering the mesoscale structural surface with a discrete number of sensors to enable direct damage detection and localization [10]. Among these sensors, the SEC is a flexible skin-type strain sensor that offers various advantages for SHM applications: large coverage, low cost, high sensitivity, ultra compliance, customizable geometry, and robustness. The performance of static and dynamic strain sensing capability of the SEC has been validated for steel and concrete structures via laboratory and field tests [5,10,11]. Moreover, the damage detection capabilities of SEC have been investigated, including for steel structure fatigue crack

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monitoring [10,12], concrete damage detection [6], and wind turbine damage detection [5]. However, conventional wired data acquisition for such capacitive strain sensors hinders its extended use for large-scale SHM applications.

Wireless smart sensors (WSS) are an attractive solution for SHM in that they enable wireless communication among sensor nodes distributed over large-scale structural systems without costly cabling [13]. Various sensing hardware & software systems have been developed for accelerometer and resistive strain gauge sensing and validated over full-scale implementations [14,15]. However, capacitance-based strain sensing methods have not benefited from these advantages of WSS networks for SHM.

A recent research has developed an analog De Sauty bridge-based wireless capacitive strain sensor board (c-strain sensor board) that demonstrated extremely low-level capacitive strain sensing capability in a wireless manner [1]. It was successfully integrated with the high-fidelity smart sensing platform Xnode that provides various functionalities for high-sensitivity wireless SHM; Xnode functions include a solar-powered battery, low power consumption, 3.3 V power supply, onboard signal processing, wireless communication, and 24-bit analog-to-digital conversion. The static and dynamic strain sensing sensitivity of the developed c-strain sensor board was validated via a series of lab tests. However, several practical limitations remain to be resolved for large-scale field implementations. The c-strain sensor board comprises full analog circuits; AC-bridge balancing, amplification, and a two-step shunt calibration process are required be done manually with an oscilloscope for high-frequency AC signal control prior to actual deployment for sensing to ensure high-quality measurement. However, such manual setup with the oscilloscope is cumbersome and is challenging in field conditions. Also, field engineers should have background knowledge of such sensor board pre-setup, such as precise AC bridge balancing and shunt calibration procedures, which is not desirable. Some studies has developed the automated AC bridge balancing techniques for easy capacitance sensing applications [16,17]. However, none of these approaches deals with automated amplification and shunt calibration required for wireless SHM applications.

This study presents the development of a fully automated c-strain sensor board for wireless SHM applications, which can interface with the Xnode wireless sensor platform to be used under its 3.3 V power for a measurement range of 0–2.4 V. While keeping the basic capacitance measurement framework of the analog c-strain sensor board, we developed a low-cost microcontroller-based automated AC bridge balancing, amplification, and shunt calibration method. Peak-detection circuits and a 16 bit ADC were employed to read the peak voltages of the high-frequency AC signals. Digital potentiometers, digital bus switch, and an 8-bit microcontroller were employed to control the AC bridge balancing, signal amplification, and two-step shunt calibration. Embedded software was developed for automated control of the digital components. A prototype of the new sensor board was produced, and the performance was validated via lab tests and compared with a commercial wired capacitance measurement system.

2. Fully automated capacitive strain sensor board design

The research objectives include measuring low-level structural strains using the SEC by converting the capacitance variation of SEC into analog voltage signal in a fully automated manner. We designed the new sensor board under the following requirements: i) integration with the existing wireless smart sensing (WSS) platform Xnode, ii) high-sensitivity capacitive strain sensing, and iii) fully automated bridge balancing, amplification, and shunt calibration. Fig. 1 shows the block diagram for the new sensor board, which illustrates the fully automated capacitance sensing procedure interfacing with the Xnode platform. The basic signal processing followed the AC bridge based analog capacitance sensing system developed by [1] that is consists of AC signal excitation, AC De sauty bridge balancing, two-step amplification, AM demodulation, and two-step shunt calibration. The full analog sensor board required manual ajustment and tunning [1]. In contrast, the new sensor board employs digitally controlled parts and their associated circuits, microcontroller unit (MCU), and embedded software for fully automated operations. Analog potentiometers and a manual switch are replaced by a digital potentiometer and a field-effect transistor (FET) bus switch controlled by the MCU. Direct control of the high-frequency AC signal by MCU is not desired for wireless sensing systems due to its intensive computational requirements. To this end, an alternative AC signal control method is developed using a peak-detection circuit and a newly developed algorithm.

2.1. Soft elastomeric capacitor

An SEC is a flexible skin-type large-area capacitor transducing geometric changes (i.e., area and thickness) into measurable capacitance changes. The SEC has distinct advantages for mesoscale monitoring in civil structures with its large surface coverage, mechanical robustness,

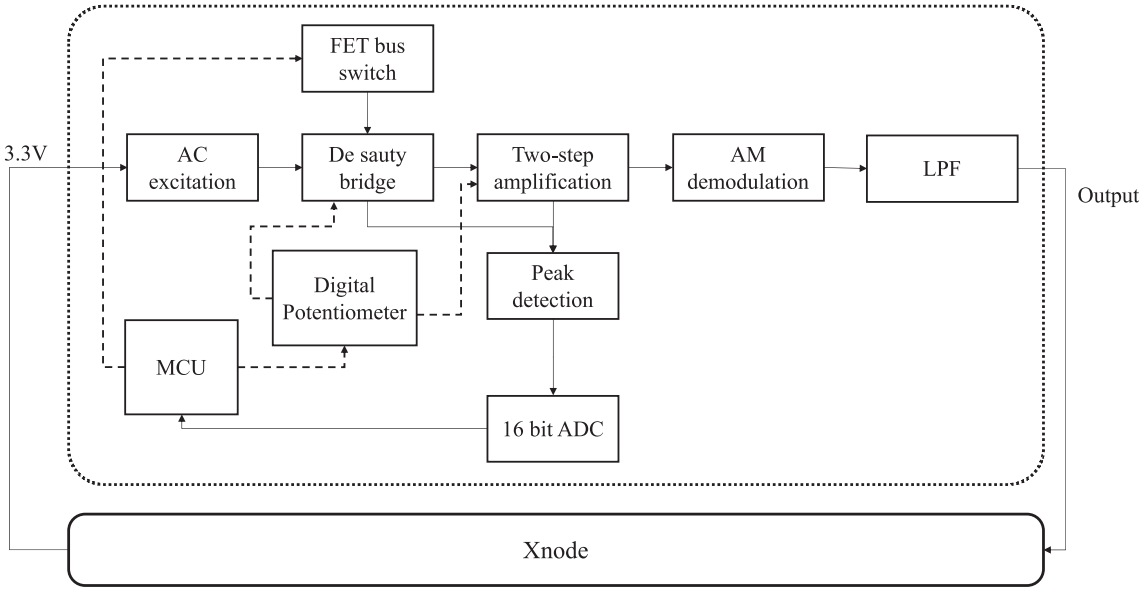


Fig. 1. Block diagram for capacitive sensing module.

ultra material compliance, and high sensitivity. Recent studies demonstrated the performance of the SEC for various SHM applications, including steel fatigue crack monitoring, concrete damage detection, and large area strain field monitoring. Details on the SEC technology can be found in [18].

A recent study developed the corrugated SEC (cSEC) with surface patterns shown in Fig. 2. It is an improvement to an earlier version of an SEC without a textured pattern to improve sensing capability for various aspects, including linearity, sensitivity, resolution, and accuracy. The new corrugated SEC improved signal accuracy and linearity up to 30% strain [19]. The improved performance was validated via a laboratory experiment monitoring the low-cycle fatigue damage on notched steel compact specimens. The basic principle of capacitance change corresponding to geometric change can be expressed as:

$$C = \frac{\varepsilon_0 \varepsilon_M A}{d}$$

where ε_0 is the vacuum permittivity, ε_M is the relative permittivity of the dielectric, A is the electrode area, and d is the thickness of the dielectric. The detailed sensing principle can be found in [4]. In this study, corrugated SECs measuring 3 × 3 in (7.6 × 7.6 cm) and covering 9 in^2 (57.76 cm^2)were used for validation.

2.2. Design considerations: Interface with high-fidelity wireless sensing platform – Xnode

The new sensor board was developed to interface with a commercial wireless smart sensing platform Xnode, which provides the most advanced hardware & software features for wireless SHM applications available on current market, enabling wireless capacitive strain sensing. The Xnode has a powerful dual-core CPU (ARM cortex M0/M4), 24 bit ADC (ADS131E8), low-power wireless radio transceiver (Atmel AT 86RF233), SD data storage, triaxial accelerometer, three-channel strain Wheatstone bridge, five additional analog voltage input channels, and 4G LTE module (Sierra Wireless HL7588 LTE-CAT4) for data transfer to cloud storage. The Xnode uses a software framework based on the Illinois Structural Health Monitoring Project (ISHMP) services Toolshuite, providing various functionality for robust wireless SHM applications [13]. The Xnode has demonstrated its performance via various full-scale SHM projects [20,21].

Particularly, the sensor board hardware is designed to be compatible with the Xnode hardware system. All parts and circuits were selected and designed to be powered by the Xnode's regulated 3.3 V voltage supply, and the sensor board output was adjusted to meet the measurement range (i.e. 0–2.4 V) of the Xnode's 24bit ADC after onboard signal conditioning. Fig. 3 shows a schematic of the new sensorboard and Xnode interface configuration. As shown in Fig. 3, the Xnode has two types of nodes in the network; leaf node roles in measuring structural response data from the target structures and transmitting data to the gateway node. The gateway node manages the whole sensor network by scheduling and triggering the network operation, collecting the measurement data from leaf nodes, transmitting the collected data to cloud storage. The Fig. 3 configuration has been successfully demonstrated in field conditions in the recent study [22] and the new sensorboard was also designed in the same compliance with the former system [1].

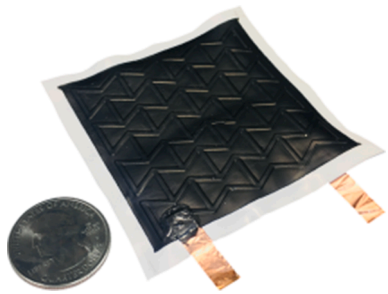


Fig. 2. Corrugated Soft elastomeric capacitor (cSEC).

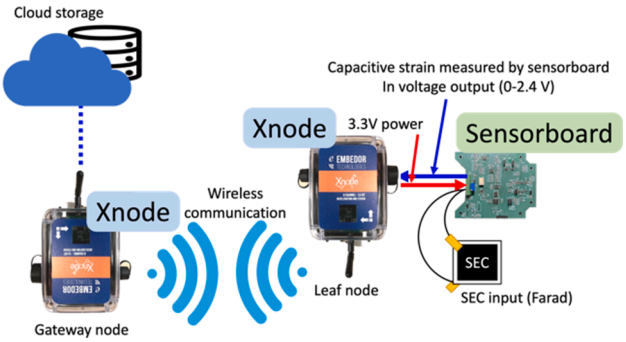


Fig. 3. Sensorboard and Xnode interface configuration.

2.3. AC De sauty bridge & amplifiers

The AC De sauty bridge balancing and the two-step signal amplification are the two major parts for high-sensitivity capacitive strain sensing proposed in this study. The bridge balancing should be designed precisely and proper amplification is required to ensure the maximum sensitivity without saturation. The high-frequency AC signal (V_{in}, OSC) was excited using a 32.768 kHz square wave oscillator and converted to sine wave using a fourth-order Sallen-key filter. The AC bridge with two resistors and two capacitors known as the De sauty bridge was used. It requires two potentiometers for bridge balancing and a dual step amplification stage for gain control. There are various kinds of automated De sauty bridge balancing techniques that have been developed utilizing voltage-controlled resistor (VCR) and feedback loop circuits [16]. We employed a four-channel non-volatile digital potentiometer (AD5254 with 256-tabs 100 kΩ 4 CH, Analog devices) to directly control the bridge balancing and amplification via a microcontroller. Fig. 4 shows the detailed schematic diagram of the De sauty bridge, amplifiers, peak detection circuit, 16-bit ADC, and MCU. The digital potentiometer directly adjusts four resistances ($R_{1\ 4}$) for bridge balancing and amplifications.

The balanced bridge configuration status is obtained when $R_2/R_1 = C_1/C_2$. C_1 is the nominal capacitance of the SEC (DUT, device under test) and C_2 is the reference capacitor. Two AC signals from the De sauty bridge and two AC signals from the two-step amplifiers (AD8226, Analog Devices), total of four AC signals are fed to the peak detection circuit shown in Fig. 5, which detects AC peak voltages. A total of four peak detection circuits were employed to detect AC peaks separately, targeting the 0–40 Hz frequency bandwidth. The four signals are fed into

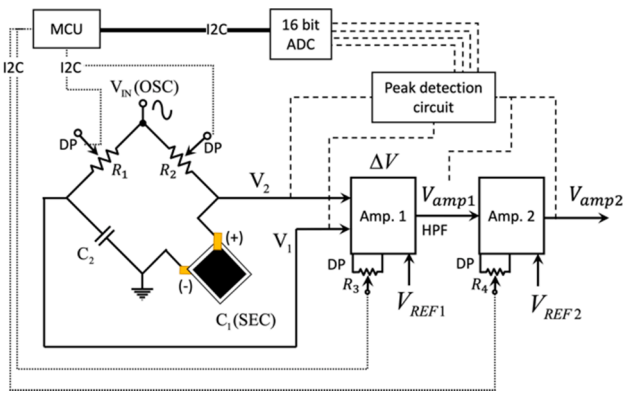


Fig. 4. Fully automated De sauty bridge and two-step amplification design.

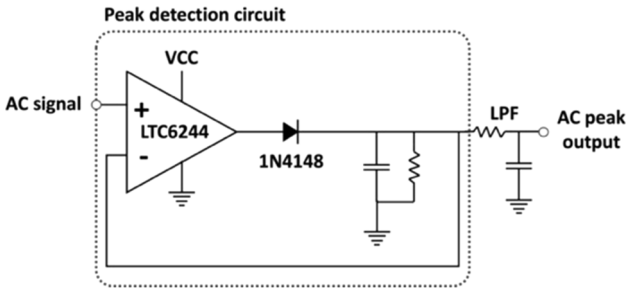


Fig. 5. Peak detection circuit.

a 16-bit analog-to-digital converter (ADS1115, Texas Instruments) for precise peak voltage detection from the MCU with 0.1 mV resolution (i.e., ADS1115 has 15-bit effective resolution). Fig. 6 shows an example of peak detection output that the peak of AC signal was precisely detected. The peak signals are feed to the ADC for precise voltage monitoring. A software was developed for automated bridge balancing and amplification, which will be discussed in section 3.

The voltage difference from the De sauty bridge (i.e. $V_2 - V_1$), which was induced by the variation of SEC capacitance $C_1^{'} = C_1 + \Delta C$, can be expressed as:

$$V_{test} = V_2 - V_1 = V_{in}\left(\frac{\frac{1}{j\omega C_2}}{R_2 + \frac{1}{j\omega C_2}} - \frac{\frac{1}{j\omega(C_1+\Delta C)}}{R_1 + \frac{1}{j\omega(C_1+\Delta C)}}\right) \quad (1)$$

Eq. (1) can be rearranged to the following equation:

$$V_{test} = V_{in}\left(\frac{j\omega(C_1R_1 - C_2R_2) + j\omega\Delta CR_1}{(1 + j\omega C_1R_1 + j\omega\Delta CR_1)(1 + j\omega C_2R_2)}\right) \quad (2)$$

Eq. (2) can be simplified by neglecting ΔC in the denominator, since the capacitance variation is very small compared to the nominal capacitances (i.e. C_1 and C_2) of the SEC and reference capacitor, and C_1R_1 - C_2R_2 is zero in the numerator when the bridge is balanced. Therefore, Eq. (2) can be approximated by the linear expression shown in the following equation:

$$V_{test} = V_2 - V_1 = V_{in}\left(\frac{j\omega R_1}{(1 + j\omega C_1R_1)(1 + j\omega C_2R_2)}\right)\Delta C \quad (3)$$

The maximized amplification is essential for high-sensitivity capacitive strain sensing. The voltage variation V_{test} by ΔC is amplified in the amplification stage. However, perfect balancing cannot be achieved in practice due to the parasitic capacitance, which leads the DC components in V_{test}. Therefore, a two-step amplification was employed with a high-pass filter between two amplification stages to maximize the sensitivity, expressed as:

$$V_{output} = G_2\{(G_1 \bullet V_{test} + V_{REF1}) - V_{HPF}\} + V_{REF2} \quad (4)$$

The digital potentiometer directly controls the gains for each amplification stage, and DC voltages are supplied via V_{REF1} and V_{REF2} to prevent saturation and control the output level.

2.4. AM demodulation and LPF

The amplitude of the amplified signal V_{output} represents the capacitance change ΔC. The AM demodulation circuit was employed to take the amplitude envelope targeting the frequency bandwidth 0–30 Hz based on the following equation (5).

$$\frac{1}{f} \ll \tau = RC \ll \frac{1}{\omega} \quad (5)$$

where f is the carrier frequency, τ is the RC circuit charging time, and ω is the message bandwidth. The enveloped signal is passed through a second-order active low pass filter (LPF) to clean the voltage output.

2.5. Two-step shunt calibration

Shunt calibration is a key step to convert the voltage output to the desired unit for Wheatstone bridge-based sensing applications. Particularly in this application, the capacitance is affected by the parasitic capacitance (Z_L) in the lead wires that connect the SEC and AC De sauty bridge, as shown in Fig. 7, of which the parasitic capacitance effect needs to be effectively considered for accurate calibration. A recent study introduced the two-step shunt calibration strategy to avoid parasitic capacitance effect [1]. In this study, a field-effect transistor (FET) bus switch (SN74CBT, Texas Instruments), which can handle multiple switch channels, was employed for the automated two-step shunt calibration procedure. The majority of digitally controllable switches, such as a bipolar junction transistor (BJT) and electro-mechanical relay, have a substantial parasitic capacitance, which is not negligible for this high-sensitivity measurement application. Indeed, each component has its own unknown parasitic capacitance; which may result in inaccurate shunt calibration, particularly when a serial connection effect with the shunt capacitor is expected. The multi-channel FET bus switch, selected for this application, has a low internal capacitance that is not prone to such an unknown parasitic capacitance effect.

The voltage-unit sensorboard output (i.e. ΔV) can be converted into capacitance unit (i.e. ΔC) by the following equation:

$$\Delta C = \left(\frac{C_{c1} - C_{c2}}{V_{C_{C1}} - V_{C_{C2}}}\right)\Delta V \quad (6)$$

where C_{c1} and C_{c2} are shunt capacitors with different capacitance values, $V_{C_{C1}}$ and $V_{C_{C2}}$ are the voltage levels measured from the two shunt calibration steps, respectively. The shunt calibration factor, which is the coefficient expression in the equation (6), can be obtained by dividing the shunt capacitors' value difference (i.e. $C_{c1} - C_{c2}$) by the measured

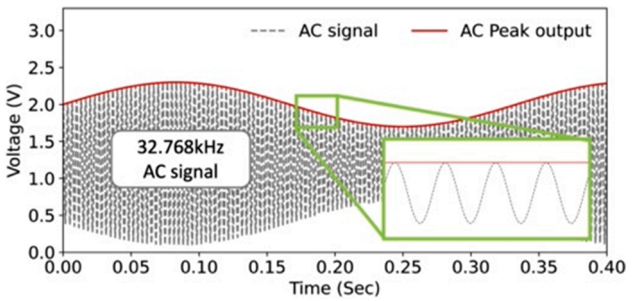


Fig. 6. Peak detection result.

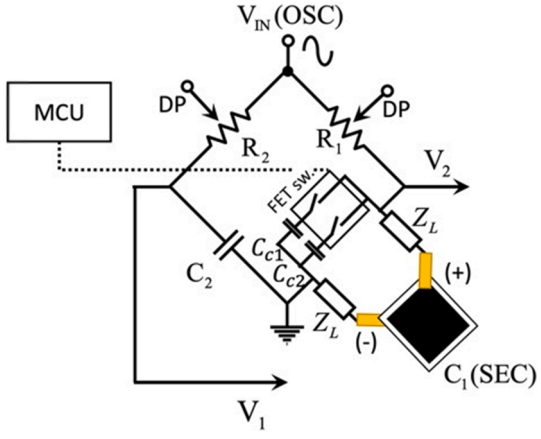


Fig. 7. Two-step shunt calibration diagram.

voltage difference (i.e. $V_{C_{C1}} - V_{C_{C2}}$) between each shunt steps.

The accuracy of the two-step shunt calibration using the FET bus switch was validated. The two capacitors were connected to the FET bus swich via parallel connection with a SEC having 870 pF nominal capacitance. The FET bus swich was controlled by a microcontroller (ATmega328P). The capacitance was measured using an off-the-shelf capacitance measurement toolkit PCAP02 for a reference evaluation. Fig. 8 shows the example test results of two cases using two pairs of shunt capacitors (i.e. 10 pF and 30 pF capacitors for case 1 and 10 pF and 47 pF capacitors for case 2) to demonstrate why two-step shunt calibration is required for the De sauty bridge-based capacitance sensing and validate if the selected FTE swich works as expected. For example, when the first 10 pF shunt capacitor was connected (i.e. 10 pF on and 30 pF off) to the SEC bridge arm in parallel in case 1, 27 pF capacitance increment was observed as shown in Fig. 8(a), while 10 pF increment was expected. This implies that unexpected additional 17 pF parasitic capacitance, which is the difference between 27 pF observation and 10 pF shunt capacitor, exists in the bridge circuit and lead wires. Similarly, when the second 30 pF shunt capacitor was connected in case 1 (i.e., 10 pF off, and 30 pF on), 47 pF increment was observed, which still includes the 17 pF parastic capacitance (i.e. 47 pF – 30 pF = 17 pF). However, the capacitance difference between the two shunt capacitors (i.e. 30 pF – 10 pF = 20 pF) exactly matched with the measurement difference (i.e. 47 pF – 27 pF = 20 pF), implying that two-step shunt calibration process is required to get rid of the parastic capacitance hidden in the bridge circuit and lead wires. The case 2 using different pair of shunt capacitors also showed the same-trend results as shown in Fig. 8 (b). When 10 pF and 47 pF shunt capacitors were used, the capacitance difference of 37 pF (i.e. 47 pF – 10 pF = 37 pF) exactly matched with the measurement difference (i.e. 64 pF – 27 pF = 47 pF), validating that the selected FET switch worked as expected with good accuracy for the two-step shunt calibration.

3. Fully automated bridge balancing, amplification, and shunt calibration software development

In addition to the hardware improvement, a new software framework was developed to implement the fully automated bridge balancing, signal amplification, and shunt calibration. The ATmega328P-AU (microchip) was used as a microprocessing unit (MCU). While the original clock speed is 16 MHz under a 5 V supply, the ATmega328P-AU was downclocked to 8 MHz to work under a 3.3 V supply with lower power consumption.

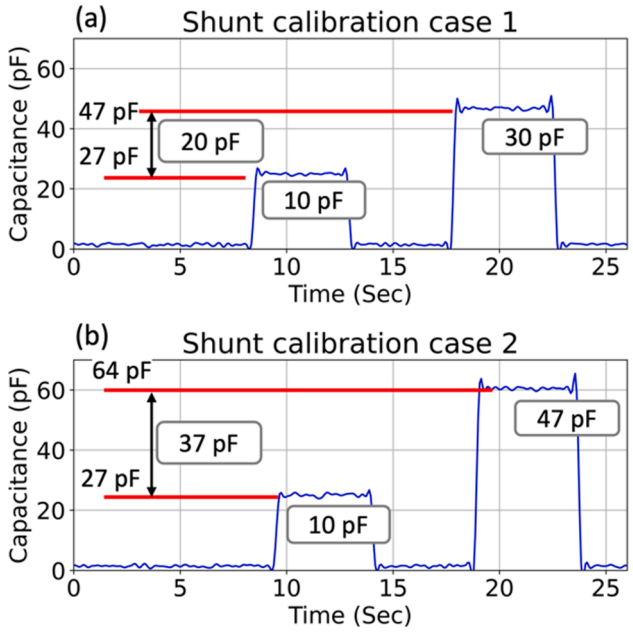


Fig. 8. FET switch bus validation for the proposed two-step shunt calibration (two example cases for demonstration).

Fig. 9 shows the flowchart of the fully automated De sauty bridge balancing, amplification, and shunt calibration procedures. When powered on, the ATmega328 MCU loads the initial potentiometer values. After initialization, the potentiometer tap on the SEC side changes n steps (i.e. n = searching range) while the one on the reference side is fixed. The searching range (i.e. **n** value) can be different depending on the possible capacitance difference between the reference capacitor and SEC. This study used n = 50 (out of 256 taps of the selected digital potentiometer), which was sufficient for covering up to about 5–10% capacitance difference. The peak amplitude of AC signals in the amplification stage significantly varies depending on the bridge balancing status.

$$V_{amp1} = G_1\{(V_{REF}sin(\alpha_1) - V_{SEC}sin(\alpha_2)) - V_{HPF}\} + V_{REF1} \quad (7)$$

$$V_{amp2} = G_2\{(V_{amp1}) - V_{HPF}\} + V_{REF2} \quad (8)$$

Due to parasitic impedance in the SEC and lead wire, achieving perfect balancing to have exactly the same amplitude and phase between $V_{REF}\sin(\alpha_1)$ and $V_{SEC}\sin(\alpha_2)$ is not possible. An AC component always exists, which represents the difference between the two AC signals from the De sauty bridge. Optimal balancing can be achieved when the amplitude difference (between V_{REF} and V_{SEC}) and phase difference (i.e., $\alpha_1 - \alpha_2$) in equation (7) are minimized. The peak voltage levels extracted from a peak-detection circuit of V_{amp1} and V_{amp2} can represent the bridge balancing quality. Once the optimal balancing is achieved, the signal amplification level is adjusted to the desired level. In this study, the amplified signal (V_{amp2}) is adjusted to have a 2 V peak level that may have sufficient amplification level and margin to the maximum measurable voltage range of Xnode.

In this study, the peak voltage of the second amplifier V_{amp2} is used as an indicator for the bridge balancing quality. The detailed procedures for the proposed automated bridge balancing, amplification, and shunt calibration are summarized as follows:

Step 1) Potentiometer tab initialized.
Step 2) Search optimal digital potentiometer (DP) tap (for SEC side) *n* times: update DP tab for SEC side, compare it with the current V_{amp2} and minimum peak amplitude (V_{opt}), and update V_{opt} and DP_{opt1} if $V_{amp2} < V_{opt}$.
Step 3) Adjust DP tab for SEC side to DP_{opt1}.
Step 4) Adjust V_{amp2} amplitude to maximize the sensitivity: update the DP tab for the second amplifier, compare it with the current V_{amp2} and desired peak voltage $V_{amp2_{out}}$ (i.e., up to 2.4 V, current setup: 2 V), update DP_{opt2} if $V_{amp2} < V_{opt}$.
Step 5) Adjust DP tab for the second amplifier to DP_{opt2}.
Step 6) Do two-step shunt calibration.

Fig. 10 visualizes the automated bridge balancing procedure described above by showing the changes of the AC signals from the De sauty bridge, Fig. 10(a), and the first & second amplifier, Fig. 10(b and c), as searching the optimal DP taps. As shown in the left figure of Fig. 10 (a), two signals from the reference side (red line, V_1 in Fig. 3) and SEC side (blue line, V_2 in Fig. 4, s1-initial setup) of the De sauty bridge are not matched (i.e. not balanced) in the beginning. Then the amplitude and phase of SEC side's signal (blue) changes according to DP tap changes (i: 0 → n) while updating V_{opt} and DP_{opt1}, as shown with the s2 and s3 in left figure of Fig. 10(a). After that, SEC side's DP tap is adjusted to DP_{opt1} (i.e. s2 in Fig. 10) as the optimally balanced setup because the best match is obtained between the two signals, which is the right figure of Fig. 10(a). Meanwhile, as the balancing status changes (s1-s2-s3), the amplitude of V_{amp2} (AC signal from the second amplifier) changes

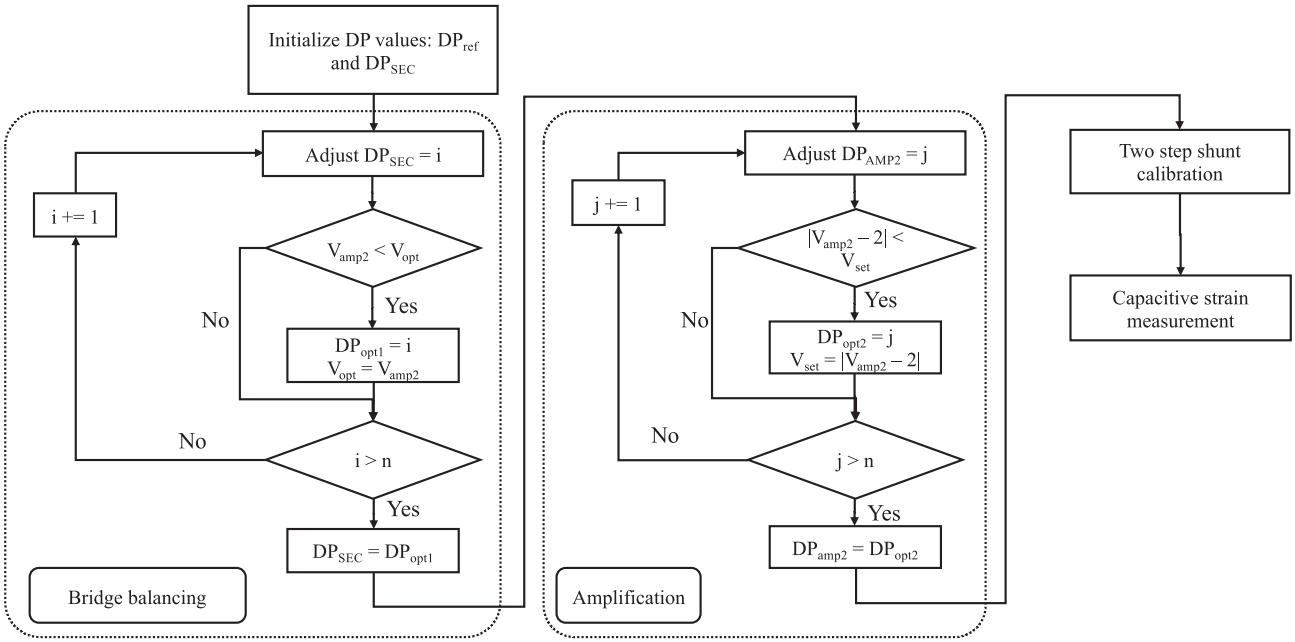


Fig. 9. Fully automated bridge balancing, amplification and shunt calibration diagram.

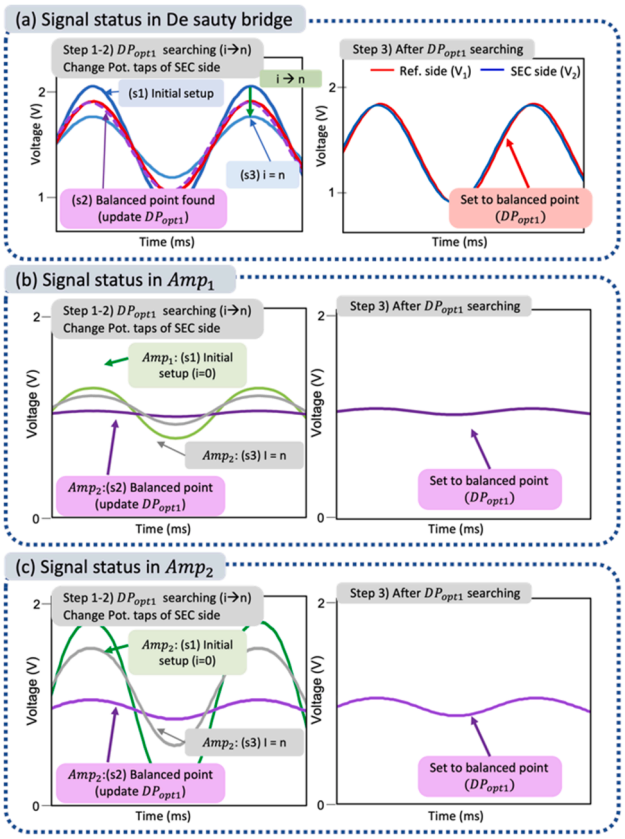


Fig. 10. Bridge balancing procedure in detail.

significantly as shown in the left of Fig. 10(b). The optimal balance case can be determined by identifying the minimum-amplitude case (i.e. s2 in the left figure of Fig. 10(c)), which represents the best match between the two signals from the De sauty bridge.

In short, the adjustment of SEC side's DP tap to DP_{opt1} will set to the smallest peak amplitude of V_{amp2}. Once the automated balancing is done, the V_{amp2} need to be adjusted for maximized sensitivity as discussed in detailed procedure (4–5) described above.

Fig. 11 shows the assembled prototype sensor board for performance validation. Each component has been described in Section 2 and consists of basic signal processing circuits, digital components, and peak-detection circuits.

4. Experimental validation

The performance of the developed sensor board was evaluated through lab-scale tests. A static noise test and a cantilever beam free-vibration test were conducted for performance validation. Two 3×3 in^2 (7.6×7.6 cm^2). SECs were used for a test having different nominal capacitance (SEC1: 326 pF, and SEC2: 335 pF) shown in Fig. 12(a). Fig. 12(b,c) shows the detailed schematic of test setup. A $24 \times 8 \times 0.05$ in. ($609.6 \times 203.2 \times 1.3$ mm) steel plate was used. Two SECs were installed on the steel plate cantilever for a free vibration test. A foil type strain gauge (OMEGA kFH-3-120-C1-11L3M3R, nominal resistance of 120 ± 0.35 Ω, 2×3 mm measurement grid) was installed between the

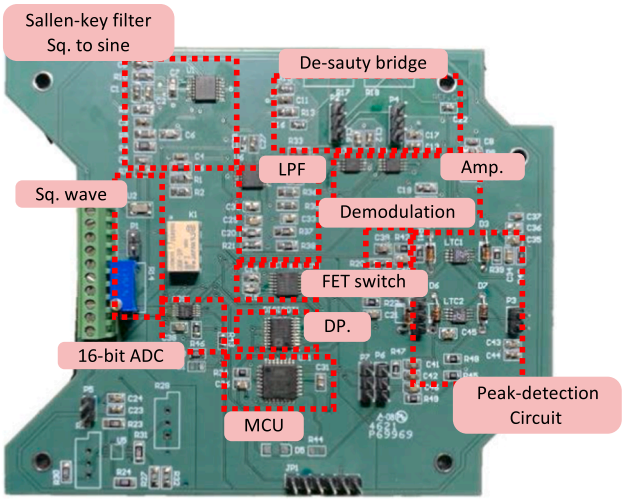


Fig. 11. Prototype sensor board.

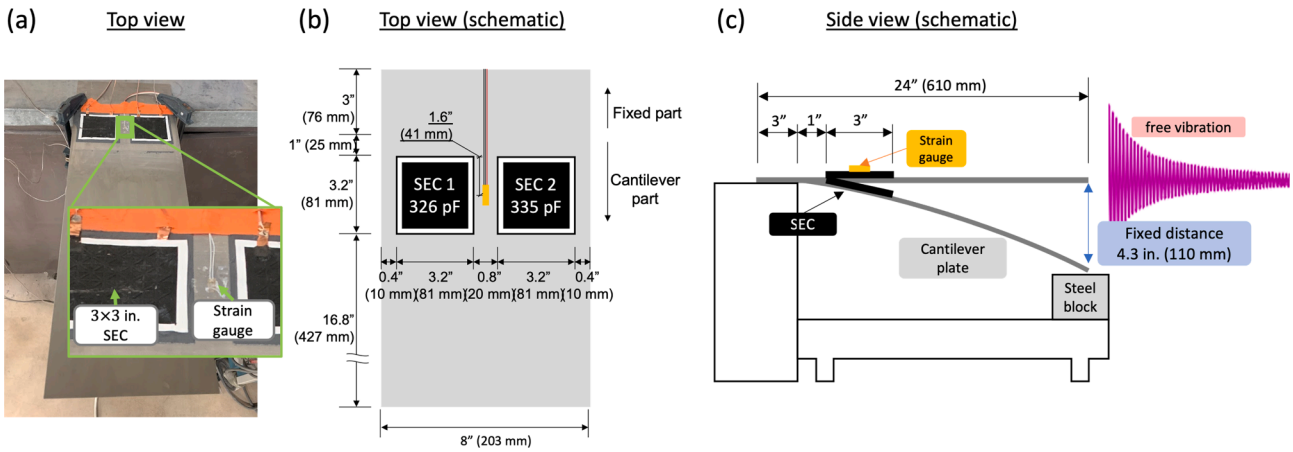


Fig. 12. Test specimens installed on steel plate cantilever.

two SECs for comparison. A National Instrument CompactDAQ chassis (cDAQ-9178) was used to collect the voltage output from strain gauge using an NI9235 module and sensor board using NI9234 module. A wired commercial capacitance measurement device PCAP (PCAP02) was used to compare the capacitance sensing performance. The NI DAQ measurements were sampled at 2 kHz. PCAP measurements were sampled at 110 samples/second.

The free vibration test setup was designed to apply exactly the same vibration history for every test. Fig. 12(c) shows the detailed test setup. The cantilever was bended to touch the steel block located below 4.3 in. (110 mm) by pushing free end point introducing about 400 micro-strain read by strain gauge. The free vibration was generated by releasing the free end. Fig. 13 shows the strain gauge measurement of two free-vibration test results, which matches exactly.

4.1. Shunt calibration

Before testing, each SEC was balanced and calibrated to convert the voltage output to absolute capacitance changes. This study selected shunt capacitors as 1 pF and 3 pF to provide a 2 pF difference. Fig. 14 shows an example of sensorboard output measurement during bridge balancing, amplification, and shunt calibration. The shunt calibration factor for the two SECs are calculated as 0.105 pF/mV for SEC1 and 0.235 pF/mV for SEC2.

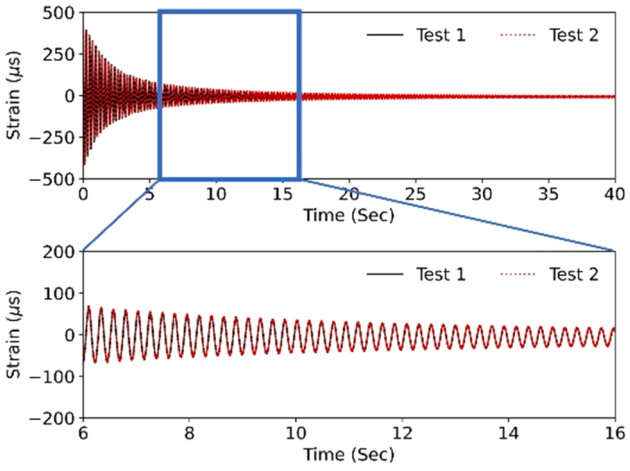


Fig. 13. Strain response time history from two free vibration tests.

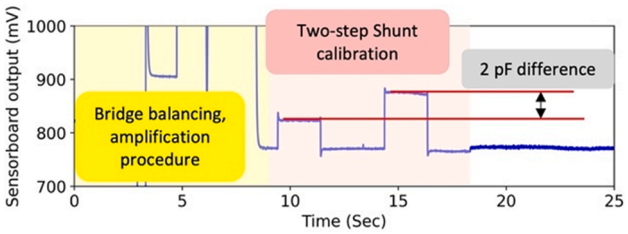


Fig. 14. Output measurement during automated bridge balancing, amplification, and shunt calibration.

4.2. Static noise test

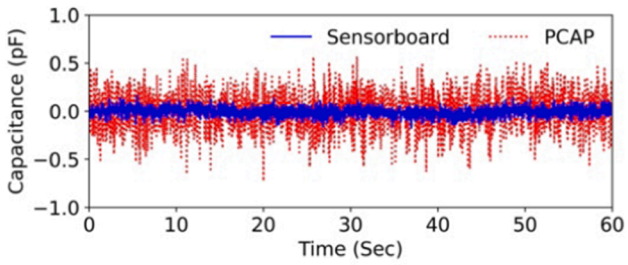
The static noise performance of the developed sensor board is evaluated. Considering the high-sensitivity requirement near the micro-strain level for SHM applications, the noise performance is critical to capture the ambient structural vibration. The ambient root-mean-square (RMS) noise of the sensor board and PCAP are both measured and compared. The ambient RMS noise of the sensor board was measured as 0.121 pF, and the RMS noise of PCAP was 0.184 pF at 15 Hz band width. About 34% lower measurement noise than PCAP was achieved from the sensor board in this study. Fig. 15 shows the ambient noise test results in the time and frequency domains.

4.3. Free vibration test

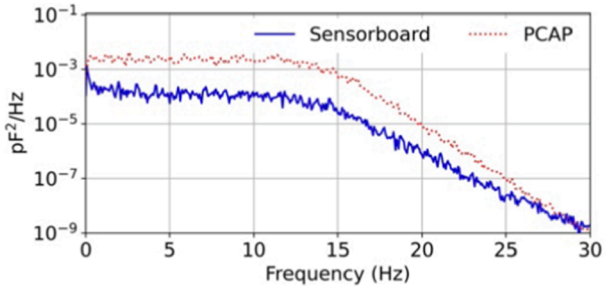
Free vibration tests were conducted to evaluate the sensor board's performance. Two test cases using two different SEC were conducted and compared with the PCAP measurement. The free-vibration test results from the sensor board connected to the SEC were compared with those from the PCAP measurement. The voltage measurement from sensor board was converted to pico-farad (pF) using the calibration coefficient achieved from section 4.1.

The dynamic performance of the sensor board was evaluated by free vibration tests. Figs. 16(a) and 17(a) shows the test measurements from strain gauge (reference), PCAP, and the new sensor board in the time domain. The vibration was excited from ±330 microstrain and decayed to ±80 microstrain after five seconds. The vibration response was measured for 40 s until the strain level reached around ±2–3 microstrains.

As shown in Figs. 16 and 17, the strain gauge measurements showed clear free-vibration responses and well caught the natural frequency peaks of the cantilever beam, of which expected first four frequencies are 4.15 Hz, 8.3 Hz, 12.45 Hz, and 16.6 Hz from the eigenvalue analysis, providing the reference information for the test. The test results from the



(a) Time history



(b) Frequency domain

Fig. 15. Static noise test results.

PCAP and new sensor board connected to the SECs showed somewhat noisier measurements than strain gauge data, as expected, due to the SEC's intrinsic characteristic prone to the electromagnetic field (EM) noise. But they showed a very similar trend at the initial stage when the vibration amplitude was large, i.e., around 0–5 s for both the SEC cases shown in Figs 16(a) and 17(a). However, the amplitude of the PCAP measurement did not decrease according to the actual vibration amplitude decay due to the high noise floor, while the new sensor board's signal decayed accordingly. Figs. 16 and 17(b) and 17(b) show the cross power spectral density (CPSD) of each test case. The CPSDs of different metric measurements are compared based on the capacitance (power) unit (i.e. pF2/Hz) after converting all measurements in to pF unit. PCAP provides the capacitance unit directly, but the sensorboard measurements were converted from mV unit to pF unit using the shunt calibration factors that we obtained in the section 4.1. And the strain gauge measurements were converted from μs unit to pF unit with the scale factors (0.001515 pF/μs for SEC1 test and 0.0056 pF/μs for SEC2 test) that we obtained from the time history peak comparison.

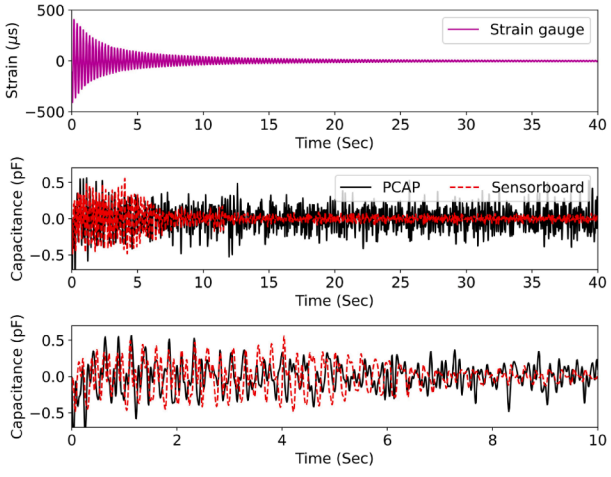
While the strain gauge identified multiple clear peaks, including 4.3, 8.4, and 12.9 Hz, the new sensor board identified two~three peaks. Three peaks are clearly identified from the SEC1 case. However, the SEC2 case does not show clear peaks at 12.9 Hz. This can be explained by the intrinsic electrical loss behavior associated with many sensors fabricated from hyperelastic materials [23]. The PCAP was not able to identify clear peaks due to the high noise floor. The identified frequency peaks have minor differences with the strain gauge measurement caused by differences in the covered geometry area. Consequently, the new sensor board showed better performance compared to the PCAP over the whole frequency range.

5. Conclusions

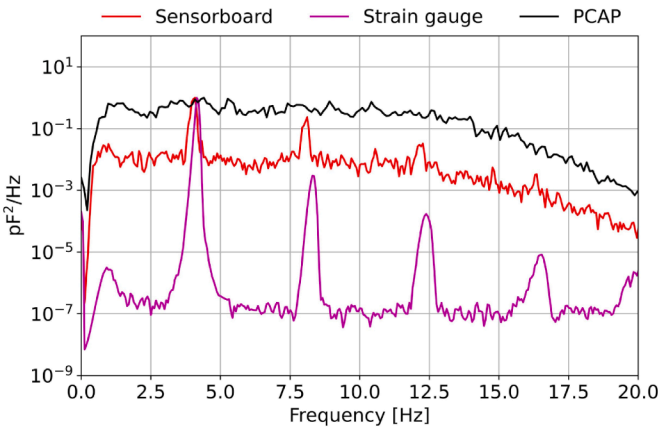
In this study, a fully automated wireless capacitive strain sensor board has been developed, which can be interfaced with the high-fidelity wireless sensing platform Xnode. A fully automated AC De sauty bridge balancing technique has been developed with a series of digital circuitries. A low-cost 8-bit microcontroller was employed to control the digital components such as a digital potentiometer, analog-to-digital converter, and FET bus switch. A peak detection circuit was employed to monitor the high-frequency AC signal effectively using the low-power 8-bit microcontroller ATmega328P. In addition, an integrated software was newly developed for onboard control of the digital components, allowing fully automated bridge balancing, amplification, and two-step shunt calibration. The performance of the developed hardware and software was validated with the lab-scale tests. The developed sensor board successfully balanced the AC De sauty bridge, amplified, and was calibrated in a fully automated fashion for high-sensitivity capacitive strain sensing. A series of lab tests validated that the developed new sensor board outperformed the commercial wired capacitance measurement system PCAP02. The developed sensor board showed a much lower measurement noise than the PCAP02 and confirmed that the automated control features worked as designed.

CRediT authorship contribution statement

Jong-Hyun Jeong: Conceptualization, Methodology, Software, Validation, Writing – original draft. **Hongki Jo:** Supervision, Conceptualization, Writing – review & editing. **Simon Laflamme:** Resources, Project administration, Writing – review & editing. **Jian Li:** Software, Writing – review & editing. **Austin Downey:** Resources, Writing – review & editing. **Caroline Bennett:** Supervision, Writing – review & editing. **William Collins:** Supervision, Writing – review & editing. **Sdiq**

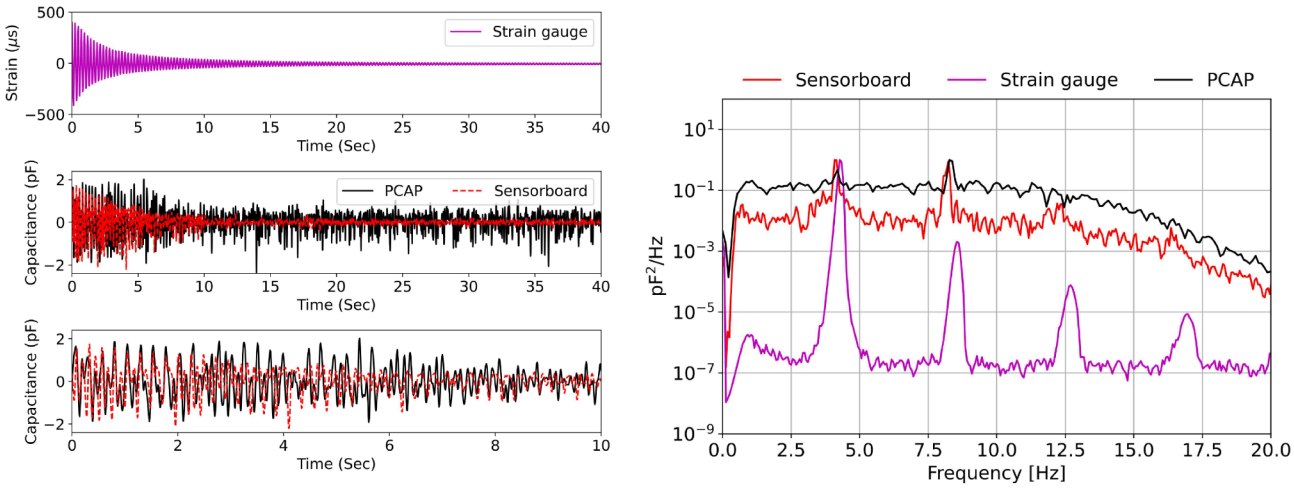


(a) Time history



(b) Frequency domain

Fig. 16. SEC1 test results.



(a) Time history (b) Frequency domain

Fig. 17. SEC2 test results.

Anwar Taher: Investigation, Software. **Han Liu:** Investigation, Resources. **Hyung-Jo Jung:** Supervision, Writing – review & editing.

Declaration of Competing Interest

One of the authors, Hongki Jo, in this publication serves as a scientific advisor for the Embedor Technologies that manufactures the Xnode. Hongki Jo has disclosed an outside interest in the Embedor Technologies to the University of Arizona. Conflicts of interest resulting from this interest are being managed by the University of Arizona in accordance with its policy. This work was supported by Transportation Pooled Fund Study TPF-5(449) that includes the states of Iowa, Kansas, North Carolina, and South Carolina. The support is gratefully acknowledged. Also, the authors thank Prof. Jongwoong Park for advice on hardware system design.

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