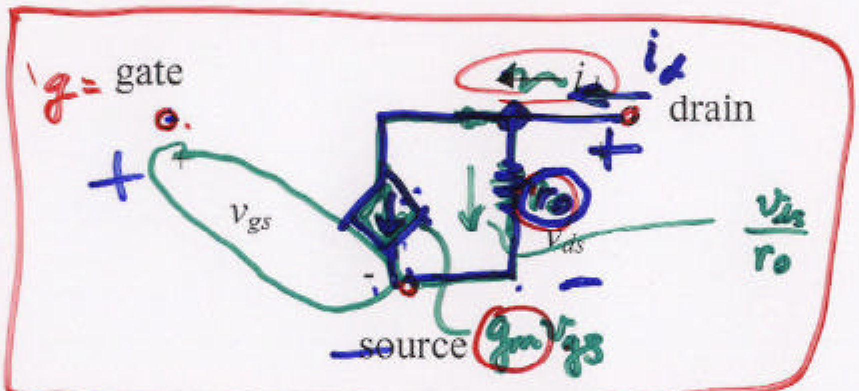
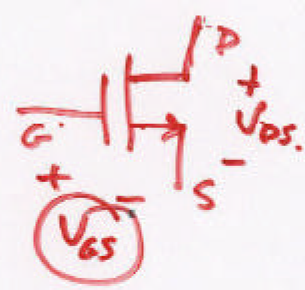
• REVIEW 6 → 7:30 MONDAY NIGHT.
• PS 6: DUE ON THURS. AT 4 pm.
ONLY DO PART a) OF ③; b) & c) → PS 7.

Lecture 16

- Last time:
  - MOSFET small-signal model: three (four) terminal device → complicated!
- Today :
  - Complete small-signal model: add capacitors
  - P-channel MOSFET
  - MOSFET Spice Model

Putting Together a Small-Signal Circuit Model



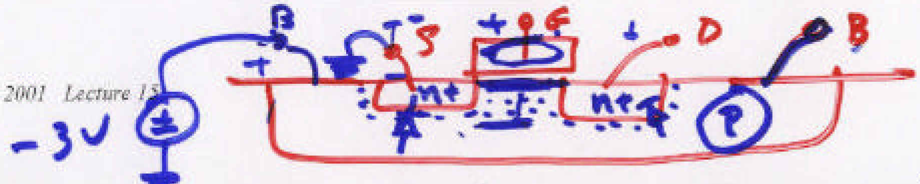


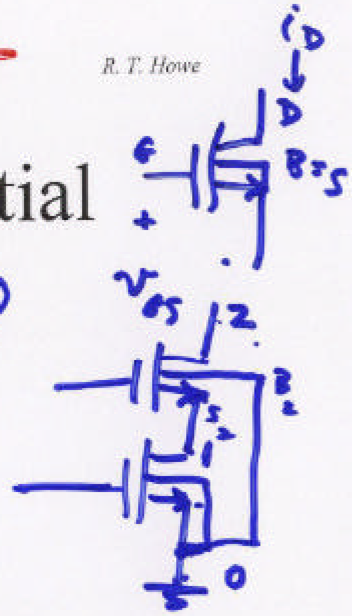
EQUATION → CIRCUIT.

$$i_d = \Delta i_D = \frac{\Delta i_D}{\Delta v_{GS}} + \frac{\Delta i_D}{\Delta v_{DS}}$$

$$i_d = \left.\frac{\partial i_D}{\partial v_{GS}}\right|_Q v_{gs} + \left.\frac{\partial i_D}{\partial v_{DS}}\right|_Q v_{ds}$$

g_m, $\frac{1}{r_o} = g_o$





Role of the Substrate Potential

Need not be the source potential, but $V_B \leq V_S$

... could $V_B = V_S$ + a little....

Effect: changes threshold voltage, which changes the drain current … substrate acts like a "backgate"

2nd order effect

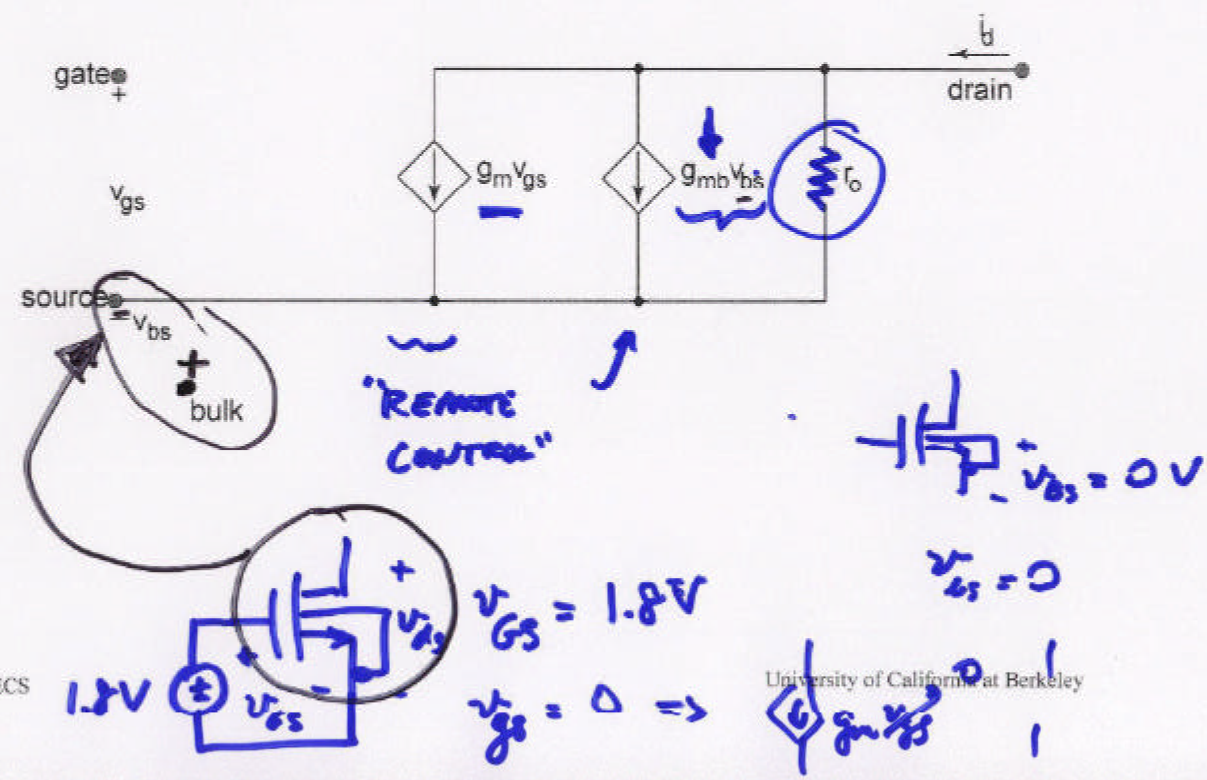
$$g_{mb} = \left.\frac{\Delta i_D}{\Delta v_{BS}}\right|_{(V_{GS},V_{DS},V_{BS})} = \left.\frac{\partial i_D}{\partial v_{BS}}\right|_{(V_{GS},V_{DS},V_{BS})}$$

$V_{BS} < 0$

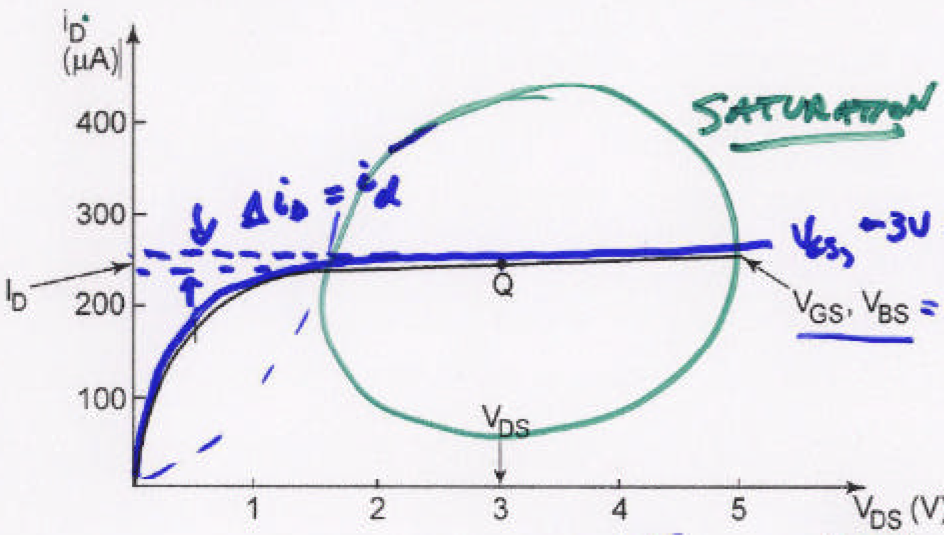
$V_{SB} > 0$.

$Q = (V_{GS}, V_{DS}, V_{BS})$

Four-Terminal Small-Signal Model



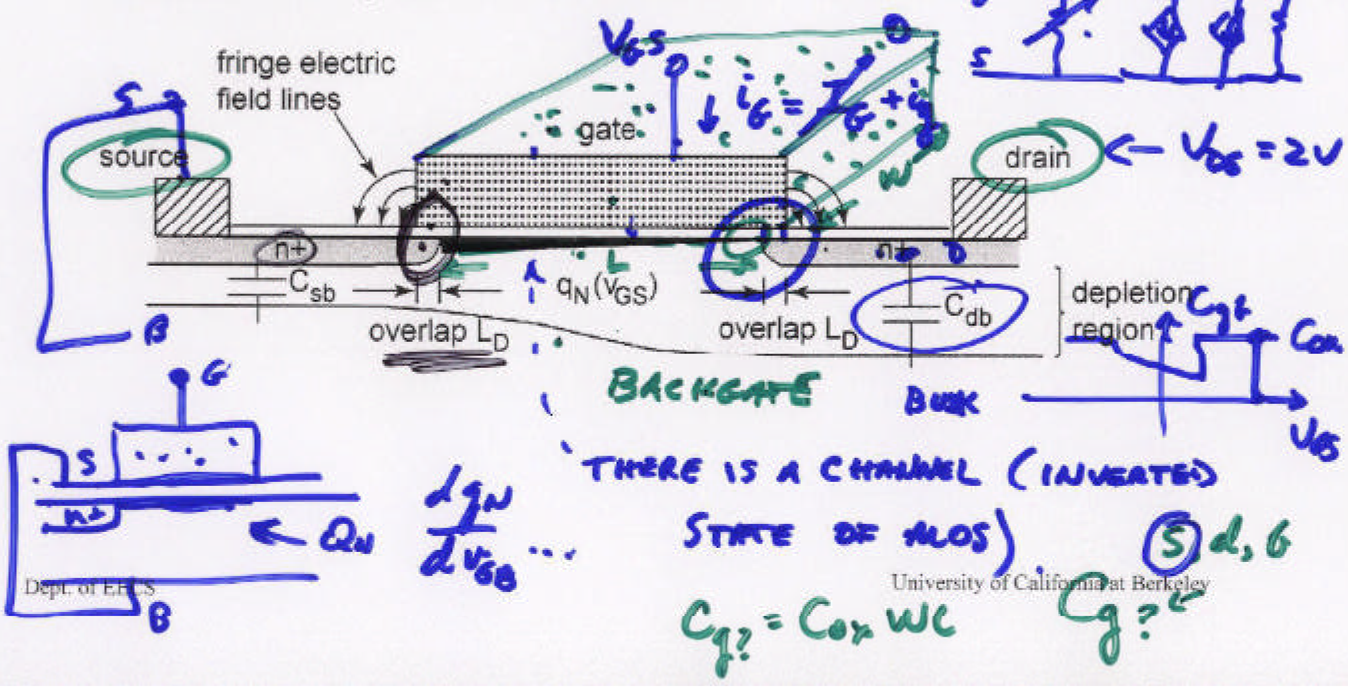
Backgate Transconductance



Result: $g_{mb} = \left.\frac{\partial i_D}{\partial v_{BS}}\right|_Q = \left[\left.\frac{\partial i_D}{\partial V_{Tn}}\right|_Q\right]\left[\left.\frac{\partial V_{Tn}}{\partial v_{BS}}\right|_Q\right] =$

MOSFET Capacitances in Saturation

Gate-source capacitance: channel charge is not controlled by drain in saturation.



Gate-Source Capacitance C_{gs}

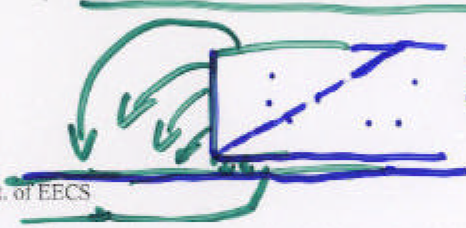
Wedge-shaped charge in saturation → effective area is $(2/3)WL$ (see H&S 4.5.4 for details)

$$C_{gs} = (2/3)WLC_{ox} + C_{ov}$$

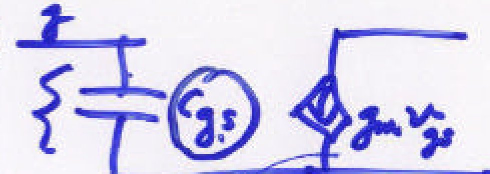
Overlap capacitance along source edge of gate →

$$C_{ov} = L_D W C_{ox}$$

(Underestimate due to fringing fields)



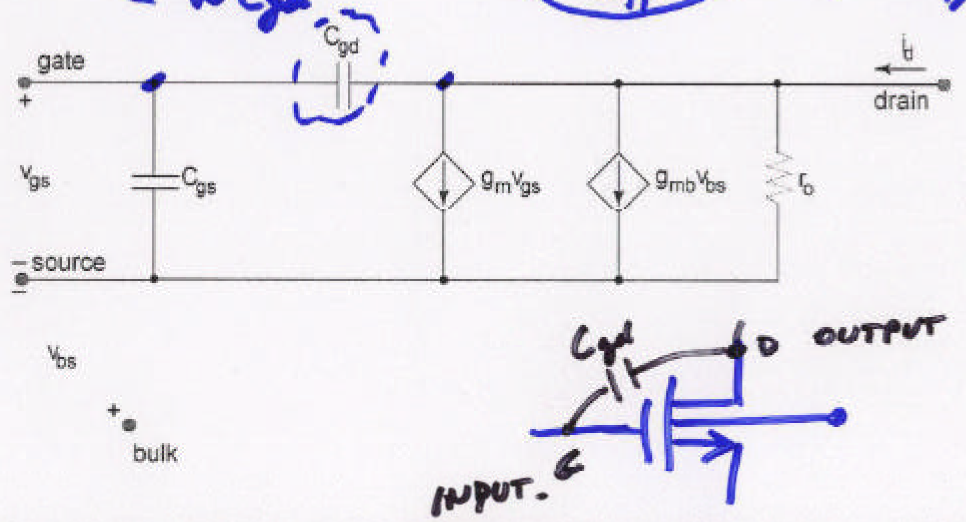
$Z = \frac{1}{j\omega C_{gs}}$



Gate-Drain Capacitance C_{gd}

Not due to change in inversion charge in channel $\left. -\frac{\partial q_N}{\partial v_{DS}} \right|_Q = \phi$ ← SATURATION

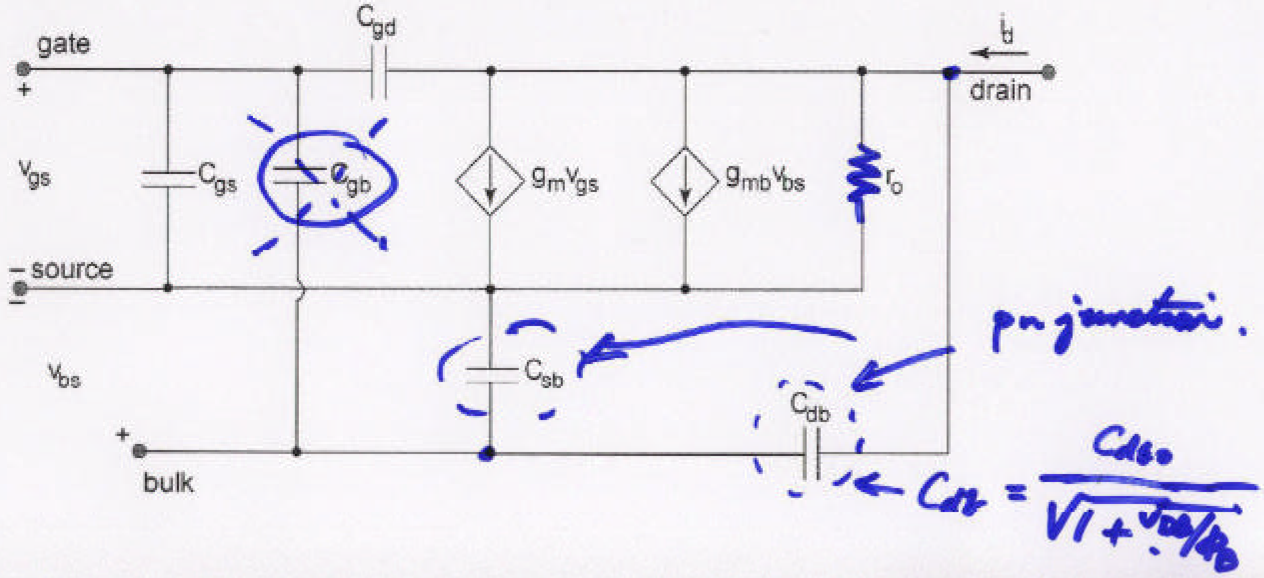
Overlap capacitance C_{ov} between drain and source is $C_{gd} \cong L_D W C_{ox} = W C_{gd}'$ $L_D C_{ox}$ eff ← C_{gd}' fF/μm.



Junction Capacitances

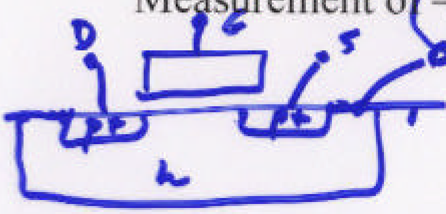
- Drain and source diffusions have (different) junction capacitances since V_{SB} and $V_{DB} = V_{SB} + V_{DS}$ aren't the same

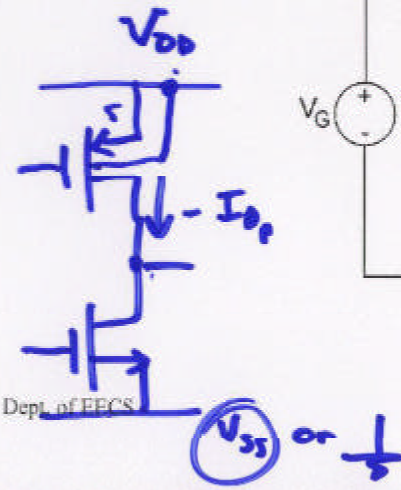
Complete model (without interconnects)

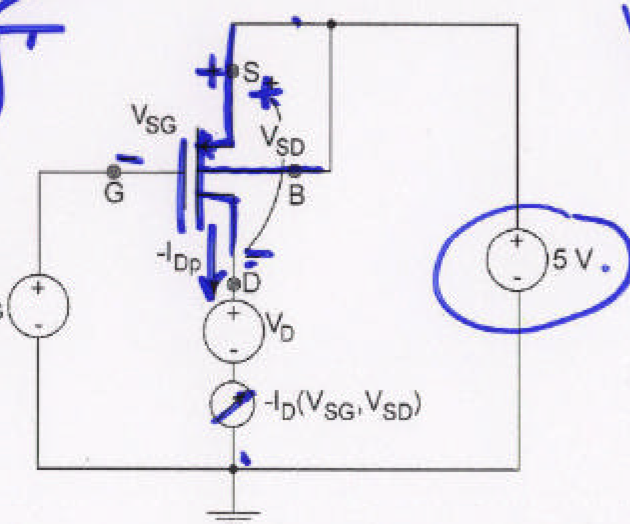


P-Channel MOSFET

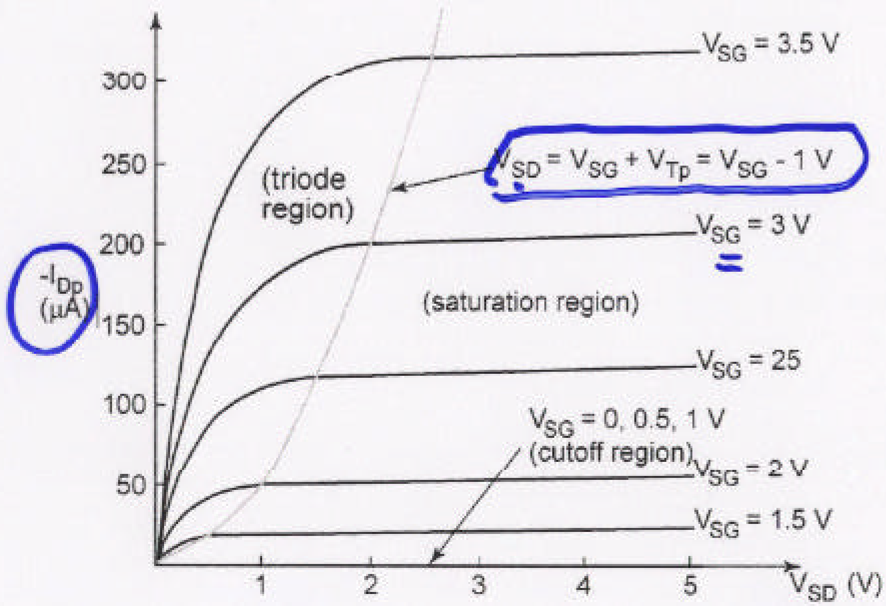
Measurement of $-I_{Dp}$ versus V_{SD}, with V_{SG} as a parameter:





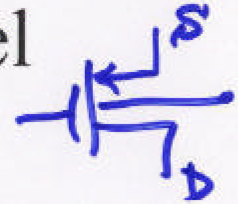


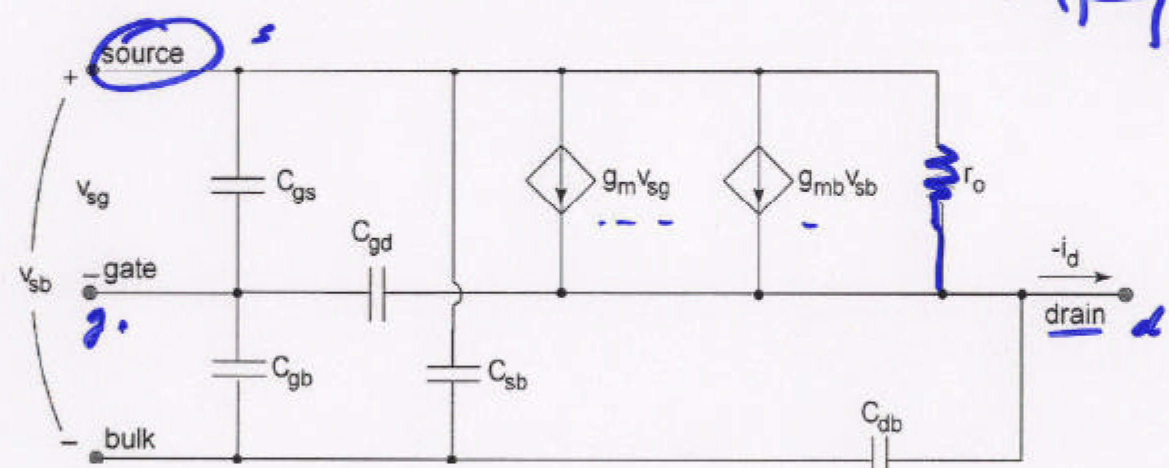
Square-Law PMOS Characteristics



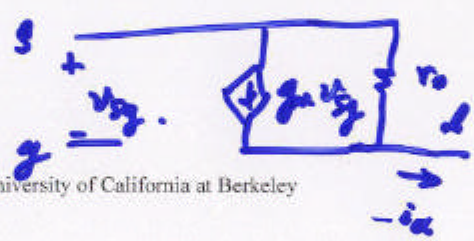
$$I_{D_{p,SAT}} = -\left(\frac{W}{2L}\right)\mu_p C_{ox} \left(V_{SG} + V_{T_p}\right)^2 \left(1 + \lambda_p V_{SD}\right)$$

Small-Signal PMOS Model





$$\frac{\partial(\ )}{\partial v_{SG},\ v_{SD},\ v_{SB}}$$



MOSFET SPICE Model

Many "levels" … we will use the square-law "Level 1" model

See H&S 4.6 + Spice refs. on reserve for details.

↓λ_n γ

.MODEL MODN NMOS LEVEL = 1 VTO = 1 KP = 50U LAMBDA = .033 GAMMA = .6
+ PHI = 0.8 TOX = 1.5E–10 CGDO = 5E–10 CGSO = 5E–10 CJ = 1E–4 CJSW = 5E–10
+ MJ = 0.5 PB = 0.95

.MODEL MODP PMOS LEVEL = 1 VTO = –1 KP = 25U LAMBDA = .033 GAMMA = .6
+ PHI = 0.8 TOX = 1.5E–10 CGDO = 5E–10 CGSO = 5E–10 CJ = 3E–4 CJSW = 3.5E–10
+ MJ = 0.5 PB = 0.95