ECE 137 B: Notes Set 1
Transistor High-Frequency Models

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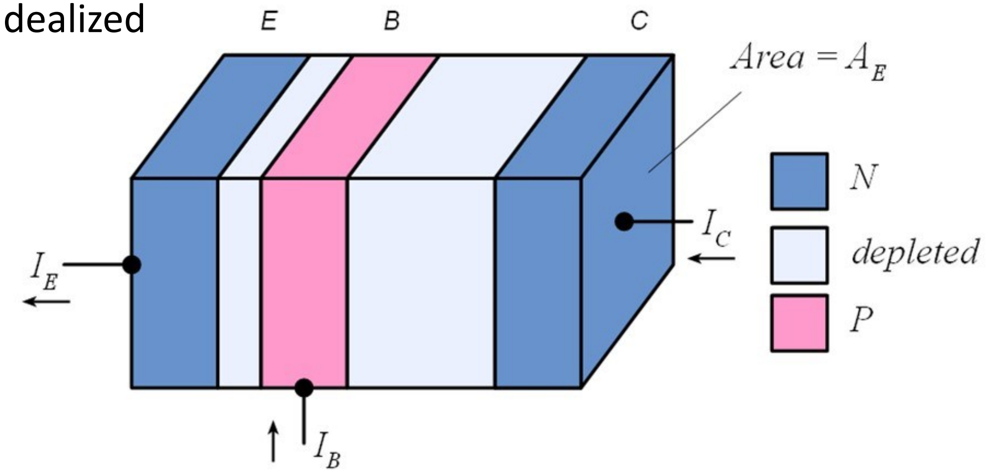
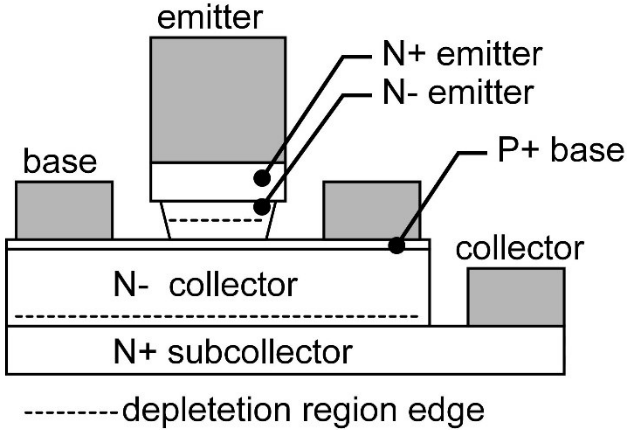
Bipolar transistor structure

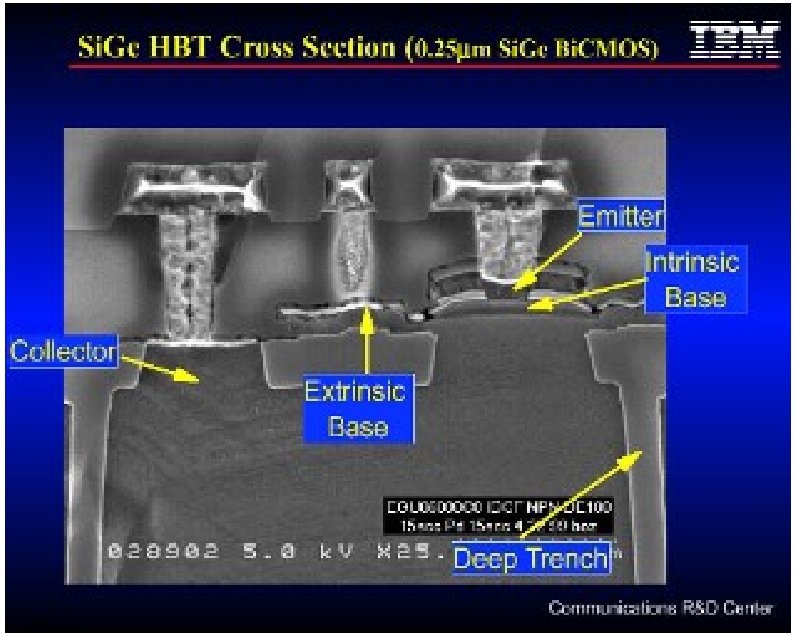
Idealized



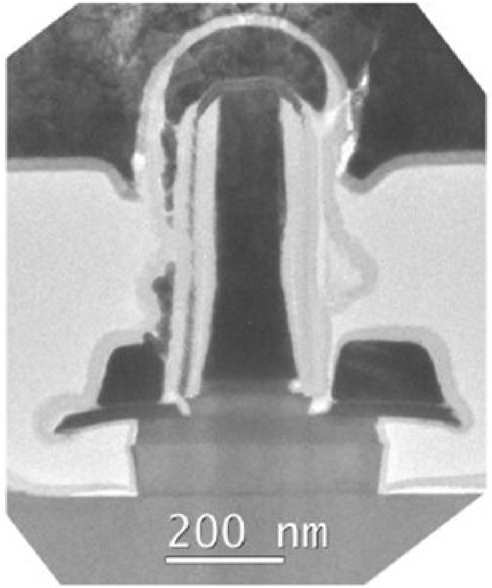
somewhat idealized



real



real



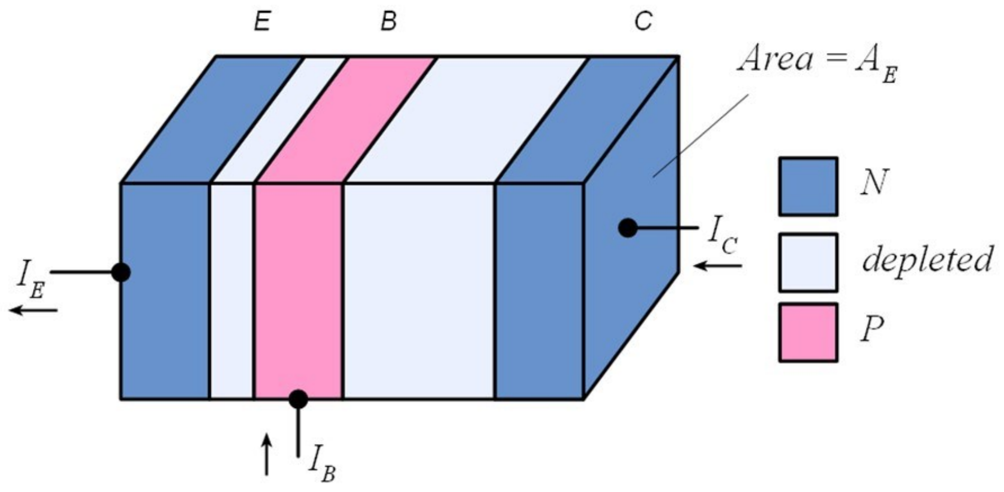
M. Urteaga, Z. Griffith, M. Seo, J. Hacker and M. J. W. Rodwell, "InP HBT Technologies for THz Integrated Circuits," in *Proceedings of the IEEE*, vol. 105, no. 6, pp. 1051-1067, June 2017, doi: 10.1109/JPROC.2017.2692178.

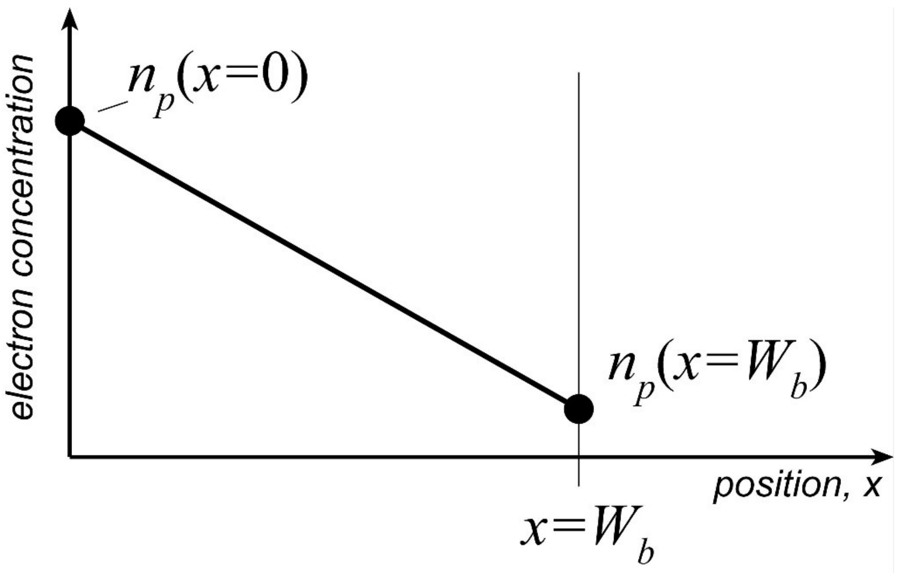
J. J. Pekarik *et al*., "A 90nm SiGe BiCMOS technology for mm-wave and high-performance analog applications," *2014 IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM)*, Coronado, CA, USA, 2014, pp. 92-95, doi: 10.1109/BCTM.2014.6981293.

J. C. Rode *et al*., "Indium Phosphide Heterobipolar Transistor Technology Beyond 1-THz Bandwidth," in *IEEE Transactions on Electron Devices*, vol. 62, no. 9, pp. 2779-2785, Sept. 2015, doi: 10.1109/TED.2015.2455231.

Base charge storage (1)

$$n_p(0) = n_{po}\exp(V_{be}/V_t)$$
$$n_p(W_b) = n_{po}\exp(V_{bc}/V_t)$$
$$V_t = kT/q$$
$$n_{po} = n_i^2/N_A$$
$$N_A = \text{ base doping}$$



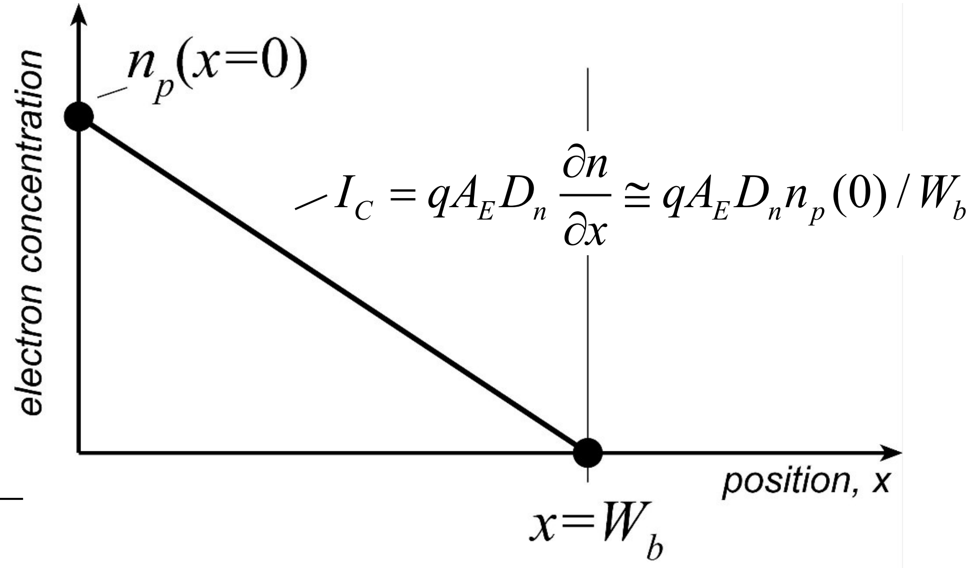


Base charge storage (2)

Normally: collector-base junction reverse-biased:

$V_{bc} < 0,\ |V_{bc}| >> V_t,$ so $n_p(W_b) << n_{po}$

$$\Rightarrow \text{Emitter current} = I_E = \frac{qA_E D_n n_{po}}{W_b} \exp(V_{be}/V_t)$$



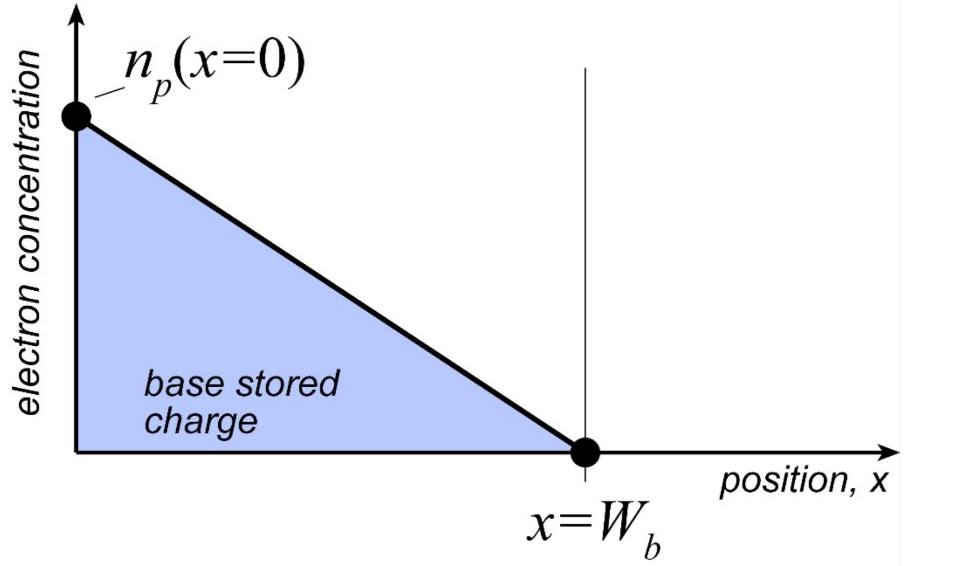
Stored charge in base:

$$Q = \frac{qn_p(0)W_b A_E}{2} = \frac{qW_b A_E n_{po}}{2} \exp(V_{be}/V_t)$$

Comparing this to the expression for I_E

$$\frac{Q}{I_E} = \frac{W_b^2}{2D_n} \triangleq \tau_b$$

$$Q = \tau_b I_E \text{ where } \tau_b = \frac{W_b^2}{2D_n}$$

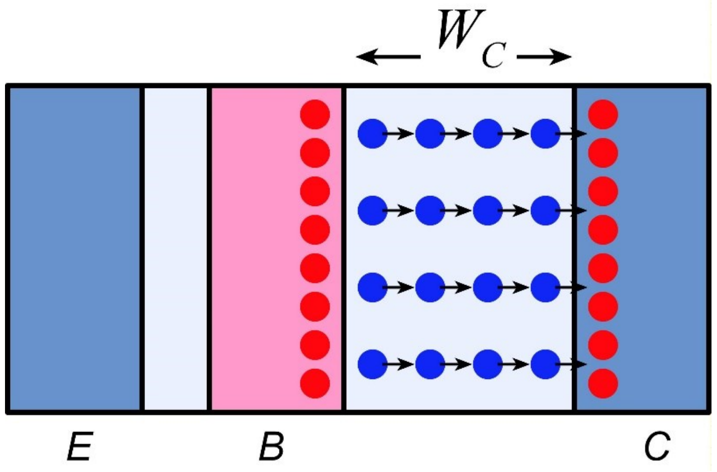


Collector charge storage

Current in collector depletion region = I_E

electron velocity in depletion region = $v_{sat} \sim 10^7$ cm/s (Si)

negative electron charge in depletion region = $-I_E W_c / v_{sat}$



electron charge balanced by + charge in base, collector.

Equal + charge in base and in collector

$\rightarrow$ +charge on base side of deplection region $= +I_E W_c / 2v_{sat}$

$Q = I_E W_c / 2v_{sat}$

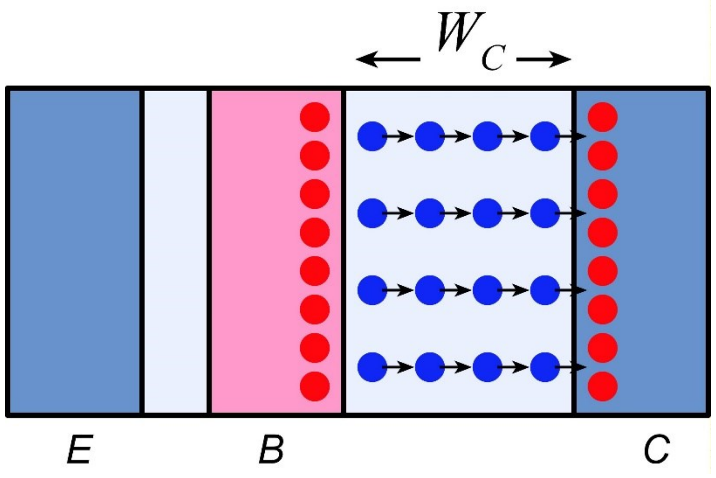
$$Q = \tau_c I_E \text{ where } \tau_c = \frac{W_C}{2v_{sat}}$$

Total stored charge and diffusion capacitance

Total stored charge

$Q_F = (\tau_b + \tau_c)\, I_E = \tau_F \; I_E$

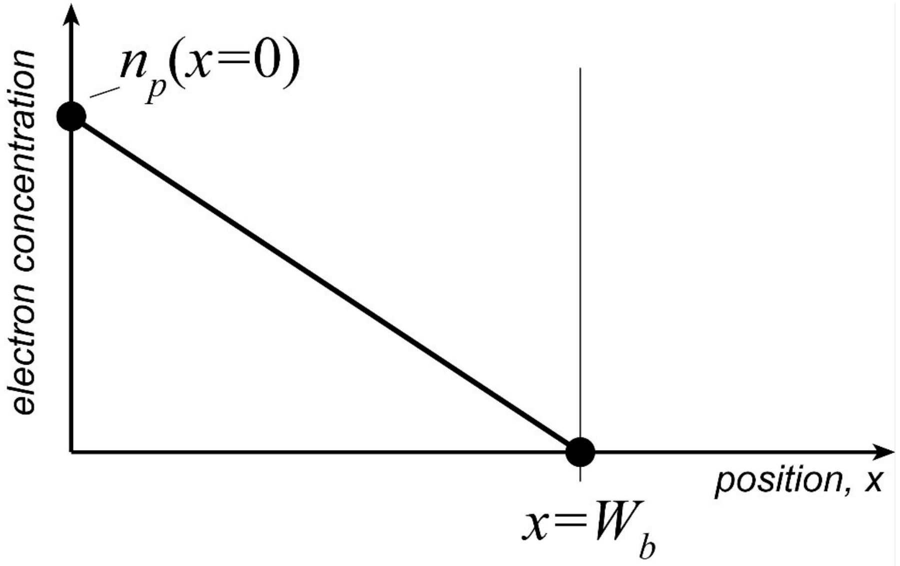
τ_F = forward transit time = $\tau_b + \tau_c$



Diffusion capacitance

$$C_{diff} \triangleq \frac{\partial Q_F}{\partial V_{be}} = \frac{\partial Q_F}{\partial I_C}\frac{\partial I_C}{\partial V_{be}} = g_m \tau_F$$

$$C_{diff} = g_m \tau_F$$



C_{diff} is a mathematical trick to turn transit time into capacitance.

C_{diff} is nevertheless 100% real and measurable.

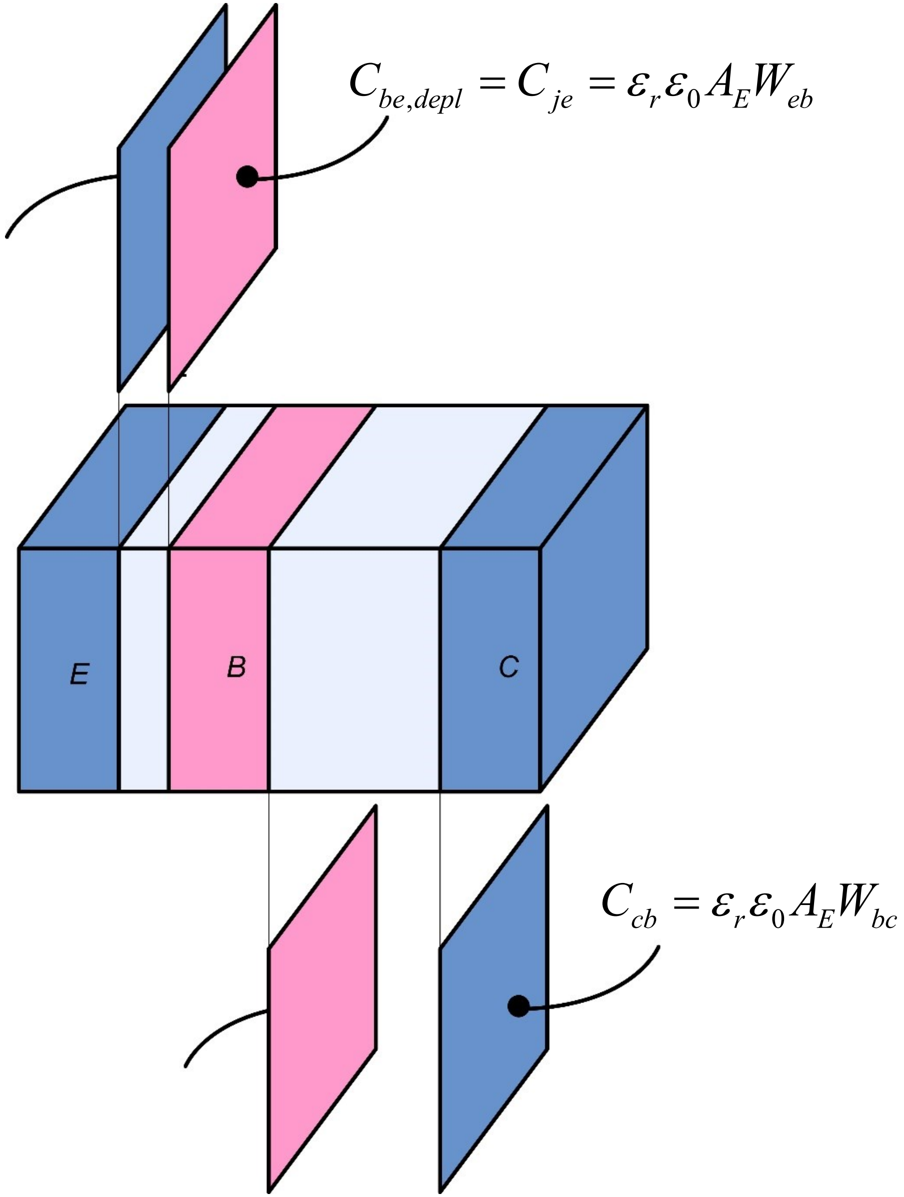
...it is just not a parallel plate capacitance.

Depletion capacitances

In a real transistor, the area of the base-collector junction is much larger than the area of the base-emitter junction.

In a real transistor, the base-collector depletion depth W_c is much larger than the area of the base-emitter depletion depth W_{eb}.

In a real transistor, the current transiting the base-emitter depletion region adds additional terms to the expression for $C_{be,depl}$.



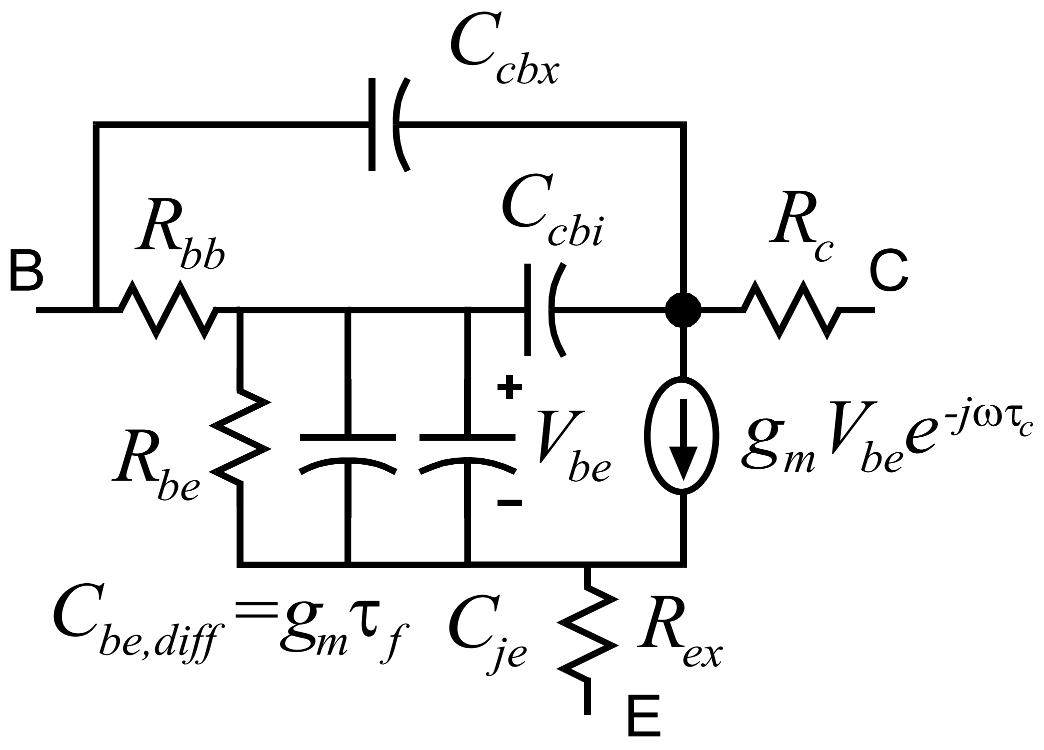
Fairly accurate high-frequency bipolar transistor model

$R_{be} = \beta / g_m$

$\tau_f = \tau_b + \tau_c$

$g_{mo} \equiv \frac{\partial I_C}{\partial V_{BE}} = \frac{I_C}{(nkT/q)}$

$g_m = g_{mo} e^{-j\omega\gamma\tau_c} \quad 0 < \gamma < 1$ (typically ~0.8)



C_{je}, C_{cbi}, C_{cbx} : depletion capacitances

$C_{be,diff}$: diffusion capacitance

τ_b, τ_c : carrier transit times in base and collector

R_b, R_e, R_c : parasitic resitances

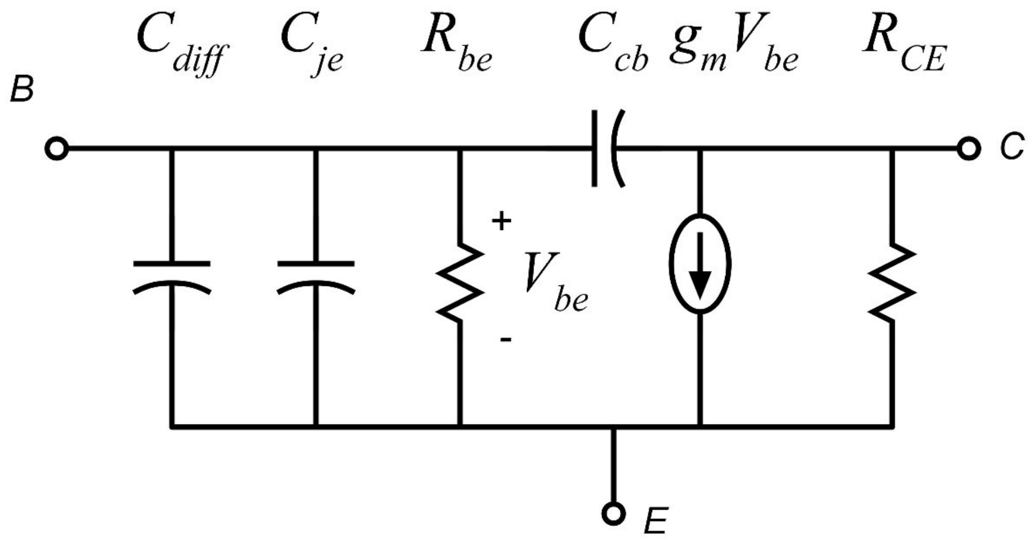
This is called a hybrid-π model

Simplified high-frequency bipolar transistor model

$R_{be} = \beta / g_m$

$\tau_f = \tau_b + \tau_c$

$g_m = \dfrac{\partial I_C}{\partial V_{BE}} = \dfrac{I_C}{V_T}$ where $V_t = kT / q$



C_{je}, C_{cbi}, C_{cbx} : depletion capacitances

$C_{be,diff}$: diffusion capacitance

τ_b, τ_c : carrier transit times in base and collector

This is called a simplified hybrid-π model

....we will use this model in this class.

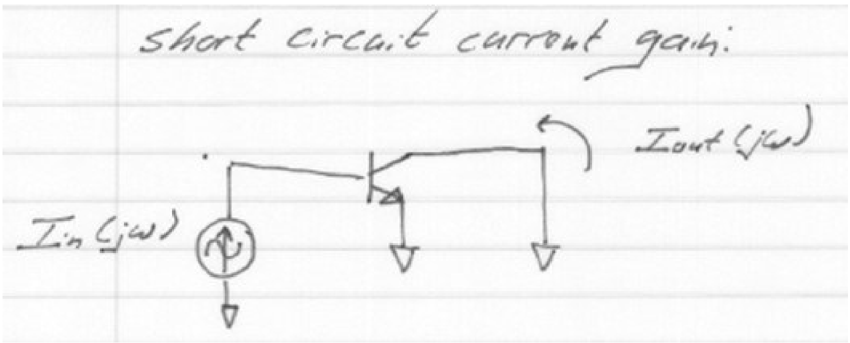
Short-circuit current gain.

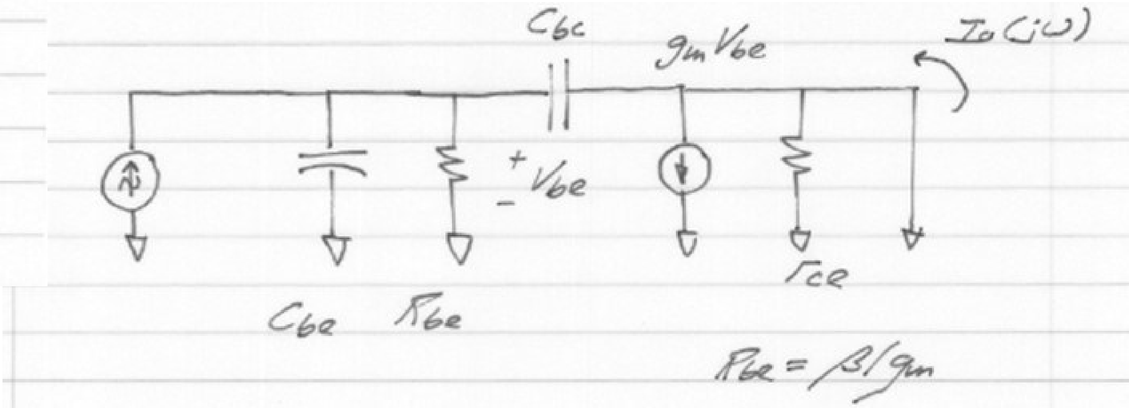
$$\frac{I_o(j\omega)}{I_i(j\omega)} = g_m\left(r_{be} \,\|\, \frac{1}{j\omega(C_{be}+C_{cb})}\right) - \frac{j\omega C_{cb}}{1/r_{be}+j\omega(C_{cb}+C_{be})}$$

$$= \frac{g_m}{1/r_{be}+j\omega(C_{be}+C_{cb})} - \frac{j\omega C_{cb}}{\text{same denominator}}$$

note $g_m r_{be} = \beta$

$$= \frac{\beta(1-j\omega C_{cb}/g_m)}{1+j\omega(C_{be}+C_{cb})\beta/g_m}$$





f_τ=short-circuit current gain cutoff frequency

lets neglect the zero → then $\|I_o/I_i\| = 1$

when $f = f_\tau$ and we find f_τ like so:

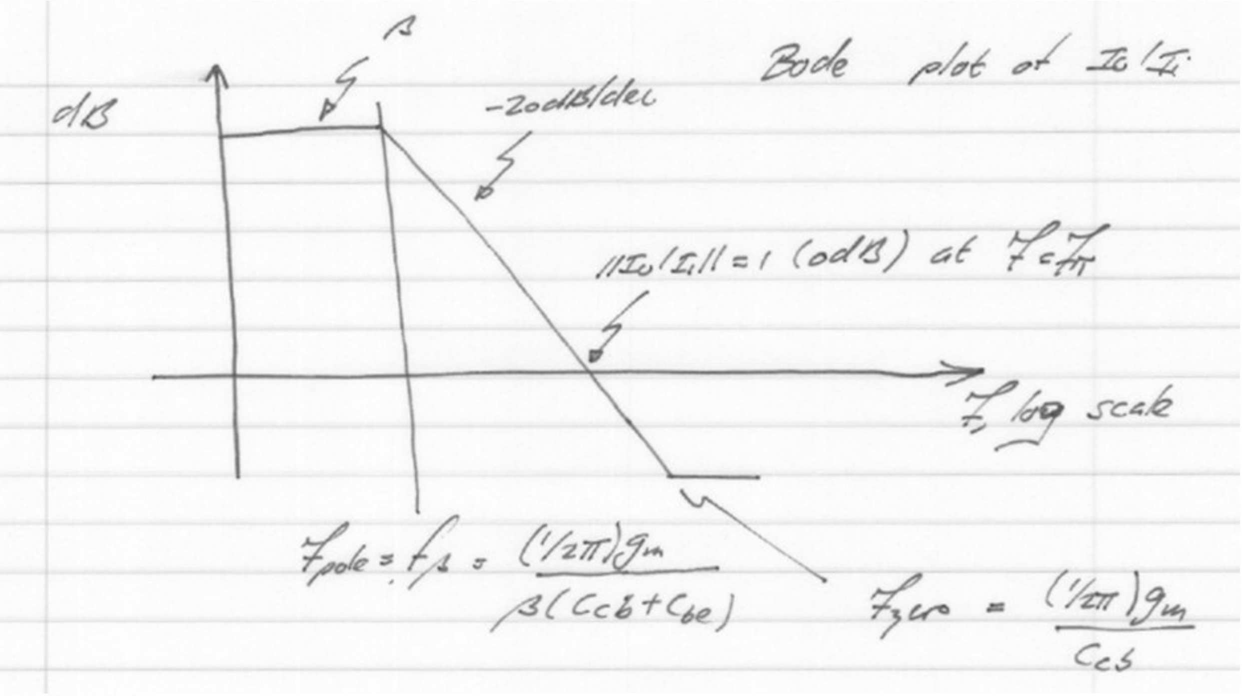
$$1 = \|h_{21}\| = \left\|\frac{I_o}{I_i}\right\| = \frac{\beta}{\sqrt{1+\beta^2\omega_\tau^2(C_{be}+C_{cb})^2/g_m^2}}$$

If $\beta >> 1$, this means

$$\beta = \beta\omega_\tau(C_{be}+C_{cb})/g_m$$

$$\rightarrow \boxed{f_\tau = \frac{\omega_\tau}{2\pi} = (1/2\pi)\frac{g_m}{C_{cb}+C_{be}}}$$

this is called the "short circuit current gain cutoff frequency"



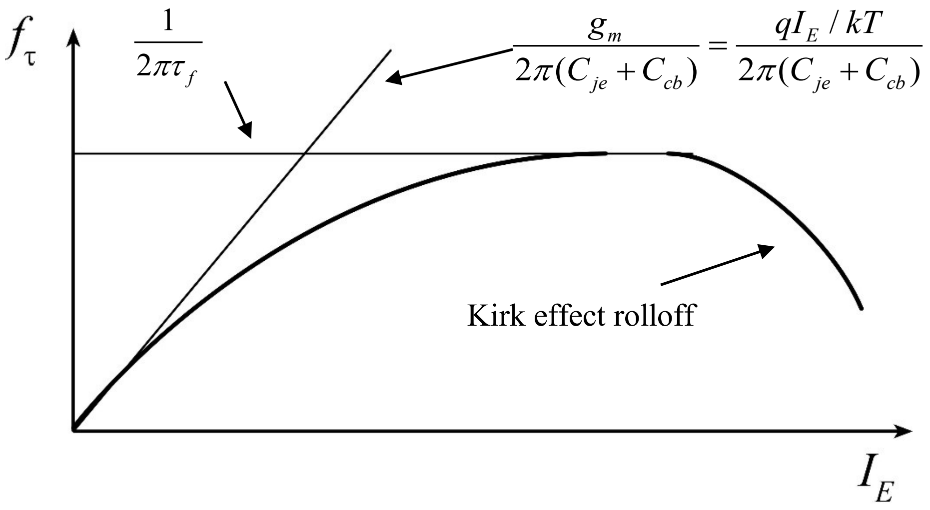
Variation of f_τ with current

$$C_{be} = C_{be,depl} + C_{be,diff} = C_{be,depl} + g_m \tau_f$$

$$f_\tau = (1/2\pi)\frac{g_m}{C_{cb} + C_{be,depl} + g_m \tau_f}$$

$$= \left(\frac{1}{2\pi}\right)\frac{1}{\tau_f + (C_{cb} + C_{be,depl})\, r_e}$$

$$r_e = \frac{1}{g_m} = \frac{kT}{qI_E}$$



Getting high-frequency BJT #s from SPICE model

1) τ_f ← SPICE uses this directly

2) $C_{cb}(V_{bc}) = \dfrac{C_{jc}}{(1+V_{cb}/V_{jc})^{M_{jc}}}$

M_{jc}, C_{jc}, V_{jc} model parameters.

3) $C_{je}(V_{be}) \stackrel{?}{=} \dfrac{C_{je}}{(1-V_{be}/V_{je})^{M_{je}}}$

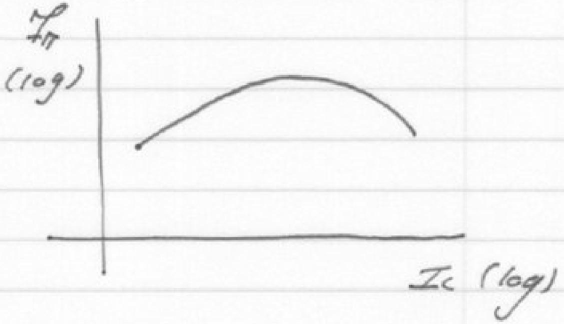
this formula is modified when V_{be} is close to turn-on ... exact expression is very complex

Getting high-frequency BJT #s from data sheet

- data sheet usually gives C_{cb} directly vs V_{cb}

  sometimes gives C_{ob}; $C_{ob} \simeq C_{cb}$

- usually gives f_T vs I_c:

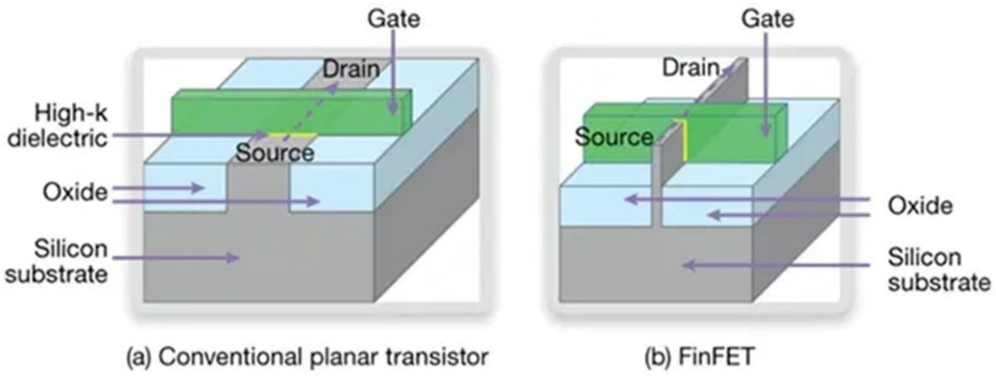


Procedure is:

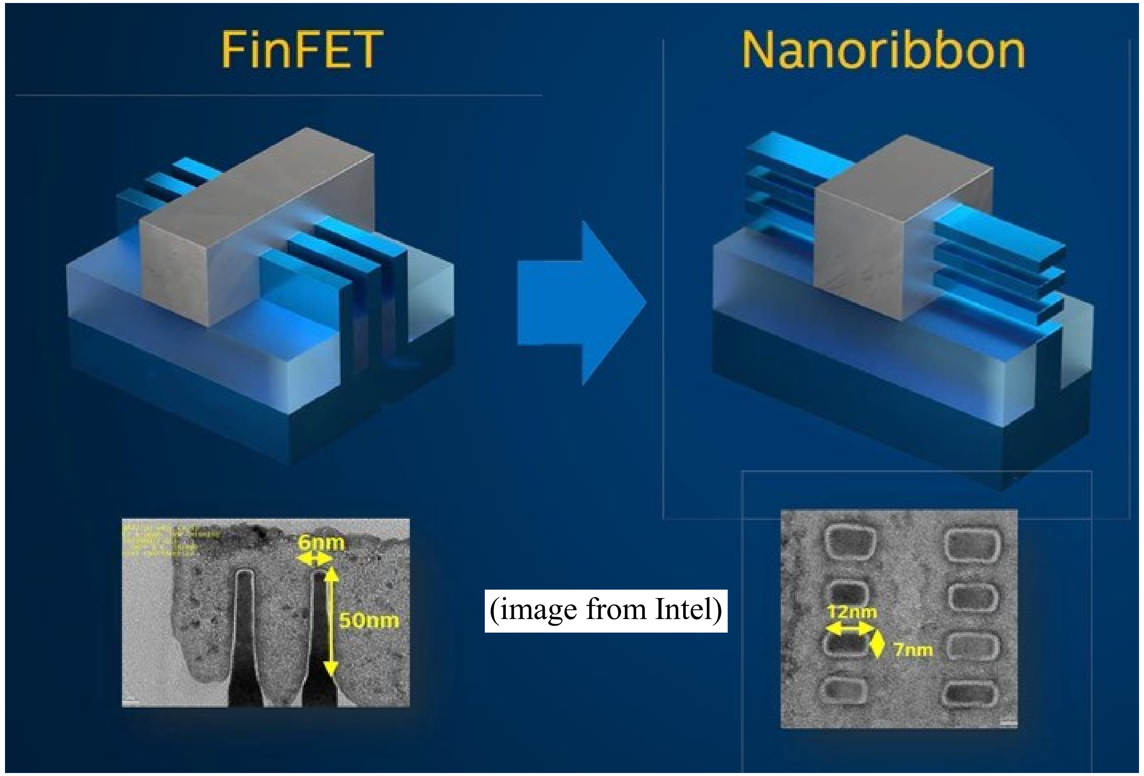
- read C_{bc} from datasheet
- read f_T at current of interest
- determine C_{be} from

$$C_{be} = \frac{g_m}{2\pi f_T} - C_{cb}.$$

MOSFET physical structures

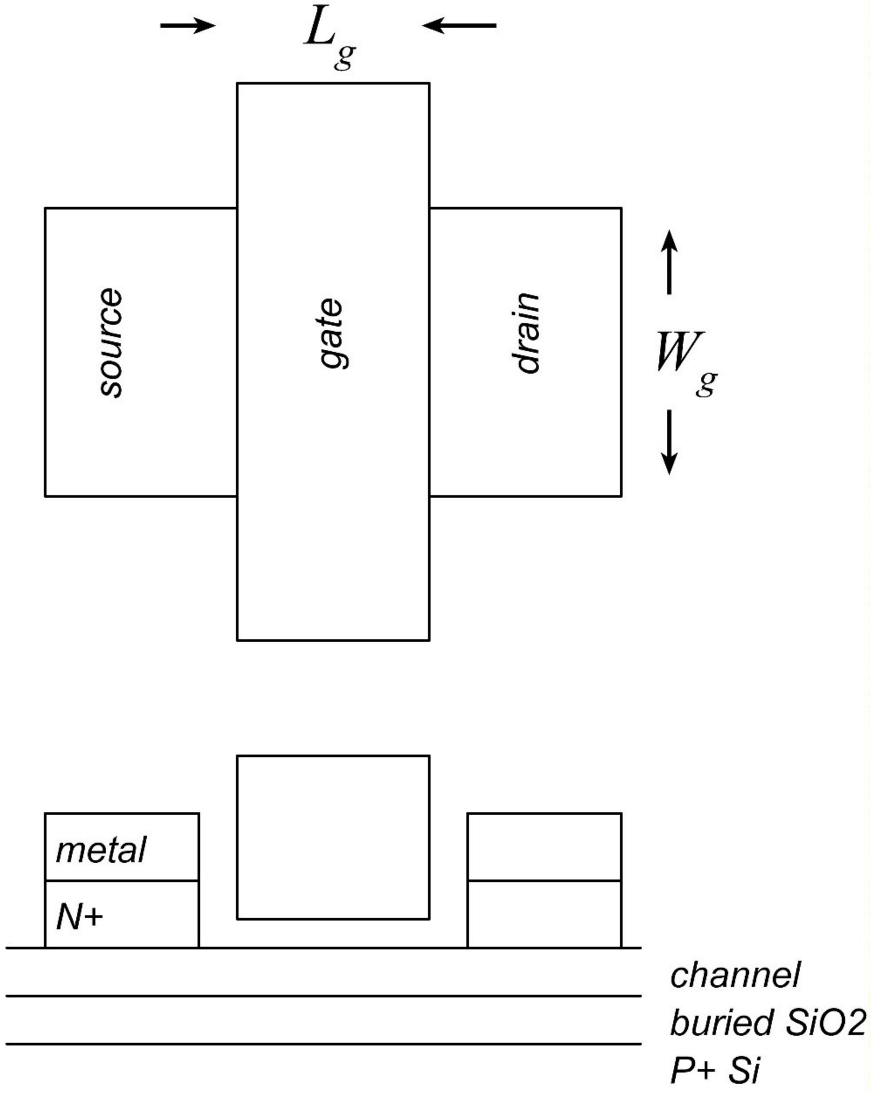


(image from Intel)



(image from Intel)

Cartoon of SOI device



Physical structure and capacitanes

Gate-channel capacitance:

$$\frac{1}{C_{gate-channel}} \approx \frac{T_{ox}}{L_g W_g \varepsilon_r \varepsilon_{ox}} + \frac{1}{L_g W_g c_{semi}}$$

$\varepsilon_r =$ gate insulator dielectric constant

$T_{ox} =$ gate insulator thickness

$c_{semi} =$ semiconductor surface capacitance per unit area.

-depends on bias $(V_{gs} - V_{th})$

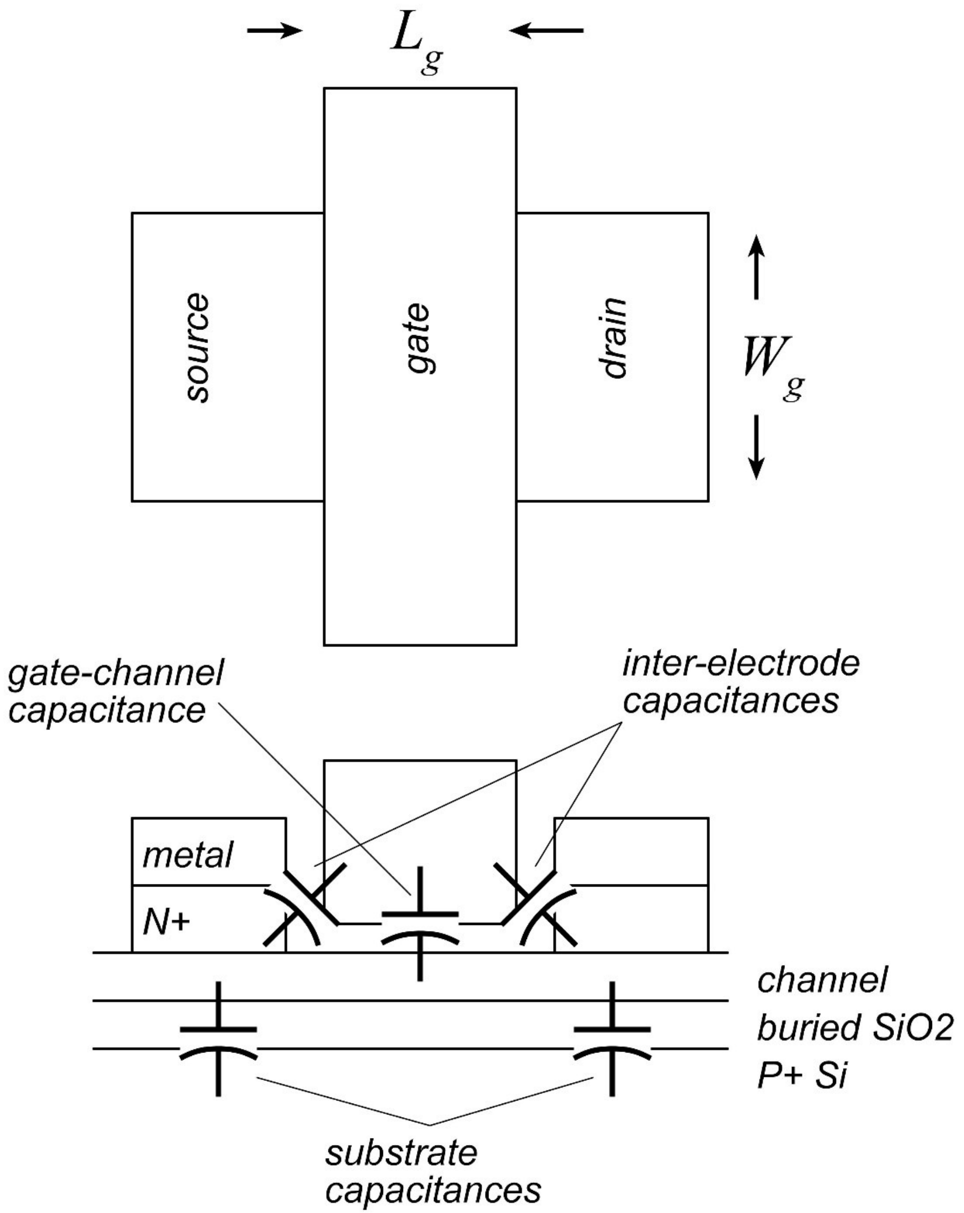
-even in strong inversion is not infinite (see 137A notes)

Inter-electrode capacitances: $C_{\text{int}} \propto W_g$

Gate-source capacitance: $C_{gs} = C_{\text{int}} + C_{gate-channel}$

Gate-drain capacitance: $C_{gd} = C_{\text{int}}$

Note also the source, drain capacitances to the substrate



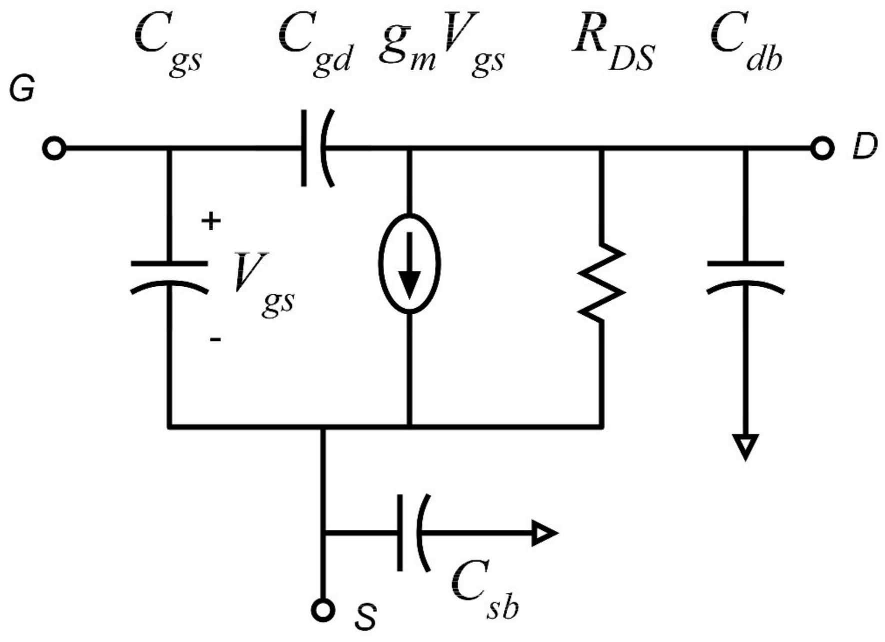
Simplified Model of MOSFET capacitances

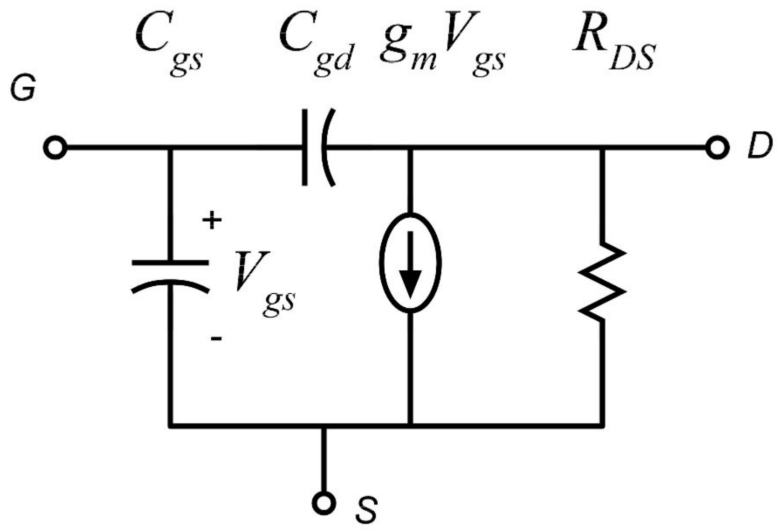
In modern MOSFETs, inter-electrode capacitances are large.
This tends to "hide" the variation of $C_{gate-channel}$ with bias
We will use a very simple model:

Gate-source capacitance: $C_{gs} = k_1 W_g$
Gate-drain capacitance: $C_{gd} = k_2 W_g$
Source-substrate capacitance: $C_{sb} = k_3 W_g$
Drain-substrate capacitance: $C_{db} = k_3 W_g$

$k_1 ... k_3$ will be specified.
This model neglects the bias-dependence of all capacitances.

To make problems easier to work, we will usually neglect C_{sb} and C_{db} , even though this is a poor approximation.





MOSFET short-circuit current gain