30.7 A Crystal-Less BLE Transmitter with -86dBm Frequency-Hopping Back-Channel WRX and Over-the-Air Clock Recovery from a GFSK-Modulated BLE Packet

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Wireless transceivers traditionally perform local-oscillator (LO) calibration using an external crystal oscillator (XTAL) that adds significant size and cost to a system. Removing the XTAL enables a true single-chip radio, but an alternate means for calibrating the LO is required. Integrated references like on-chip LC [1] or relaxation [2] oscillators are either high power or have PVT sensitivity too high for wireless standards. Multiple crystal-less radios address this challenge [3-6]. [3] replaces the XTAL with an FBAR resonator, which is still not fully integrated. [4-5] recover a reference clock from a received signal but take hundreds of milliseconds to lock and are thus highly susceptible to interference. [6] uses an open-loop LC oscillator to reduce power but has insufficient frequency accuracy for wireless standards.

This paper presents a crystal-less transmitter with symmetric over-the-air clock recovery compliant with the BLE standard. The novelty of this work is 1) a frequency-hopping back-channel receiver to detect advertising events from a broadcaster while rejecting interference; 2) an architecture with two fast-locking PLLs and selective baseband filter to recover a reference clock from a received packet and then transmit a GFSK-modulated BLE packet on any channel, and 3) an ADPLL with averaging controller to recover a stable reference from a GFSK-modulated data-whitened signal. The crystal-less transmitter with clock recovery meets all BLE requirements for SIR, making this a robust solution for removing the XTAL even in densely populated networks.

The fully integrated crystal-less transceiver is shown in Fig. 30.7.1, which receives and transmits BLE compliant messages. The receiver consists of two RX signal paths mixed down by LO_1: 1) a back-channel (BC) direct-conversion path for detecting advertising (ADV) events, and 2) a clock-recovery path with an intermediate frequency of 8MHz producing the reference for PLL_1 and PLL_2. The transmitter comprises a second PLL_2 with LO_2, a GFSK modulator for open-loop modulation, and a digital PA. Both LOs are on-chip LC oscillators, are trimmed only once for process variation, and when in BC scanning mode operate open-loop without any reference. This is sufficient for a divided LO_2 to clock the digital baseband and for LO_1 to frequency hop between ADV channels in the energy-detection BC path and detect an ADV event (a sequence of 3 packets on the ADV channels). Upon detecting the 3rd packet in an ADV event, PLL_1 is enabled and locks LO_1 within 50µs to the 8MHz reference recovered from the packet by using a novel averaging controller immune to GFSK-modulated signals. Lock detect of PLL_1 then enables PLL_2 to lock LO_2 in less than 50µs to the 8MHz recovered reference with the LO_2 RF centered on any of the 40 BLE channels. The 8MHz reference is only present while the 3rd packet is being received, therefore both PLLs must lock before it ends. Finally, after the 3rd packet ends, the chip switches from RX to TX mode, and LO_2 is used in open-loop to transmit a GFSK-modulated BLE-compliant packet in the desired channel.

Figure 30.7.2 shows the state diagram and waveforms for the transient operation of the transceiver detecting an ADV event, recovering the 8MHz reference, and then transmitting a packet. The process begins with the RX back-channel path enabled, scanning the 3 BLE ADV channels for a predefined advertising channel hopping sequence and packet length as in [7]. These channels are CH37, CH38, and CH39 at 2402, 2426, and 2480MHz, respectively. LO_1 hops between channels every 50µs to oversample and detect the energy of ADV packets. Since the BC RX is only scanning for energy in the ADV channels, the LO frequency accuracy is relaxed, and the ADV event can be detected with LO_1 hopping open-loop. In addition, using direct conversion simplifies the baseband filtering and gain and reduces this path's power consumption. Once the BC demodulator detects the intended ADV event by correlating the digitized signal with programmable templates, the receiver switches to the 2nd RX path to recover a clock reference from the last incoming packet. This ensures that neither of the two PLLs are enabled until a valid ADV event is detected, eliminating false wakeups and erroneous transmissions.

In the clock recovery path, the BLE packet is downconverted to an IF of 8MHz and filtered by a 6th-order BPF with a bandwidth of 2MHz, removing interferers on adjacent channels. This filter is trimmed only once for process variation. A glitch filter removes short pulses that might exist, e.g. from noise. This signal then becomes the reference for the 2 PLLs, only present while receiving the packet. An 8MHz reference is sufficient for a combined PLL lock time less than one ADV packet, meaning the TX LO is ready before the end of the ADV event. 8MHz also relaxes the required BPF center frequency and quality factor. Using two LOs allows for receiving and transmitting on different BLE channels and for optimizing each PLL controller.

Figure 30.7.3 shows a simplified block diagram for both PLLs for reference recovery from the BLE packet and TX transmission. It is a type-I ADPLL with an embedded averaging processing unit (APU) to calibrate the digital control word (DCW) while the PLL is locked. The APU is required because the 8MHz reference is a data-whitened, GFSK-modulated BLE packet, and the FM needs to be removed. The frequency accuracy increases with increasing averaging time, and with enough PLL cycles, the influence from GFSK modulation is minimized. The PLLs in the RX/TX paths are controlled by different frequency control words (FCW) and work at separate frequencies. This reduces mutual coupling between the 2 LOs and enables the TX to transmit in any channel. The LC oscillator (Fig. 30.7.3) uses both NMOS and PMOS cross-coupled pairs for negative resistance and a digitally tuned resistor tail, which helps keep the transistors out of triode and improves phase noise. The 6th-order active RC BPF is synthesized by cascading three 2nd-order biquads (Fig. 30.7.3). Each biquad stage is fully differential using the Tow-Thomas topology for its lower sensitivity to parastics. In TX mode, a switched-capacitor digital PA [8] improves efficiency at low power levels.

The transceiver was fabricated in a 40nm CMOS process. The measured sensitivity is -86dBm at a BER of 10^{-3} (Fig. 30.7.4). The SIR when receiving back-channel messages (Fig. 30.7.4) was measured to be -18dB, -51dB, and <-60dB for the 1st, 5th, and 10th adjacent channels, respectively, meeting the BLE specifications for blocker rejection. The SIR when recovering a reference clock is -20dB and <-60dB for the 1st and 2nd adjacent channels, respectively. The NF of the clock recovery path is less than 12dB. This is critical to minimize RMS jitter in the recovered clock, which is measured at 6.5ps and is comparable to crystal oscillators operating at similar frequencies. The GFSK TX output spectrum is shown in Fig. 30.7.5 along with the BLE spectral mask. The measured eye diagram of the TX output packet is shown in Fig. 30.7.5, where the clock driving the GFSK modulator is divided down from open-loop RX LO_1. The free-running LC oscillator archives -117dBc/Hz phase noise at 1MHz offset. The overall power breakdown of the TRX shows that the RF LOs and buffers consume the highest power percentage (37%) of the total active power of 2.7mW.

Figure 30.7.6 shows a comparison between this work and state-of-the-art. This paper reports a new symmetric crystal-less transceiver, where both the received and transmitted messages are compliant with the same communication standard (BLE). This work has the fastest reported frequency calibration time of all crystal-less radios in the comparison table. It outperforms previous designs in interference rejection through high-Q filtering and by enabling PLLs only after detecting a valid ADV event when a BLE packet is known to be present. Figure 30.7.7 shows the die micrograph of the chip, which has an area of 1.33mm^2.

Acknowledgements:
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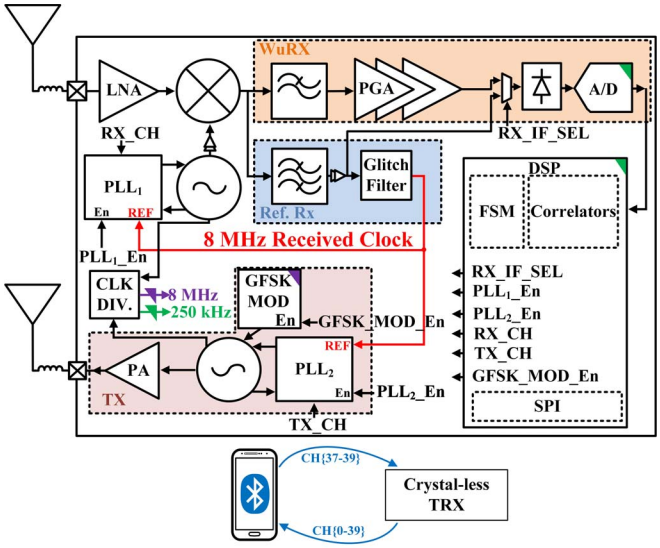

Figure 30.7.1: Block diagram of the crystal-less transceiver.

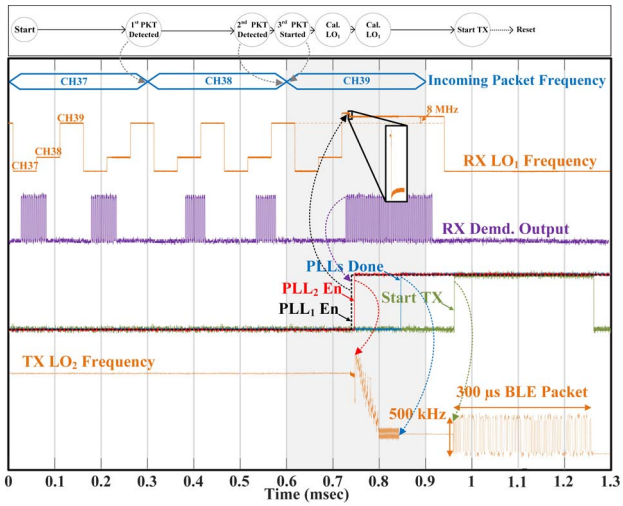

Figure 30.7.2: TRX operation state diagram. Measured waveforms of the TX/RX LO frequencies calibrations and sending of one BLE advertising packet afterwards.

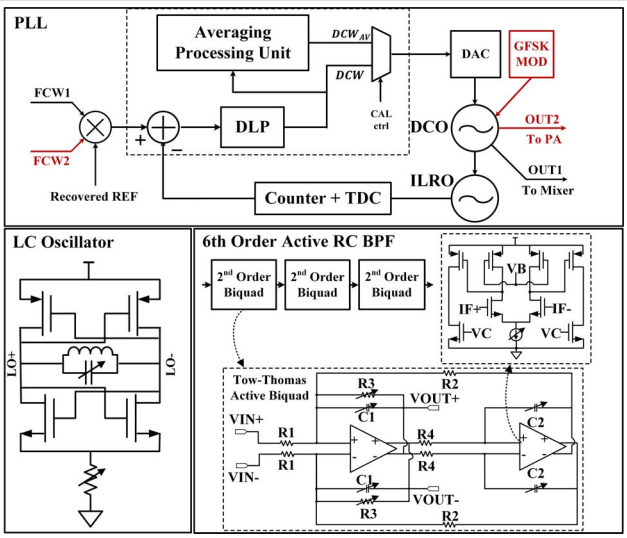

Figure 30.7.3: PLL block diagram. LC oscillator and BPF circuits (bias and CMFB are not shown).

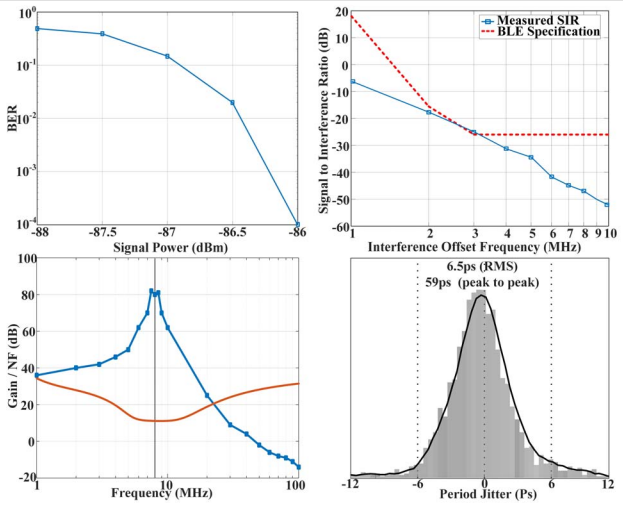

Figure 30.7.4: Measurement results: receiver BER vs. signal Power, signal-to interference ratio vs. interference offset frequency, RF front-end + NF gain and NF, received 8 MHz clock jitter.

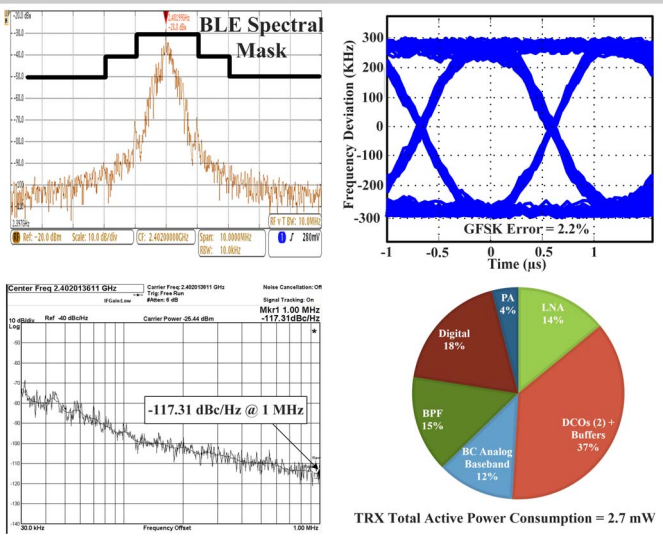

Figure 30.7.5: Measurement results: TX output spectrum, eye diagram, phase noise, transceiver power breakdown.

		This Work		VLSI 2019 [5]	VLSI 2019 [3]	TCAS-I 2012 [4]
		TX	RX			
Active Power [mW]	Analog	0.6	1.6	1.877	3.9	20.4
	Digital	0.5				
RF Frequency [MHz]		2402-2480	2402-2480	2400	2400	2400
Voltage Supply [V]		0.9/1		1.5	1.3-1.6	1.8
Sensitivity [dBm]		N/A	-86	-83.5	N/A	-65
Modulation		GFSK	BC-FSK	GFSK(TX)/ OQPSK(RX)	GFSK	QPSK
Die Area [mm²]		1.33		3.06	N/A	2.7
BLE Compatible Frequency Hopping		YES		No	No	No
Adjacent Channel SIR (dB) @ 2/3MHz		N/A	-18/-24	N/A	N/A	N/A
Channel Selectivity		N/A	Yes	Yes	N/A	No
Technology [nm]		40		65	65	180
Frequency Calibration Method		Received BLE Packet		Received 802.15.4 Packet	FBAR	Received QPSK Signal
Frequency Locking Time [µs]		< 100		N/A	N/A	800000
Comm. Standard (TX/RX)		BLE/ BC-BLE		BLE/ 802.15.4	BLE/ N/A	No/ N/A
Fully Integrated		Yes		Yes	No	No

Figure 30.7.6: Comparison with state-of-the-art crystal-less radios.

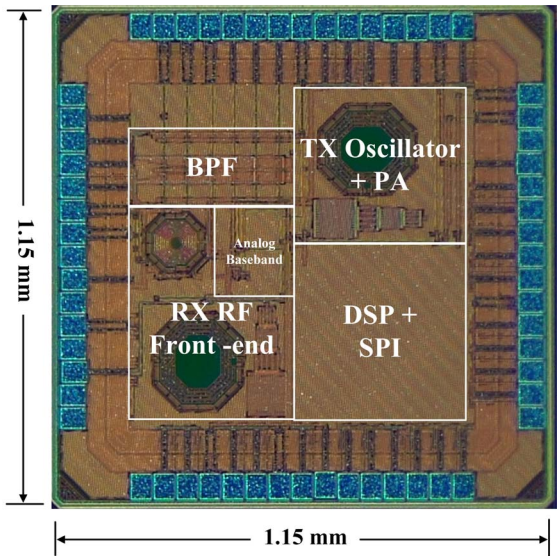

Figure 30.7.7: Die micrograph.

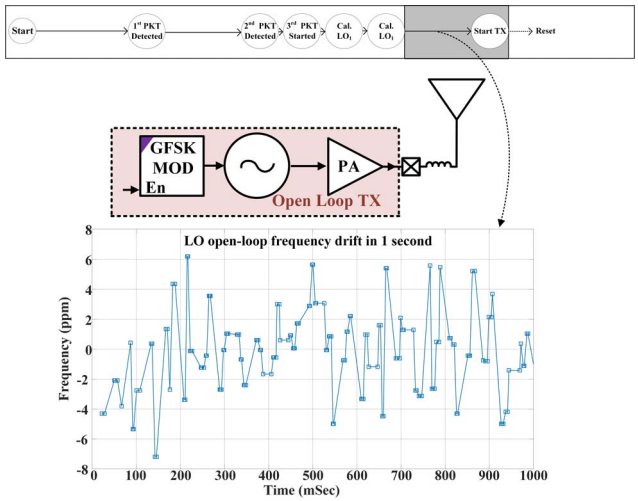

Figure 30.7.S1: LC LO running open-loop measured drift in 1 minute is less than ± 7 ppm (± 17.5 KHz) which is much less than the BLE requirement of ± 50 kHz in 300 μs.

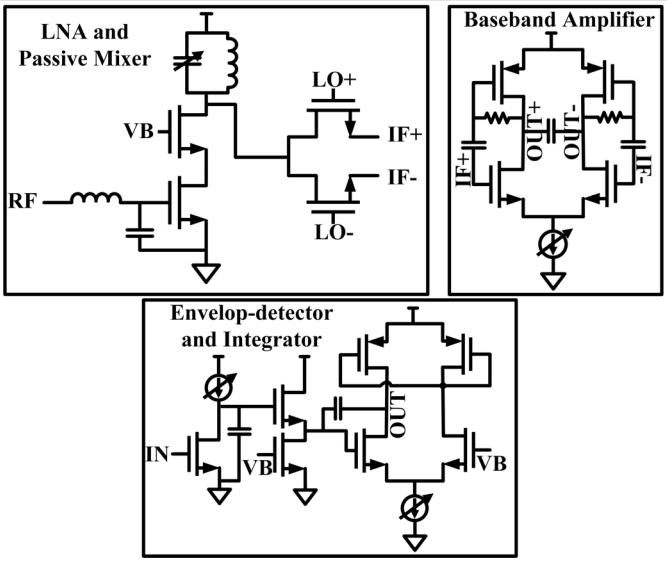

Figure 30.7.S2: Baseband Circuits (Bias is not shown).

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