High Performance of Wallace Tree Multiplier Stacking Circuit

M.VenkataRamanaiah, G.Anjaneyulu, Sudhakar Alluri

Abstract: ***In this paper one novel double counter proposed which is quick when contrasted with another normal's parallel counters. First, we are designing binary counter using solely full adders, and after with new symmetric stacking method. We are evaluating these two techniques and displaying how the symmetric stacking method is decreasing the x-or gate delays in the essential route of the binary counter. This kind of our proposed counter is very useful in the existing counter based totally Wallace tree multiplier design. With this new symmetry stacking counter we are lowering delay and increasing the performance of multipliers in VLSI circuits. We are designing and simulating our proposed quick binary counter using Xilinx ISE layout suite14.7.***

Index Terms**: *Counter, high speed, low power, multiplier, Wallace tree, VLSI.***

I. INTRODUCTION

To sketch a first-rate computational unit in VLSI circuits we need quick and environment friendly multipliers and adder units. Especially in multipliers after generating the partial merchandise including of these partial merchandise play an important function to determine the efficiency of the total computational unit. To velocity up the addition of partial merchandise in multiplier graph we are the use of 1/2 adders, full adders as proven in figure1.One full adder makes 3 input operands into two output operands. we are designing these full adders by the usage of x-or gates. But these XOR gates take a lot of time to compute the data. We can also add partial merchandise using specific full adders which are designed with two 2:1 MUX and one XOR gate. So that we can reduce the extend by way of the use of this one of a kind adder two.

II. LITERATURE REVIEW

In order to combine the partial products efficiently, column compression is commonly used. Many methods have been presented to optimize the performance of the partial product summation, such as the well-known row compression techniques in the Wallace tree [1] or Dadda tree [2], or the improved architecture in [3]. These methods involve using full adders functioning as counters to reduce groups of 3 bits of the same weight to 2 bits of different weight in parallel using a carry-save adder tree. Through several layers of reduction, the number of summands is reduced to two, which are then added using a conventional adder circuit. To achieve higher efficiency, larger numbers of bits of equal weight can be considered. The basic method when dealing with larger numbers of bits is the same: bits in one column are counted, producing fewer bits of different weights. For example, a 7:3 counter circuit accepts 7 bits of equal weight and counts the number of "1" bits. This count is then output using 3 bits of increasing weight. The 7:3 and 6:3 counter circuits can be constructed using full and half adders, as shown in Fig. 1. Much of the delay in these counter circuits is due to the chains of XOR gates on the critical path. Therefore, many faster parallel counter architectures have been presented. A parallel 7:3 counter was presented in [4] and used to design a high speed counter based Wallace tree multiplier in [5]. Additionally, counter designs as in [6] and [7] use multiplexers to reduce the number of XOR gates on the critical path. Some of these MUXs can be implemented with transmission gate logic to produce even faster designs.

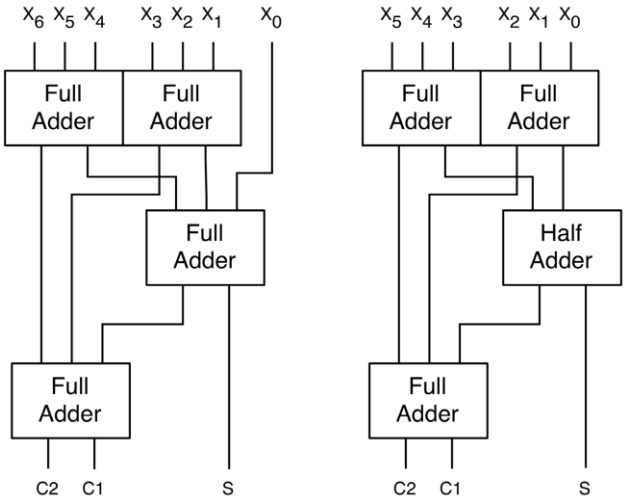

Figure 1: A 7:3 & 6:3 counters worked from half adders & full adders.

III. DESIGN METHODOLOGIES

3.1 The Fast Multiplication Process

The quickly multiplication process consists of three steps Partial product generation, Partial product discount and Final lift propagating addition. Various recording schemes are used to limit the wide variety of partial products. Compressors have been broadly used for discount method which generally contributes the most to the delay, power and region of the multiplier. To reap a better performance, the use of greater order compressors alternatively

Revised Manuscript Received October 05, 2019

M. Venkata Ramanaiah, Department of ECE, CMR Institute of Technology, JNTUH, Hyderabad, T.S, India
G. Anjaneyulu, Department of ECE, CMR Institute of Technology, JNTUH, Hyderabad, T.S, India.
Sudhakar Alluri, Department of ECE, CMR Institute of Technology, JNTUH, Hyderabad, T.S, India.

of conventional compressors, e.g. 3:2 compressors, have been considered. The reduction procedure subsequently outcomes in a 2-row matrix, and then a high- speed adder is used to get the ultimate result from the two rows. Several kinds of implementation primarily based on the conventional 6:3 structures proposed as used for quickly multiplication or a couple of addition applications. In this we are the use of the binary counter which is designed with bit stacking technique to add the partial products in a multiplier. First we to tend to gift Associate in Nursing as well as strategy that utilizes bit stacking circuits joined by technique for a totally distinctive system of consolidating two little stacks to make larger stacks. A 6:3 counter made-up utilizing this technique utilizes no XOR doors or multiplexers on its important approach. Very-large-scale integration recreation impact demonstrate that our 6:3 counter is at any rate half-hour speedier than existing counter plans whereas what is heaps of the employment of less power. The indistinguishable counter-based Wallace vary format was once used for every reenactment, whereas the among counters was once shifted. Utilization of the planned counter improves vary viably for Goliath circuits, yielding 64-and 128-piece multipliers that area unit each quicker and expend a large number less vitality than outstanding counter based absolutely Wallace (CBW) structures.

3.2 Three -Bit Stacking Circuit

3.2.1Consolidating 3 Bit Stacks into 6 Bit stack

Given inputs and outputs of stack is given as followsX0, X1, and X2 Y0, Y1, and Y2

We are getting outputs as follows

- Y0 = X0 or X1 or X2
- Y1 = X0X1 + X0X2 + X1X2
- Y2 = X0X1X2.

Namely, the first output will be “1” if any of the inputs is one, the second output will be “1” if any two of the inputs are one, and the last output will be 1. The stacking circuit appeared at Figure 2. In the above instance first we are the use of 2 three bit stacks at first level. In the output of first stage stacks we are getting two sequences of 1’s and two zeros. it is not appropriate stack alignment. So now we are interchanging the bits of one stack then we are getting one team of 1’s surrounded by means of two zeros as shown in figure3..it is additionally no longer perfect two stack alignment .so this time we are the utilization of two another couple of 3- bit stacks. Now we are getting our required stack alignment all 1’right-hand aspect and all 0’s are on left-hand side.

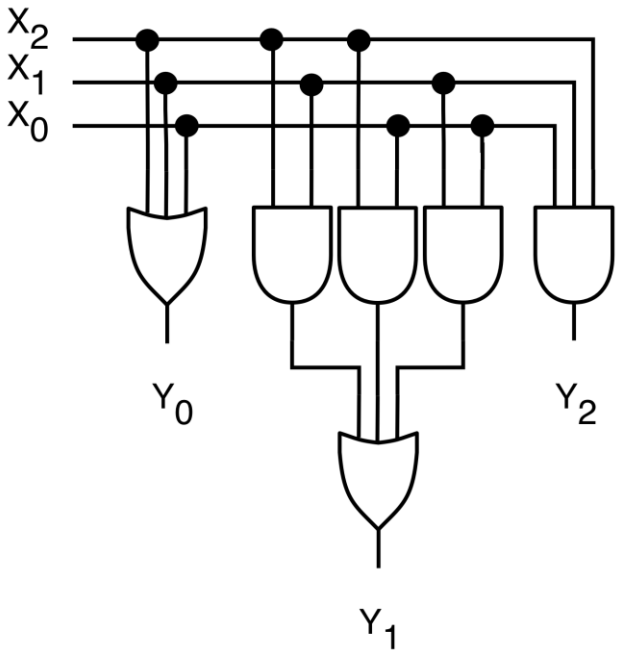

Figure 2: Three-bit stacker circuit

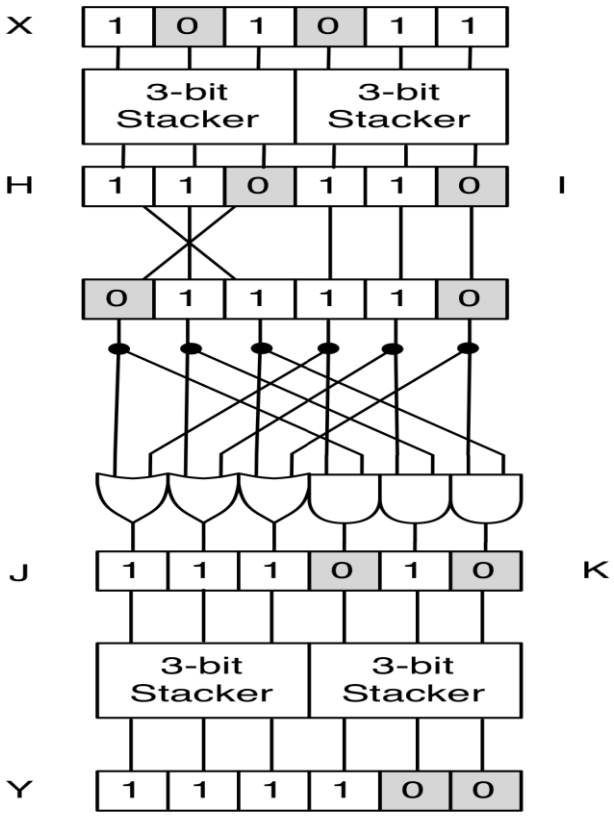

Figure 3: Example of 6-bit stacking

3.3 Changing over piece stack to paired number

We have to convert the above 6-bit stack into a binary number. For higher appreciation two we are the usage of intermediate values H ,I,K and labeling inputs as x0.x1,x2,x3,x4,x5 and outputs as S,C1,C2. We can calculate S by using the formula.

$$S = H_e \oplus I_e$$

Where He= Even parity which occurs if zero or two “1” bits appear in X0, X1, andX2.

$$C = (H_1 + I_1 + H_0 I_0)(K_0 + \overline{K_1} + K_2) + H_2 I_2 \quad (1)$$

Here ($H_1 + I_1 + H_0 I_0$) indicates in any event two information sources we have to see piles of length two from either top-level Stacker, or two heaps of length 1, $k_0 + \overline{k_1} + k_2$ indicates we tend to don't have quite Three inputs set, we tend to merely get to check that that none of the K bits is about because the K vectors solely set once quite Three inputs square measure "1," H2 I2 indicates if we've got all six inputs as "1." we square measure able to check this by checking that everyone three of each the H and that i bits are Set. As these squares measure bit stacks, we tend to merely check the right but within the stack for this case, we will simply calculate C2 because it ought to be set whenever we've got At least 4-bitsete can calculate c2 as C2 = K0 + K1 + K2. C2=1 if at least 4bits are 1

By using the above we can design one 6:3 counter except using x-or gate in the necessary path. In this the major drawback is wiring complexity. When in contrast to typical binary counter with the full adder in this we are using greater wires

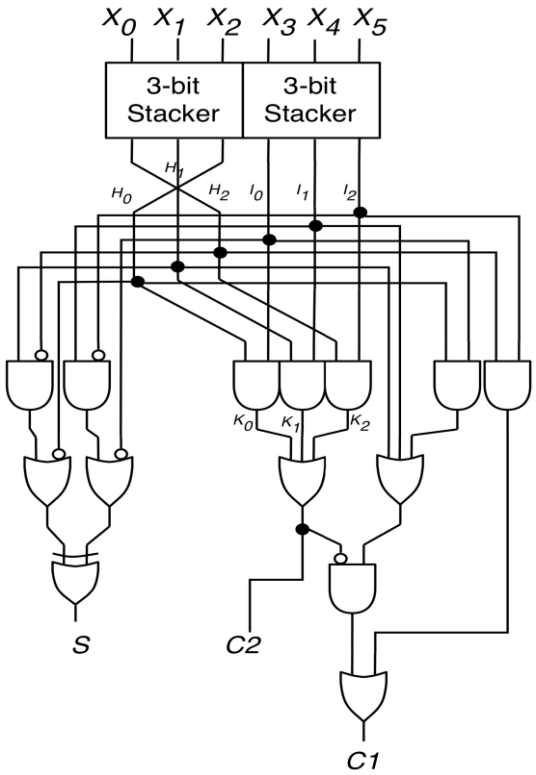

Figure 4: A Six: Three counter dependent on symmetric stacking.

$$P_{Static} = I_{Static} * v_{dd} \quad (2)$$

$$P_{Dynamic} = \alpha * c_L * v_{dd}^2 * f \quad (3)$$

$$P_{Shortcircuit} = I_{SC} * v \quad (4)$$

$$P_{Leakage} = V_{dd} * (I_S + I_G + I_D) \quad (5)$$

$$P_{Total} = P_{Dynamic} + P_{Leakage} \quad (6)$$

$$P_{Total} = (\alpha * c_l * v_{dd}^2 * f) + V_{dd} * (I_S + I_G + I_D) \quad (7)$$

3.4 Proposed Wallace Multiplier

In Wallace multiplier halfway items are spoken to with explosion as appeared in the Figure 5. The privilege most sections is called segment 0. The counters in every segment are spoken to by the containers around the speck items. The container encasing speaks to 3:2 and 2:2 counters. The stages are isolated by a thick even line. Partial products are reduced in each stage and added finally to get the final product. The Figure 5 shows the dot diagram of a 16 ×16 conventional multiplier.

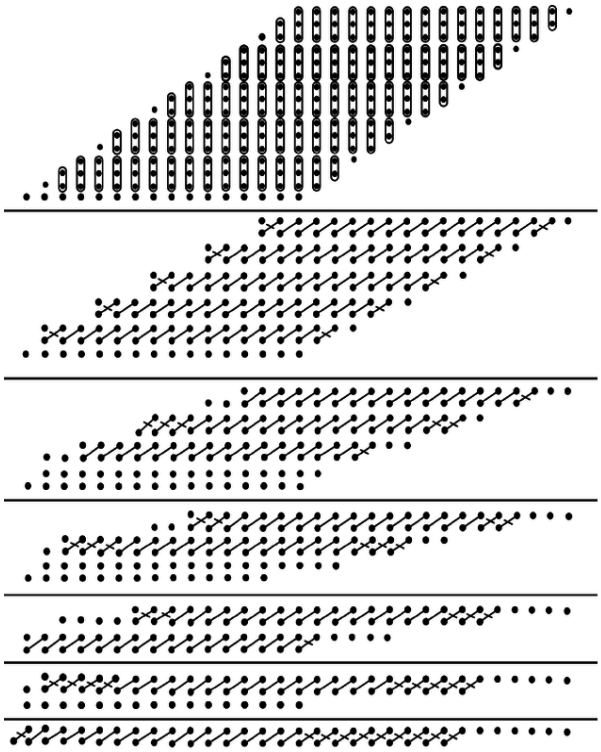

Figure 5: proposed Wallace Multiplier

3.5 Proposed Based Wallace Multiplier(CBW)

The dot documentation is employed to talk to the fractional results of the CBW number talked concerning during this phase as appeared in Figure. The privilege most section is termed phase zero. The counters in each phase square measure spoken to by the containers round the dab things. The instrumentation encasing seven, six, five, four, three, and 2 spots speaks to 7:3, 6:3, 5:3, 4:3, 3:2, and 2:2 counters, separately. The stages square measure isolated by a thick level line. the planning of CBW number depends on the keen utilization of speedy counters. The Figure 6 demonstrates the dab define of a sixteen ×16 CBW number.

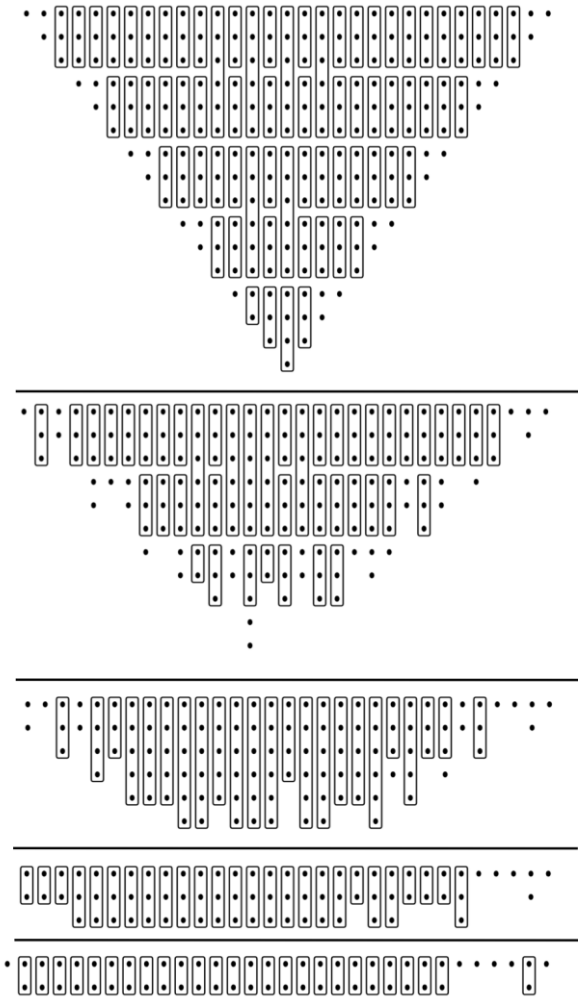

Figure 6:Counter Based Wallace Multiplier

To show Associate in Nursing utilization instance of the planned 6:3 counter, variety circuits varied of assorted sizes were built utilizing various at intervals counters. No new variety configuration is proposed; rather, existing designs unit recreated with varied interior counters. For reference, an everyday Wallace variety was dead for each size. At that point, the counter-based Wallace variety was wont to that accomplishes the tiniest quantity decrease stages. the interior 7:3 and 6:3 counters used for this counter based mostly Wallace variety was differentiated. The 5:3 and 4:3 counters were robust the proportionate for every variety, utilizing the counter plans. By virtue of the effectiveness of the 6-bit type of the organized counter, for will increase utilizing the uncounted-based counter, we have a tendency to to tend to utilize the 6-bit adaptation with no 7:3 counters, despite the very fact that these outcomes in one further decrease stage for each size. A case of a CBW variety decrease variety that utilization up to 6:3 counters for 16-bit info sources is appeared in Figure seven.

Example for 16*16 Counter Based Wallace Multiplier Using 6:3 Counters:

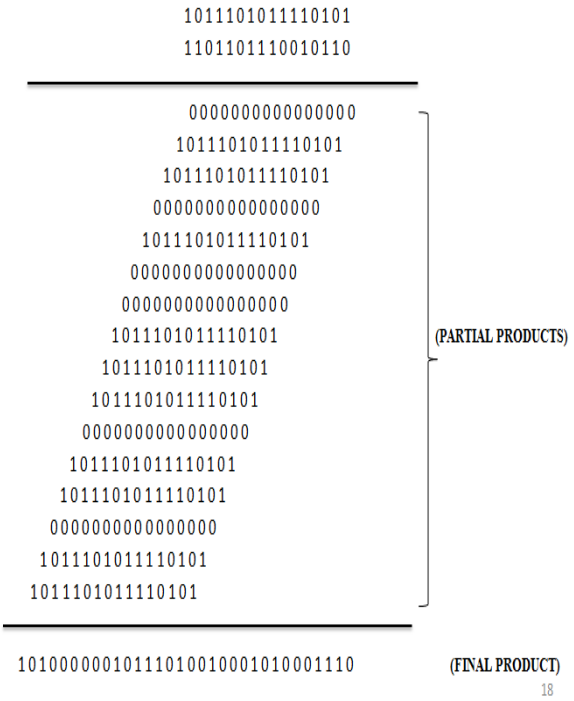

Figure 7:Example for 16*16Multiplications

An example for general 16*16 multiplication is shown in the Figure 7. It is the general binary multiplication with partial and final products. Later these partial products are changed to inverted pyramid model as shown in the Figure 8. The container encasing seven, six, five, four, three, and two numbers speaks to 7:3, 6:3, 5:3, 4:3, 3:2, and 2:2 counters, separately. Counter based Wallace Multiplier in each stage is diminished to acquire the last item as appeared in the Figure 8.

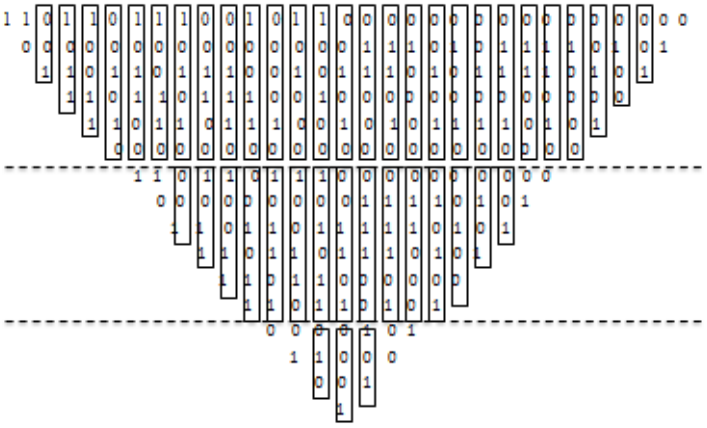

Figure 8: Counter Based Wallace Multiplier using 6:3 counters-example

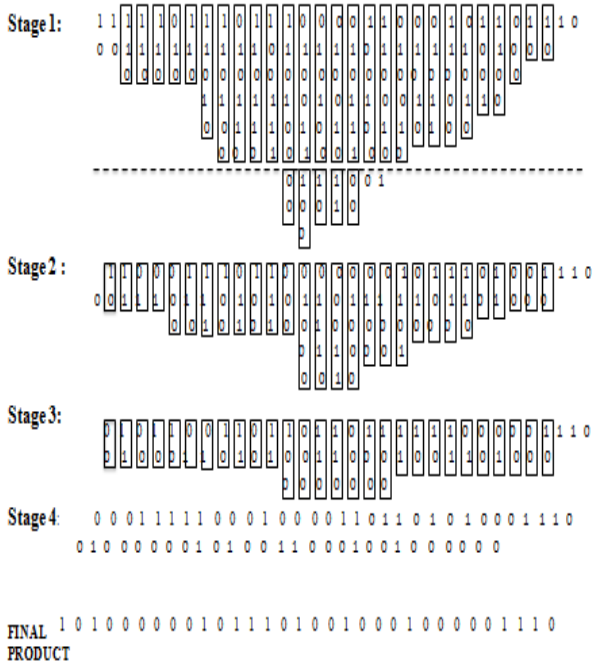

Figure 9:Counter Based Wallace Multiplier in every stage

As shown in the figures 8 and figure 9, 8-bit, 16-bit, 32-bit, 64-bit Wallace multipliers are implemented using counters based on symmetric stacking. These Wallace multiplier based on symmetric stacking are compared with Wallace multiplier without Symmetric Stacking. Therefore 8- bit, 16-bit, 32-bit, 64-bit Wallace multiplier implemented using counters based on symmetric stacking which results in less delay and power consumption.

IV. SIMULATION RESULTS

Table1: 6:3 Counter Simulation Results

Design	Delay(ns)	Avg. Power(µw)	Transistors
CMOS Full adder	2.9	124	102
Parallel Counter [4]	2.2	181	158
Mux-Based [6]	1.8	158	112
Conventional	1.4	146	124
proposed	1.3	115	95

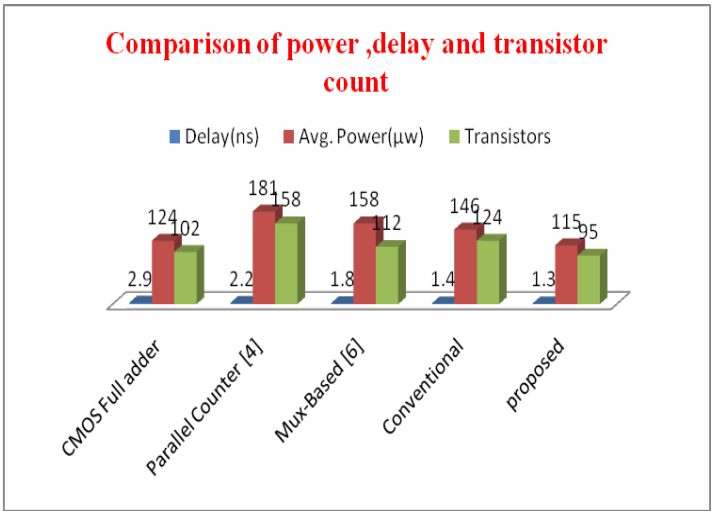

Figure 11: Comparison of power ,delay and transistor count

Utilizing (12)– (14), the last 6:3 counter circuit will be developed, as appeared in Figure 10. Utilizing larger CMOS entryways, the fundamental approach deferral is diminished to seven essential doors. As there are not any XOR doors on the fundamental approach, these 6:3 counter outflanks existing structures as appeared in table 1. One drawback of this structure is Associate in Nursing growth in the wiring intricacy: we to tend to see from figs. Three and four that the Rhombodera methodology needs a sign intersection when the first layer of stickers, whereas typical counters, as in Figure 10, do not have identical variety of running into one another.

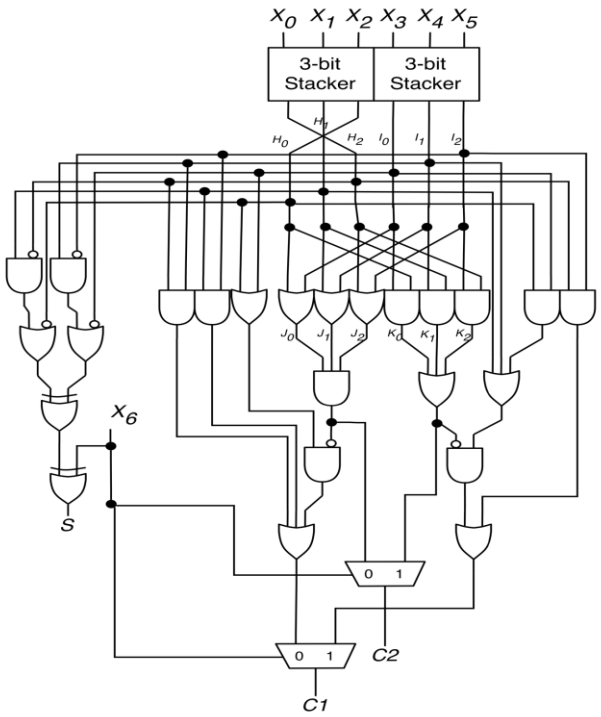

Figure 10: A 7:3 counter based on symmetric stacking.

The planned 6:3 counter structure was worked as a regular CMOS arrange and reenacted utilizing apparition, utilizing the ON semiconductor C5 zero.5-µm method (in the past AMI06). For examination, a 6:3 counter arrange was actualized utilizing customary CMOS full adders as in Figure 10. The parallel counter arrange

from [4] was modified over to a 6:3 counter and reenacted too. it's a basic approach deferral of three XOR + 2basicgates. The MUX-based counter arrange from [6] was to boot recreated. it's a basic approach deferral of XOR + 3_MUX. 2 of the MUXs on the polar approach will be actualized with transmission door explanation that is somewhat faster. The planned 6:3 counter has no XOR doors or MUXs on its basic approach. it's a basic approach postponement of seven essential doors.

Table 2: 7:3 Counter Simulation Results

Design	Delay(ns)	Avg. Power(µw)	Transistors
CMOS Full adder	3.0	222	112
Parallel Counter [4]	2.3	266	178
Mux-Based [6]	2.1	278	120
Conventional	1.8	282	194
proposed	1.7	210	105

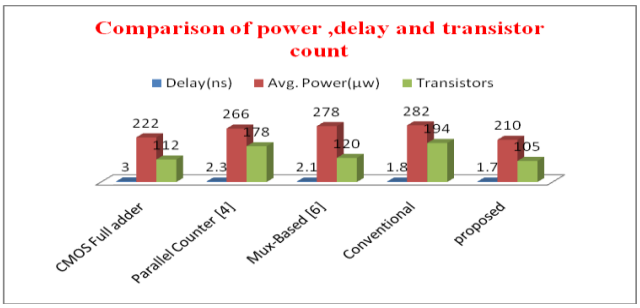

Figure 12: Comparison of power ,delay and transistor count

Table 3 Multiplier simulation results

Delay(ns)					Avg power (mw)				Area(Transistors)(k)			
Size	wallace	[5]	[6]	Stack	wallace	[5]	[6]	stack	Wallace	[5]	[6]	Stack
8	5.6	5.8	4.5	5.9	6.0	5.1	5.5	5.3	1.3	1.3	1.2	1.2
16	10.9	11.4	10.8	11.1	21.5	24.3	24.8	24.3	5.1	5.9	5.0	5.2
32	11.8	12.9	12.6	11.2	86.9	102	111	94.9	20	24	19	21
64	14.7	14.4	13.8	12.9	326	423	453	383	76	99	73	86
128	19.7	19.1	17.7	15.3	1253	1719	1826	1541	305	400	301	344
256	25.7	25.5	22.4	20.4	2150	3091	3215	2741	540	700	532	545

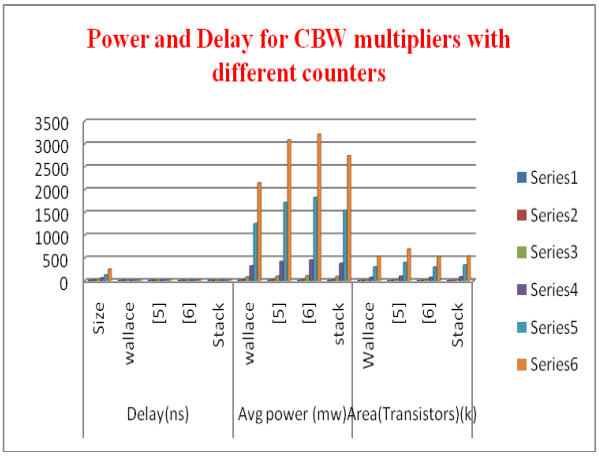

Figure 13: Power and Delay for CBW multipliers with different counters

V. CONCLUSION

In this we have designed 6:3 binary counter using symmetric stacking approach, and in contrast the parameters such as extend and region of two the proposed counter with usual counters like the parallel counter ,MUX primarily based counter and full adder based totally counters. We run all the types of counters using Xilinx ISE suit14.7 and presented the results. We approved that 6:3 counters completed with this bit stacking strategy accomplish higher speed than numerous lot of noteworthy request counter structures where as decreasing quality utilization. This can be owing to the absence of XOR entryways and multiplexers on the important approach. The 64-bit and 128-piece counter primarily based Wallace tree multipliers invented utilizing the planned 6:3 counters.

REFERENCES

1. C. S. Wallace, "A suggestion for a fast multiplier," IEEE Trans. Electron. Comput., vol. EC-13, no. 1, pp. 14–17, Feb. 1964.
2. L. Dadda, "Some schemes for parallel multipliers," Alta Freq., vol. 34, pp. 349–356, May 1965.
3. Z. Wang, G. A. Jullien, and W. C. Miller, "A new design technique for column compression multipliers," IEEE Trans. Comput., vol. 44, no. 8, pp. 962–970, Aug. 1995.
4. M. Mehta, V. Parmar, and E. Swartzlander, "High-speed multiplier design using multi-input counter and compressor circuits," in Proc. 10th IEEE Symp. Comput. Arithmetic, Jun. 1991, pp. 43–50.
5. S. Asif and Y. Kong, "Design of an algorithmic wallace multiplier using high speed counters," in Proc. IEEE Comput. Eng. Syst. (ICCES), Dec. 2015, pp. 133–138. This article has been accepted for inclusion in a future issue of this journal. Content is final as presented, with the exception of pagination. IEEE Transactions on Very Large Scale Integration (VLSI) Systems 5
6. S. Veeramachaneni, L. Avinash, M. Krishna, and M. B. Srinivas, "Novel architectures for efficient (m, n) parallel counters," in Proc. 17th ACM Great Lakes Symp. VLSI, 2007, pp. 188–191.
7. S. Veeramachaneni, K. M. Krishna, L. Avinash, S. R. Puppala, and M. B. Srinivas, "Novel architectures for high-speed and low-power 3-2, 4-2 and 5-2 compressors," in Proc. 20th Int. Conf. VLSI Design Held Jointly 6th Int. Conf. Embedded Syst. (VLSID), Jan. 2007, pp. 324–329.
8. G. OKLOBDZIJA, D. VILLEGER, AND S. S. LIU, "A METHOD FOR SPEED OPTIMIZED PARTIAL PRODUCT REDUCTION AND GENERATION OF FAST PARALLEL MULTIPLIERS USING AN ALGORITHMIC APPROACH," IEEE TRANS. COMPUT., VOL. 45, NO. 3, PP. 294–306, MAR. 1996.
9. S. Asif and Y. Kong, "Analysis of different architectures of counter based Wallace multipliers," in Proc. 10th Int. Conf. Comput. Eng. Syst. (ICCES), Dec. 2015, pp. 139–144.

10. J. Gu and C.-H. Chang, “Low voltage, low power (5:2) compressor cell for fast arithmetic circuits,” in Proc. IEEE Int. Conf. Acoust., Speech, Signal Process. (ICASSP), vol. 2. Apr. 2003, pp. 661–664.
11. K. Prasad and K. K. Parhi, “Low-power 4-2 and 5-2 compressors,” in Proc. Conf. Rec. 35th Asilomar Conf. Signals, Syst. Comput., vol. 1. Nov. 2001, pp. 129–133.
I. Koren, Computer Arithmetic Algorithms, 2nd ed. Natick, MA, USA: A. K. Peters, 2002.
12. M. Rouholamini, O. Kavehie, A.-P. Mirbaha, S. J. Jasbi, and K. Navi, “A new design for 7:2 compressors,” in Proc. IEEE/ACS Int. Conf. Comput. Syst. Appl., May 2007, pp. 474–478.
I. Dandapat, S. Ghosal, P. Sarkar, and D. Mukhopadhyay, “A 1.2-ns 16 × 16-bit binary multiplier using high speed compressors,” Int. J. Elect. Electron. Eng., vol. 4, no. 3, pp. 234–239, 2010.
13. D. Radhakrishnan, “Low-voltage low-power CMOS full adder,” IEE Proc.-Circuits, Devices Syst., vol. 148, no. 1, pp. 19–24, Feb. 2001. [16] S.-F. Hsiao, M.-R. Jiang, and J.-S. Yeh, “Design of high-speed lowpower 3-2 counter and 4-2 compressor for fast multipliers,” Electron. Lett., vol. 34, no. 4, pp. 341–343, Feb. 1998.
14. K.Praveen Kumar, Kumaraswamy Gajula “Fractal Array antenna Design for C-Band Applications”, International Journal of Innovative Technology and Exploring Engineering (IJITEE), Volume-8 Issue-8 June, 2019.
15. K.Praveen Kumar, “Active Switchable Band-Notched UWB Patch Antenna”, International Journal of Innovative Technology and Exploring Engineering (IJITEE), Volume-8 Issue-8 June, 2019.
16. K.Praveen Kumar, “Circularly Polarization of Edge-Fed Square Patch Antenna using Truncated Technique for WLAN Applications”, International Journal of Innovative Technology and Exploring Engineering (IJITEE), Volume-8 Issue-8 June, 2019.
17. K.Praveen Kumar, “Triple Band Edge Feed Patch Antenna; Design and Analysis”, International Journal of Innovative Technology and Exploring Engineering (IJITEE), Volume-8 Issue-8 June, 2019.
18. K.Praveen Kumar, Dr. Habibulla Khan "Optimization of EBG structure for mutual coupling reduction in antenna arrays; a comparitive study" International Journal of engineering and technology, Vol-7, No-3.6, Special issue-06, 2018.
19. K.Praveen Kumar, Dr. Habibulla Khan "Active PSEBG structure design for low profile steerable antenna applications" Journal of advanced research in dynamical and control systems, Vol-10, Special issue-03, 2018.
20. K.Praveen Kumar, Dr. Habibulla Khan, "Design and characterization of Optimized stacked electromagnetic band gap ground plane for low profile patch antennas" International journal of pure and applied mathematics, Vol 118, No. 20, 2018, 4765-4776.
21. K.Praveen Kumar, Dr Habibulla Khan " Surface wave suppression band, In phase reflection band and High Impedance region of 3DEBG Characterization" International journal of applied engineering research (IJAER), Vol 10, No 11, 2015.
22. K.Praveen Kumar, Dr. Habibulla Khan " Active progressive stacked electromagnetic band gap structure (APSEBG) structure design for low profile steerable antenna applications" International Conference on Contemporary engineering and technology 2018 (ICCET-2018) March 10 - 11, 2018. Prince Shri Venkateshwara Padmavathy Engineering College, Chennai.
23. K.Praveen Kumar, Dr. Habibulla Khan "Optimization of EBG structures for Mutual coupling reduction in antenna arrays; A comparative study" International Conference on Contemporary engineering and technology 2018 (ICCET-2018) March 10 - 11, 2018. Prince Shri Venkateshwara Padmavathy Engineering College, Chennai.
24. K Satish Reddy a, K Praveen Kumar, Habibulla Khan, Harswaroop Vaish “Measuring the surface properties of a Novel 3-D Artificial Magnetic Material” 2nd International Conference on Nanomaterials and Technologies (CNT 2014), Elsevier Procedia material Science.
25. K.Praveen Kumar, "Mutual Coupling Reduction between antenna elements using 3DEBG" IEEE International conference on communication technology ICCT-April-2015. Noor Ul Islam University Tamilnadu.
26. K.Praveen Kumar, "The surface properties of TMMD-HIS material; A measurement" IEEE International conference on communication technology ICCT-April-2015. Noor Ul Islam University Tamilnadu.
27. K.Praveen Kumar, "Design of 3D EBG for L band Applications" IEEE International conference on communication technology ICCT-April-2015. Noor Ul Islam University Tamilnadu.
28. K.Praveen Kumar, "Effect of 2DEBG structure on Monopole Antenna Radiation and Analysis of It's characteristics" IEEE International conference on communication technology ICCT-April-2015. Noor Ul Islam University Tamilnadu.
29. K.Praveen Kumar, Dr Habibulla Khan " The surface properties of TMMD-HIS material; a measurement" IEEE International conferance on electrical, electronics, signals, communication & optimization EESCO - January 2015.
I. Venkateswar Rao, Praveen Kumar Kancherla, Sunita Panda “Multiband slotted Elliptical printed Antenna Design and Analysis” Journal Of Mechanics Of Continua And Mathematical Sciences (JMCMS), Vol.-14, No.-4, July-August (2019) pp 378-386.
30. Kumaraswami Gajula, Amulya Boyina, K. Praveen Kumar “Active Quad band Antenna Design for Wireless Medical and Satellite Communication Applications” Journal Of Mechanics Of Continua And Mathematical Sciences (JMCMS), Vol.-14, No.-4, July-August (2019) pp 239-252.
31. Amulya Boyina, K. Praveen Kumar “Active Coplanar Wave guide Fed Switchable Multimode Antenna Design and Analysis” Journal Of Mechanics Of Continua And Mathematical Sciences (JMCMS), Vol.-14, No.-4, July-August (2019) pp 188-196.