A review on GDI technique based analysis of Wallace multiplier

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***Abstract*: Multiplier is the most commonly used circuit in the digital devices. Multiplication is one of the basic functions used in digital signal processing. Most high performance DSP systems rely on hardware multiplication to achieve high data throughput. There are various types of multipliers available depending upon the application in which they are used. Gate diffusion input (GDI)—a new technique of low-power digital combinational circuit is design with Wallace tree multiplier, which is found to be much more power efficient in comparison with array multiplier design which ultimately reduces the power dissipation and improve the area of digital circuits while maintaining low complexity of logic design. The multipliers based on GDI cells are designed using EDA Tanner tool version 13, simulations are based on 90nm technology, where the transistor count is reduced using GDI technique.**

***Index term*-Wallace tree multiplier, Gate Diffusion Input, CMOS, Low Power.**

Introduction: The multiplier plays an important rolein most high speed Digital Signal Processing (DSP) and multimedia applications because it dominates the chip power consumption and operation speed. The power consumption, delay and area are always been an important design considerations for any chip designer. Many DSP structures incorporate multipliers in their design. Delay of the circuit inevitably changes with the delay of the multiplier. Therefore research is going on to reduce the delay of multiplier so that the delay of whole circuit can be reduce.

Wallace Multiplier: Wallace tree multiplier has been evolved as high speed and area efficient multiplier. The Wallace tree multiplier involves ANDing of multiplier and multiplicand bits for the generation of partial products. Any multiplier can be divided into three stages: Partial products generation stage, partial products addition stage, and the final addition stage. By reducing the number of partial products the speed of multiplication can be increased. Many high-performance algorithms and architectures have been proposed to accelerate multiplication. In second phase full adders and half adders has been used for the reduction of generated partial products in two rows. Followed by addition of two rows using fast carry adders in the third stage.

Why GDI?

The rapid development in portable digital applications, the demand for increasing speed, compact implementation, and low power dissipation triggers numerous research efforts.To improve the performance of logic circuits, we developed CMOS technology, which resulted in many logic design techniques, one form of logic that is popular in low-power digital circuits is pass-transistor logic (PTL). In the literature we proposed many PTL circuits. Main advantages of PTL over standard CMOS design are

1)because of the small node capacitances we get high speed,

2)number of transistors are reduced due to low power dissipation

3) andlower interconnection effects due to a small area. There are two basic problems for PTL implementations. First,there is reduced current and voltagebecausethe threshold drop across the single-channel pass transistorshence slower operation. It is important for low-power design to operate at the lowest possible voltage level. Second, the high input voltage level at the regenerative inverters is not, the PMOS device in the inverter is not fully turned off, and hence direct-path static power dissipation could be significant.

There are PTL techniques that solve the problems mentioned above.

1. Transmission gate CMOS (TG) uses it's logic to realize complex logic functions using a small number of complementary transistors. It will solve the problem of low logic level swing by using PMOS as well as NMOS.

2.Complementary pass-transistor logic (CPL) uses NMOS pass-transistor logic with CMOS output inverters. It's most important feature, which contribute to lowering the power consumptionis the small stack height and the internal node low swing. The CPL suffers from static power consumption due to the low swing at the gates of the output inverters. Different circuit styles like LCPL and SRPLare used to lower the power consumption of CPL circuits. These circuit styles containcross-coupled inverters or PMOS restoration transistors.

3. To reduce the dc power consumption, Double pass-transistor logic (DPL) uses complementary transistors to keep full swing operation. So the need for restoration circuitry is eliminated. Due to the presence of PMOS transistors large area used this is one of the disadvantage of DPL. The top-down logic design complexity is the additional problem of existing PTL, which prevents from capturing a major role of the pass transistors in real logic LSIs.For PTL-based designsimple and universal cell library is not

available is one of the main reasons for this. Now we present gate diffusion input (GDI) technique which solves most of the problems discussed above.
Using only two transistorsthe GDI approach allows implementation of a wide range of complex logic functions. ThiTo design fast, low-power circuits and reduced number of transistors (as compared to CMOS and existing PTL techniques) this method is very good. By using small cell library we can improve logic level swing and static power characteristics which allow simple top-down design.

BASIC GDI FUNCTIONS

The GDI technology is based on the simple cell as shown in Fig. 1. The basic cell reminds of the CMOS inverter, but there are some important differences.
1) The GDI cell has three inputs: (common gate input of NMOS and PMOS), P (input to the source/drain of PMOS), and N (input to the source/drain of NMOS).
2) Both bulks of NMOS and PMOS are connected to N or P (respectively), so it is biased at contrast with a CMOS inverter**.**

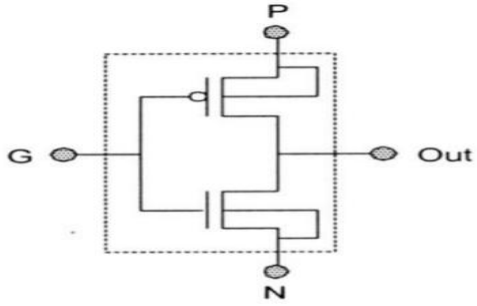


Fig 1: GDI basic cell. [9]

It must be noticed that not all of the functions are possible in standard p-well CMOS process but they can be successfully implemented in twin-well CMOS or silicon on insulator (SOI) technologies.

Literature Review

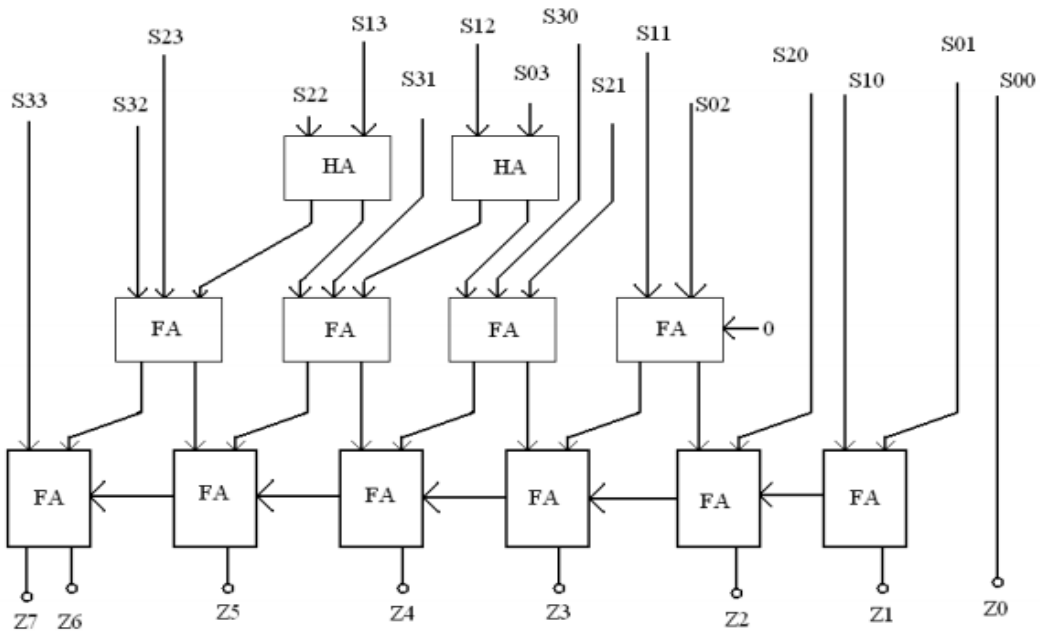
Kokila Bharti Jaiswal, Nithish Kumar, Pavithra Seshadri and Lakshminarayanan G[1], "Low Power Wallace Tree Multiplier Using Modified Full Adder", 2015 3rd International Conference on Signal Processing, Communication and Networking (ICSCN). In this paper, a modified full adder using multiplexers and XOR gate is proposed. By incorporating the modified full adder in the reduction stage of Wallace tree multiplier, an average power, area and delay reduction of 37.45% , 45.75% and 17.65% respectively, compared to existing methods respectively is achieved. The synthesis result confirms that the proposed Wallace tree multiplier is suitable for low power and small area applications.**Mohan Shoba, Rangaswamy Nakkeeran[2] ,"**GDI based full adders for energy efficient arithmetic applications**"**, Engineering Science and Technology, International Journal(2016). In this paper, three full adders having low power are designed using AND, OR and XOR gates to remove threshold voltage problem which is commonly found in Gate Diffusion Input (GDI) logic. This problem usually does not allow the full adder circuits to operate without additional inverters. However, the three full adders are successfully realized using gates with the significant improvementin their performance. The performance of these proposed designs is compared with the many other full adder designs, like CMOS, CPL, hybrid and GDI through SPICE simulations using 45 nm technology models.Simulation results reveal that proposed designs have lower energy consumption among all the conventional designs taken for comparison.**Vijaya Shekhawat, T.Sharma and Krishna G. Sharma[3]**,"2-Bit Magnitude Comparator using GDI Technique" IEEE International Conference on Recent Advances and Innovations in Engineering (ICRAIE-2014), May 09-11,2014, Jaipur, India. In this paper, performance of the proposed GDI magnitude comparator circuit with help of full adder logic has shown good performance in compare to existing conventional CMOS based design. The comparative performance of conventional CMOS and proposed GOI magnitude comparator with respect to power consumption at different range of input voltage, temperature and frequency has been discussed in above section. The smaller area of proposed GDI magnitude comparator results into shorter interconnects and thus less crosstalkenable more efficient placement and routing. Thus, it is concluded that proposed magnitude comparator based on GDI technique require less power and smaller area in comparison to CMOS magnitude comparator. Both the circuits are designed and simulated using Tanner EDA Tool version 12.6 at 45nm process technology.

Methodology

Wallace tree multiplier is a base paper and was designed on 90nm CMOS technology. Also it was designed with the help of Verilog. In this project we will not use Verilog, we will design Wallace tree multiplier in Tanner tool for the sake of comparison . We will maintain 90nm CMOS technology platform.

Process of Project

Block diagram of Wallace Tree is given as below



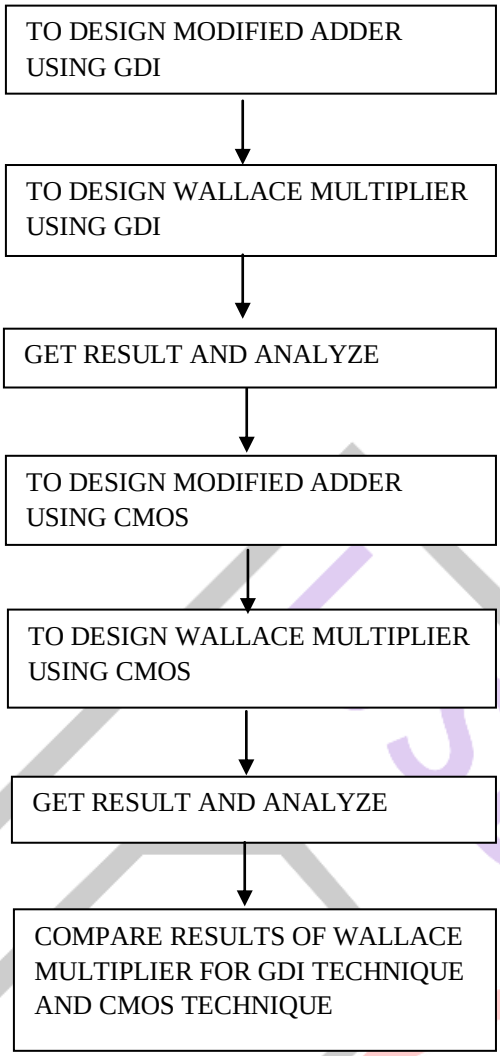
Wallace Tree Multiplier Structure

The Wallace tree multiplier provide low power dissipation for all possible input combinations but other multiplier cannot do that. Thus we design Wallace tree multiplier using GDI technique which reduces the power consumption. We use 90nm CMOS technology in our project.

The Wallace tree has three steps:

ANDing that is each bit of one of the arguments multiply by each bit of the other, yielding results. Depending on the position of multiplied bits, the wires can carry different weights b. Reduce the number of partial products to two by using full and half adders.c. Group the wires in two numbers, then add them with a conventional adder. Then if there are three or more wires with the same weight add a following layer.d. Take any three wires with the same weights and input them into a full adder. The result will be an output wire of the same weight and an output wire with a higher weight for each three input wires.e. If there are two wires of the same weight left, input them into a half adder.If there is just one wire left, connect it to the next layer.

FLOW OF PROJECT WORK



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[2] Mohan Shoba, RangaswamyNakkeeran, "GDI based full adders for energy efficient arithmetic applications" Elsevier, Engineering Science and Technology, an International Journal 19 (2016) 485–496
[3] VijayaShekhawat, Tripti Sharma and Krishna Gopal Sharma, "2-Bit Magnitude Comparator using GDI Technique"IEEE International Conference on Recent Advances and Innovations in Engineering (ICRAIE-2014), May 09-11, 2014, Jaipur, India
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