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Rotary Switch and Current Monitor by Hall-Based Microsystems

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CONTENTS

ABSTRACT

This thesis reports the development of two Hall-based microsystems: a rotary switch and a current monitor. These microsystems employ integrated CMOS Hall devices sensitive to fields either perpendicular or parallel to the chip-surface. In exploiting commercial IC technology, cost effective batch fabrication with well established reliability is utilized. Combined with dedicated packaging solutions, inexpensive microsystems with superior performance have been realized.

Following an introduction to the field of magnetic sensors, theoretical aspects relevant to the design of integrated Hall devices are discussed. This includes general performance figures of merit as well as compensation techniques for the sensor offset voltage. Two compensation methods are treated in more detail: offset reduction using the technique of continuous spinning current and through use of a double-Hall sensor. Furthermore, a numerical model is presented to predict device performance from fabrication process simulations.

The remaining part of the thesis deals with the fabrication and characterization of CMOS Hall sensors and associated application demonstrators. Lateral and trench-Hall devices, sensitive to magnetic fields perpendicular and parallel to the chip surface, respectively, are presented. Both devices yield excellent sensitivity of 200 to 300 V/AT and linearity from 0.01 to 0.1% in a ±0.3 T range. The low cross-sensitivity to out-of-plane magnetic induction makes trench-Hall devices well suited for vector field measurements.

The first demonstrator reported shows a rotary switch employing the vertical trench-Hall device. The application is intended for angular measurement of high accuracy in a harsh environment involving mechanical loading and a wide temperature range. The measurement principle implies a permanent magnet attached to an axis of rotation. By detecting the two components of the magnetic induction B_x and B_y parallel to the sensor chip surface, robustness against mechanical tolerances of the packaging is obtained. The demonstrator exhibits a resolution smaller than 0.2° over 360°. The second application example is a current monitor using lead-on-chip packaging technology. The entire system fabrication is in line with commercial IC mass manufacturing. The system features galvanically isolated current detection up to 20 A with an accuracy of 150 mA at 100 Hz.

ZUSAMMENFASSUNG

Im Zentrum dieser Arbeit stehen zwei Mikrosysteme: Ein Drehschalter und ein Stromsensor, deren Messprinzip auf integrierten Hall Sensoren beruht. Die Hall Sensoren, hergestellt in einem CMOS Fabrikationsprozess, weisen eine Sensitivität senkrecht oder parallel zur Chipoberfläche auf. Die Verwendung von IC-Technologie und massgeschneiderten Verpackungslösungen erlaubt eine kostengünstige Massenfabrikation bei gleichzeitig hoher Zuverlässigkeit.

Nach einer Einführung in das Gebiet der Magnetfeldsensoren werden theoretische Aspekte zur Funktion von integrierten Hall Sensoren diskutiert. Dabei handelt es sich um allgemeine Kenndaten der Sensoren und um Verfahren der Offset-Reduktion. Folgende Reduktionsverfahren werden erläutert: das 'Continuous Spinning Current'-Verfahren und das Verfahren mit einem Doppel-Hall Sensor. Weiter wird die Theorie zur Simulation eines Hall Sensors vorgestellt, welche als Randbedingung lediglich Daten aus Prozess-Simulationen benötigt.

Weitere Teile dieser Arbeit handeln von der Herstellung und Charakterisierung von CMOS Hall Sensoren, sowie deren Anwendung. Der verwendete laterale Hall Sensor weist eine Sensitivität von etwa 200 V/AT senkrecht zur Chipoberfläche auf (Linearität: 0.01% für ±0.3T). Der Trench-Hall Sensor reagiert auf magnetische Felder in der Chipebene mit einer Sensitivität von ca. 300 V/AT (Linearität: 0.1% für ±0.3T). Die starke Richtungsabhängigkeit der Sensitivität ermöglicht dabei eine Vektormessung des Magnetfeldes.

In dieser Arbeit wird ein Drehschalter vorgestellt, welcher auf Trench-Hall Sensoren basiert. Zur Winkelbestimmung wird die Richtung des Magnetfeldes gemessen, das von einem Permanentmagneten auf einer Achse erzeugt wird. Diese Methode erlaubt eine hohe Messauflösung kleiner 0.2° über einen Bereich von 360°. Dabei wird die Auflösung weder durch äussere mechanische Einflüsse, Temperaturänderungen oder Gehäusetoleranzen beeinträchtigt. Weiter wird ein Stromsensor vorgestellt, der mit dem 'Lead-On-Chip'-Verfahren hergestellt wurde. Der gesamte Herstellungsprozess deckt sich mit kommerziellen Halbleiter-Herstellungsmethoden. Mit dem vorgestellten Stromsensor können Ströme bis zu 20 A, mit einer Genauigkeit von 150 mA bei 100 Hz, galvanisch getrennt gemessen werden.

1 INTRODUCTION

1.1 State of the Art

Integrated microsensors offer unique features such as cost effective sensor batch fabrication, miniaturization with unique reliability, and co-integration of dedicated electronics [1, 2]. Integrated sensor development has been initiated decades ago with the introduction of photodiodes and Hall devices [3] in silicon technology. More recently piezoresistors have been introduced following the discovery of piezoresistivity in silicon [4]. By use of IC technology for sensor manufacturing [5], system cost and performance have gradually improved. Here, a fabrication scheme which combines conventional CMOS IC technology with additional processing steps has been successfully demonstrated [6, 7]. Preferably, additional post-processing steps, which include etching or thin film deposition, are performed after completion of the regular IC process sequence [8]. Also, CMOS pre-processing has been demonstrated [9] but this requires a close collaboration between the sensor designer and the IC manufacturer [6].

Technologies for microtransducers have been pushed to well established manufacturing standards. Bulk micromachining and surface micromachining have already become routine technologies [10, 11]. Also, new materials are introduced in the IC process enabling new features for sensor design. As an example, electroplating of different materials on a die manufactured in a CMOS process has been demonstrated [12]. The deposition of additional layers, such as polymers and piezoelectric films, in line with common IC technologies, has proven to be feasible [13, 14].

IC sensors are superior in many aspects compared to discrete solutions. Due to their potential for growth in the market place, increased research activities in industry and academic institutions is critical. Eventhough the latter is actively engaged in many aspects of microsystems research [15], technology transfer has yet to be fully exploited [16]. In order to enhance the transfer of technology, three promising methods are suggested: new start-up companies spinned-off from university research, recruitment of qualified engineers by companies, and university-industry collaboration in research projects [17].

1.2 Magnetic Field Sensors

A magnetic sensor converts a magnetic field into an electrical signal. In most applications magnetic sensors are used as tandem transducers [18, 19]. They detect a change or disturbance in the magnetic field caused by a non-magnetic physical signal. Examples of physical signals include position, linear and angular displacement, or an electrical current. Magnetic sensors can be classified in three broad categories: low-field sensors (nT-range), Earth's field sensors (μT), and bias field transducers (mT) (see Fig. 1.1) [20].

In many applications, magnetic sensing provides a means of rugged, reliable, and a maintenance free technology compared to other sensing techniques. Magnetic sensors exploit a broad range of physics and chemistry disciplines. There are many aspects, such as frequency response, size, and power, that could affect the choice of a particular sensor concept best suited for an application. A description of the various sensor types is described in the following.

Low-Field Sensors

The family of the low-field sensors includes superconducting quantum interference devices, fiber-optic magnetometers, optically pumped magnetometers, and search coil magnetometers.

The most sensitive low field sensor is the *superconducting quantum interference device* (*SQUID*) [21]. It is based on cooling a superconducting material below its transition temperature. In such materials, a magnetic field induces a current, which is not subject to any resistance. By introducing a Josephson contact in the superconducting ring, the current starts to oscillate as a function of the applied magnetic field. The sensor can respond to changes in the magnetic flux in the order of 10^{-13} T.

The *fiber-optic* magnetometer employs two glass fibers that are arranged as a Mach-Zender interferometer [22, 23]. One of the two fibers is coated with a magnetostrictive material whose dimensions change under the influence of a magnetic field, causing an interference pattern at the interferometer output. The fiber-optic magnetometer has a detection range from 10^{-10} to 10^{-3} T.

The optically pumped magnetometer is based on the Zeeman effect where the spectral lines of atoms are split when placed in a magnetic field. Here, light pass-

Sensor Technology	Detectable Field Range [Tesla] 10^{-12} 10^{-10} 10^{-8} 10^{-6} 10^{-4} 10^{-2} 10^{0} 10^{2} 10^{4}
Low-Field Sensors	
Squid	
Fiber-Optic	
Optically Pumped	
Nuclear Precession	
Search-Coil	
Earth's Field Sensors	
Anisotropic Resistivity	
Flux Gate	
Bias Field Sensors	
Magnetotransistor	
Magnetodiode	
Magneto-Optical Sensor	
Giant Magnetoresistive	
Hall-Effect Sensor	
Magnetic Field Sources	
Earth's Magnetic Field	
Permanent Magnet	
Electric Current	

Fig. 1.1: Magnetic sensor technologies and their detection capabilities [20]. The sensors are divided in three different groups of field ranges: low field (nT), Earth's field (μT), and bias field (mT).

ing through cesium or helium gas undergoes different absorption depending on the magnetic field strength. The optically pumped magnetometer suffers from a large size and high power consumption. It has a detection range form 10^{-12} to 10^{-4}T [24].

The *nuclear precession* magnetometer exploits the response to a magnetic field of the nuclei of atoms in a hydrocarbon fluid such as benzene. Due to their own angular momentum the protons in the fluid can be temporarily aligned by a magnetic field. Switching off the field for alignment, the protons begin to precess along the ambient magnetic field. The precession frequency depends on the magnitude of the field, which can be in a range of 10^{-11} to 10^{-2} T.

The *search-coil* magnetometer uses Faraday's law of induction. A change in the magnetic flux through a coil induces a current which generates a voltage at its terminals. Typically, the coil is improved by a ferromagnetic core. Depending on the change of magnetic flux, fields as weak as 10^{-12} T can be detected [25].

Earth's Field Sensors

Magnetometers based on *anisotropic resistance* summarize the group of magnetoresistive sensors. An external magnetic field deflects the current in the material causing a change in resistivity. The magnetoresistive effect was first observed in ferromagnetic materials [26, 27]. This effect shows a quadratic dependence on the magnetic field, but can be linearized by the use of barberpole structures [28]. Additionally, these structures show an angular dependence on the magnetic field. The detectable field range is from 10^{-11} to 10^{-2} T [29, 30].

Compass based navigation systems rely on *flux gate* magnetometers. An excitation and a pick-up coil are wrapped around a common high-permeability ferromagnetic core, which oscillates between points of saturation. An external magnetic field disturbs the symmetry in the oscillating signal generating a second harmonic at the pick-up coil. The magnitude of the second harmonic varies linearly with the applied magnetic field, with a detection range from 10^{-10} to 10^{-2} T [31, 32]. Flux gate magnetometers are available in (bulk) macroscopic form and in microfabricated versions with dedicated electronics [33, 34]. Recently, flux gate sensors realized in a commercial CMOS process have been reported [35].

Bias Magnetic Field Sensors

Most industrial applications make use of permanent magnets as a source of the magnetic field [36, 37]. Common bias field strengths are in the order of mT. Possible devices which fit this group of sensors are magnetotransistors, magnetodiodes, magneto-optical sensors, giant magnetoresistive sensors, and Hall devices.

A *magnetotransistor* is a two collector transistor fabricated, e.g., in CMOS technology [38, 39]. An external magnetic induction causes an imbalance in the collector currents due to the Lorentz force. The magnetotransistor can detect magnetic induction down to 10^{-5} T. Recently, even the offset, a major drawback of the device, has been drastically reduced [40, 41].

A *magnetodiode* is essentially a semiconductor diode where its p- and n-regions are separated by a region of intrinsic or low doped silicon. This intrinsic region is bounded by two surfaces with different surface recombination rates. Under high-injection conditions, the Lorentz force leads to a modulation of conductivity in the intrinsic region. In general, magnetodiodes are fabricated in silicon on sapphire technology [42, 43]. However, devices manufactured in CMOS technology with a sensitivity of 25 V/T have also been reported [44].

Magneto-optical sensor exploits the Faraday polarization effect where the direction of polarization of light changes when travelling through certain magnetic materials [45].

Giant-magnetoresistive magnetosensors show a large change of resistance up to 70% depending on the applied magnetic field [46]. Giant magnetoresistive devices consist of a ferromagnetic/non-ferromagnetic multilayer system. The resistance of two thin ferromagnetic layers, separated by a thin non-ferromagnetic conducting layer, can be altered by changing the alignment in the magnetic moments of the ferromagnetic layers from antiparallel to parallel by an external magnetic field. Layers with parallel magnetic moments have a lower likelihood of scattering at the interfaces. They have a longer mean free path, and, therefore, a decrease in resistance. The thickness of a given layer must be smaller than the mean free path of electrons in the layer, which is smaller than 10 nm [47].

In most industrial applications, where the requirements for the field magnitude are not as high, *Hall-effect sensors* can be used instead of giant magnetoresistive devices [48]. Hall sensors are easy in terms of operation, they allow dynamic offset compensation over their life-time, are small, and can be co-integrated with dedicated electronics. They are perfectly suited to detect the magnetic field of a permanent magnet, which is in the range of a few mT, or magnetic fields generated by an electric current in the A-range. Their operation is based on the Lorentz-deflection of carriers which generates a voltage in an orthogonal direction to the current flow. In applications requiring field strength in the range of

mT, the integrated Hall sensor is the best candidate in terms of overall performance.

Integrated magnetic field sensors make use of materials and processes provided for standard silicon IC technology. Such devices exploit all the advantages associated with IC technology, which explains the intensive research effort and their commercial success. In particular, because of IC technology, integrated magnetic field sensors have been boosted to the highest reliability at minimum cost. Excellent reviews on silicon magnetic sensors are given in [18, 48 to 53].

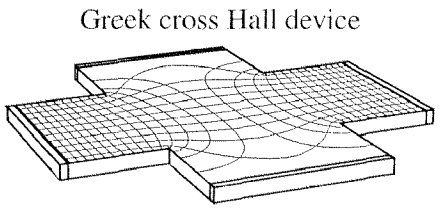
1.3 Scope of Thesis

This thesis aims to contribute to the development of integrated magnetic sensors based on the Hall effect. Although many previous research results on this topic can be found in literature, many aspects associated with the implementation in CMOS technology have been neglected. This work, therefore, emphasizes aspects such as, geometry optimization, CMOS-specific non-idealities and their compensation, and, finally, packaging concepts suited for batch fabrication. Furthermore, work on process technology is presented to realize sensor structures sensitive to magnetic inductions parallel to the chip surface, a problem not solved satisfyingly to date. Such a configuration allows multidimensional field measurements on a single chip and in combination with, e.g. dynamic offset compensation, the performance of Hall devices can be outstanding.

This thesis was embedded into an European ESPRIT project together with other Universities and industrial partners. Therefore, many of the subjects treated in this work were motivated by the issues relevant to commercialization. This work should help application designers to understand the physics of Hall devices and to design a sensor for best performance, particularly for the sample applications discussed.

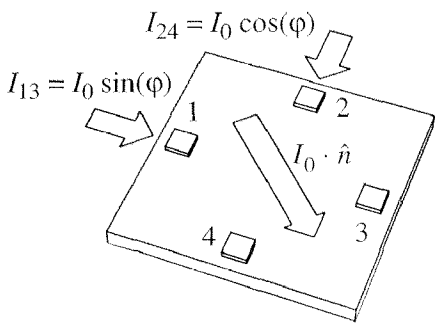
1.4 Major Results

A Numerical Description of the Performance of a Hall Device



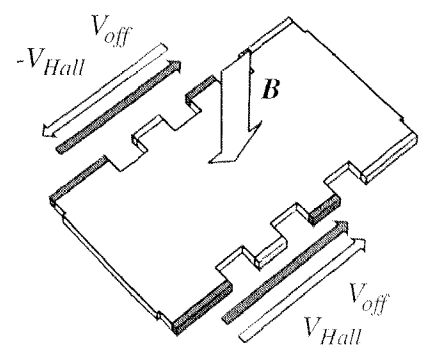
Many aspects have to be considered for an optimized layout of a CMOS Hall device. A numerical model was developed which describes the behavior of a device over a wide operating range independent of its geometry. Furthermore, non-idealities concerning mechanical stress and temperature effects, which highly degrade the device performance, are treated theoretically.

Offset Reduction by the Continuous Spinning Current Method



A major drawback of a Hall device is the high offset voltage, i.e. the output voltage at zero magnetic induction. This offset voltage depends on various physical properties and may change over the device life-time. A method for dynamic offset compensation was developed. A spinning current vector in the Hall plate is generated by superimposing two periodic biasing currents [54, 55]. From the resulting contact voltages, the almost constant Hall voltage can be separated from the periodic offset voltage. Residual offsets are below 10 µT, which corresponds to a fraction of the earth's magnetic field.

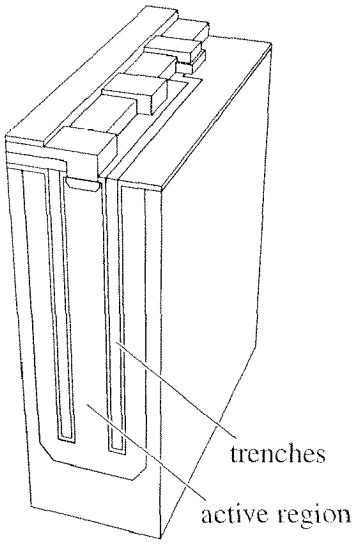
The Double-Hall Sensor



The offset voltage of the double-Hall sensor is compensated by design [56]. The sensor consists of two single Hall devices sharing the same active region. The sensor signal is given by the difference of the output voltages of the single devices. They have almost equal offsets but their magnetic response is of opposite sign due to the structure symmetry. In particular the temperature coefficient of the offset voltages are equal because they originate from the same

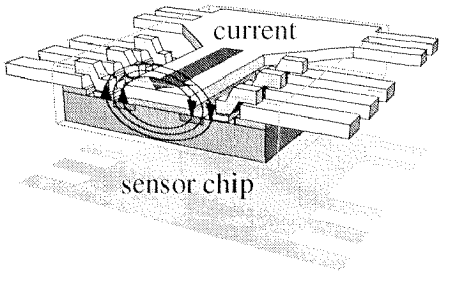
active region. The double-Hall sensor allows the implementation of a simple offset reduction regime resulting in an in-expensive magnetic microsystem.

Vertical Trench-Hall Devices



A novel vertical Hall device sensitive to magnetic induction parallel to the chip surface was developed [57, 58]. The vertically oriented active region of the sensor is defined by two parallel trenches. The performance of the sensor is comparable to the conventional lateral Hall device. The vertical trench-Hall device exhibits an outstanding xy-cross-sensitivity below 0.2% over the full circle. The fabrication technology enables co-integration of sensor and front-end circuitry on the same CMOS chip. Additionally, the sensor bears the potential for dynamic offset compensation by means of the spinning current technique. The trench-Hall device was developed in close collaboration with Austria Mikro Systeme International AG.

Applications: Current Monitor and Wear-Free Angle Measurement



A compact CMOS current monitor system for galvanically insulated current measurement is presented [59]. It is packaged with lead-on-chip technology which is usually used for high volume packaging of memory chips. The recommended fabrication flow allows inexpensive mass production of the sensor chip including packaging. With the presented systems, current measurement in a range of ± 10 A was demonstrated with a non-linearity $< \pm 0.3\%$. A further application shows a wear-free angle measurement system [57]. Combining the vertical trench-Hall device with a permanent magnet, a rotary switch with a 0.2° resolution is realized. System electronics can be co-integrated with two orthogonally arranged sensors on the same chip. Such a system meets, e.g., the harsh requirements of the automotive industry.

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2 PHYSICS OF INTEGRATED CMOS HALL DEVICES

In designing Hall sensors many theoretical aspects have to be considered. There is an abundance of important literature available that covers this large field. An introduction to general semiconductor physics is, e.g., given in [1 to 4], and details of semiconductor devices are treated in [5, 6]. Particular topics on Hall devices can be found in [7 to 12]. This chapter will focus on selected aspects relevant to the implementation of CMOS Hall devices.

The necessary basic knowledge of the Hall effect [13] is given in the following section on galvanomagnetic effects, which also introduces the notation used throughout this thesis. In an approximate analysis, the Hall voltage is presented and the important property of the Hall angle is defined. In an advanced analysis of galvanomagnetic effects, the role of collision or scattering of the charge carriers is treated.

Next, input resistance and sensitivity of a Hall device are discussed. Starting from the fundamental semiconductor equations [1, 6, 14], correction factors describing the deviation from an ideal Hall plate geometry are determined by means of conformal mapping [14, 15]. Additionally, device geometry is modified by the junction field effect [16, 17]. The use of classic Shockley theory for the junction field effect [16] predicts only poor results. Therefore, the junction field effect is revisited using the real doping profiles of a CMOS process. This results in an equivalent circuit of the Hall device that predicts the input resistance, the common-mode voltage, and the sensitivity. Furthermore, the above properties are treated in terms of their thermal behavior.

The offset voltage, which can be considered as the major drawback of a Hall device, is covered in the next two sections. Two novel offset reduction schemes based on the use of a continuous spinning current method [18] and a double Hall sensor [19] are introduced. Besides the basic considerations, all physical effects important for the continuous spinning current method are given. These include:

geometrical errors, mechanical stress issues, and non-linearities arising from the junction field effect. The offset reduction by use of a double-Hall sensor is treated in a more generic sense, whereby only the basic concepts are given. Due to the complexity, the proof of feasibility will be summarized by experimental results in chapter 3.

2.1 Galvanomagnetic Effects

Approximate Analysis of the Hall Effect and Magnetoresistance

The Hall effect is a manifestation of the Lorentz force acting on mobile charge carriers in condensed matter [13]. For an approximate analysis, electrons with a particle charge of $-q$ experience in the presence of an electromagnetic field a force given by

$$\boldsymbol{F}_L = -q\boldsymbol{E} - q[\boldsymbol{v} \times \boldsymbol{B}]. \tag{2.1}$$

Here, $\boldsymbol{E}$ denotes the electrical field, $\boldsymbol{v}$ the charge velocity, and $\boldsymbol{B}$ the applied magnetic induction. For a simplified analysis, we consider a long sample of n-type silicon with $l \gg w$ (see Fig. 2.1). An applied electrical field $\boldsymbol{E}_a = (E_a, 0, 0)$ causes a drift velocity of the electrons of $\boldsymbol{v}_n = (-\mu_n \boldsymbol{E}_a, 0, 0)$ where μ_n is the electron mobility. The associated current density $\boldsymbol{J}_n$ of the majority carriers in the absence of an applied magnetic field, is given by $\boldsymbol{J}_n = (q\mu_n n\boldsymbol{E}_a, 0, 0)$ where n is the majority carrier density in the n-type silicon. However, an applied magnetic induction $\boldsymbol{B} = (0, B, 0)$ forces the charged carriers towards one edge of the sample. The carrier concentration at this boundary of the sample generates a Hall electric field $\boldsymbol{E}_H = (0, 0, E_H)$ with a Hall force $\boldsymbol{F}_H$ balancing the Lorentz force $\boldsymbol{F}_L$. In a state of equilibrium the Hall electric field is given by

$$\boldsymbol{E}_H = \frac{\boldsymbol{F}_H}{q} = \frac{\boldsymbol{F}_L}{q} = \mu_n[\boldsymbol{E}_a \times \boldsymbol{B}]. \tag{2.2}$$

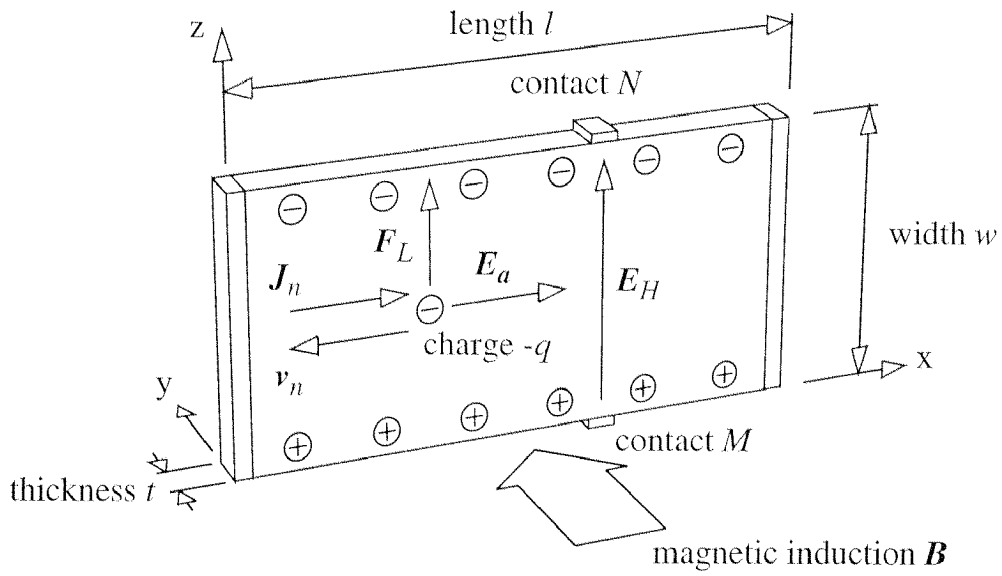


Fig. 2.1: The Hall effect in a long sample of n-type silicon. $\boldsymbol{E}_a$ denotes the applied magnetic field, $\boldsymbol{B}$ the magnetic induction, $\boldsymbol{v}_n$ the drift velocity of the electrons, $\boldsymbol{F}_L$ the magnetic force, $\boldsymbol{J}_n$ the current density, and $\boldsymbol{E}_H$ the Hall electric field.

With reference to Fig. 2.1, placing two contacts, M and N, at the opposite sides of the silicon sample allows a measurement of the corresponding Hall voltage V_H. Under the condition that the contacts are on the same equipotential line in the absence of a magnetic field (i.e. under zero offset conditions), the corresponding Hall voltage can be calculated as

$$V_H = \int_M^N \boldsymbol{E}_H \cdot ds \tag{2.3}$$

where the integral is taken along a path s connecting the contacts M and N. In terms of Eqs. (2.2, 2.3) the Hall voltage can be expressed as

$$V_H = \frac{R_H}{t} IB. \tag{2.4}$$

Here t is the thickness of the sample, the Hall coefficient $R_H = -1/qn$, the current $I = |\boldsymbol{J}_n| wt$, and the magnetic induction B is perpendicular to the sample surface. The corresponding input resistance R of the sample is calculated as

$$R = \frac{1}{qn\mu_n}\frac{1}{t}\frac{l}{w}. \tag{2.5}$$

The above considerations yield only a phenomenological description of the Hall effect. For a more detailed analysis the influence of the crystal lattice has to be considered. Therefore, the analysis can be improved by taking into account the transport of carriers under the influence of collisions with the crystal lattice.

A charged particle, exposed to orthogonal electric and magnetic fields, moves along a cycloid in vacuum [20] (see Fig. 2.2). In contrast, a charge carrier in a solid with the effective mass m^* [12] moves for only a portion of a cycloid and loses, after a relaxation time τ, all its kinetic energy due to collisions. The charge starts a new cycloid path in the direction of the electric field (see Fig. 2.2). Therefore, the mean deflection angle Θ_H correlates to the relaxation time τ and is expressed by

$$\tan\Theta_H = -\omega_c\tau = \frac{-qB}{m^*}\tau = -\mu_n B, \tag{2.6}$$

where ω_c is the cyclotron frequency [20]. However, the magnitude of the Hall electric field of Eq. (2.2) can also be represented by the Hall angle Θ_H

$$\tan\Theta_H = |\boldsymbol{E}_H|/|\boldsymbol{E}_a|. \tag{2.7}$$

Therefore, collisions in the presence of an applied magnetic induction causes the resulting electric field $\boldsymbol{E} = \boldsymbol{E}_a + \boldsymbol{E}_H$ to be non-co-linear with respect to an applied electric field $\boldsymbol{E}_a$ or the current density $\boldsymbol{J}_n$.

The presence of the Hall angle Θ_H between the current density $\boldsymbol{J}_n$ and the resulting electric field $\boldsymbol{E}$ causes an increase in the transit path for a charge moving through a sample. As a result, the resistivity of the sample increases. This effect is called the geometric magnetoresistance effect in semiconductors [12].

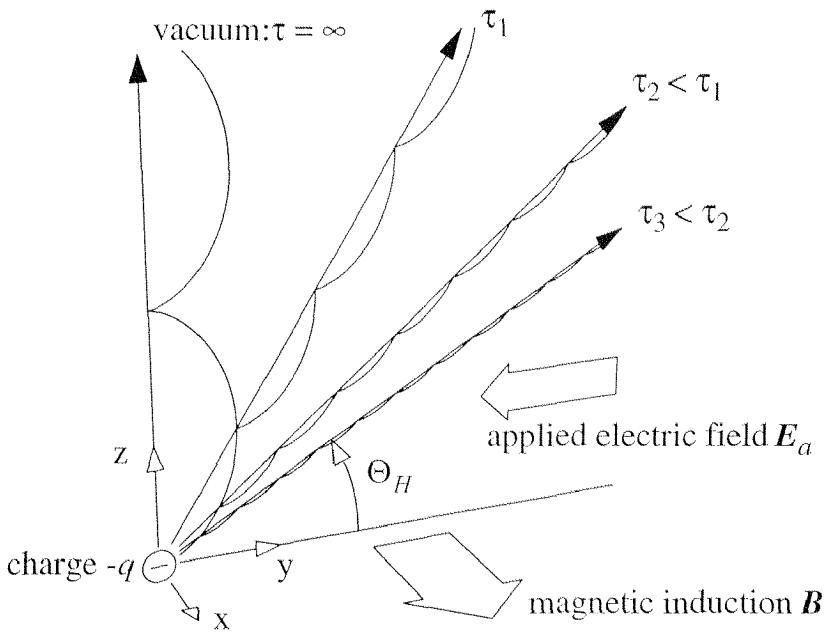


Fig. 2.2: Schematic representation of the path of electrons in vacuum and in a solid in the presence of a magnetic induction and an applied electric field. After a relaxation time τ, the electron loses all its kinetic energy due to collision and starts a new cycloid path in the direction of the applied electric field.

Furthermore, a physical magnetoresistance effect occurs in the semiconductor material [12]. This effect is related to collision factors and depends on the magnetic induction.

For a better physical understanding of the interaction of electrons with the crystal lattice, an approach based on the Boltzmann transport equation must be employed as shown in the next section.

Advanced Analysis of Galvanomagnetic Effects

An accurate analysis of the galvanomagnetic effects can be carried out by solving the Boltzmann transport equation using the relaxation-time approximation [3]. Here, we only present the key-results of such an analysis. With a uniform temperature distribution in a homogeneous semiconductor material and electrons as majority carriers, the current density is determined as

$$\boldsymbol{J}_n = q^2 K_1 \boldsymbol{E} + \frac{q^3}{m^*} K_2 [\boldsymbol{E} \times \boldsymbol{B}] + \frac{q^4}{m^{*2}} K_3 \boldsymbol{B} (\boldsymbol{E} \cdot \boldsymbol{B}). \tag{2.8}$$

Here, the magnetic field dependent transport coefficients K_1, K_2, and K_3 are energy weighted averages over the term $\tau^s/(1+\mu_n{}^2 B^2)$ $(s = 1, 2, 3)$ with the energy dependent relaxation time τ and the electron mobility $\mu_n = q\tau/m^*$ [22],

$$K_s = \frac{n}{m^*} \left\langle \frac{\tau^s}{1+\mu_n{}^2 B^2} \right\rangle, \text{ with } s = 1 \ldots 3. \tag{2.9}$$

Here, n denotes the electron carrier density and m^* the electron effective mass. For an orthogonal arrangement of the magnetic induction $\boldsymbol{B}$ and the electric field $\boldsymbol{E}$ (i.e. $\boldsymbol{B} \perp \boldsymbol{E}$), Eq. (2.8) reduces to

$$\boldsymbol{J}_n = \sigma_{Bn}(B)\boldsymbol{E} + \sigma_{Bn}(B)\mu_{Hn}(B)[\boldsymbol{E} \times \boldsymbol{B}], \tag{2.10}$$

where the effective conductivity of electrons $\sigma_{Bn}(B)$ and associated Hall mobility $\mu_{Hn}(\boldsymbol{B})$ are introduced [12] with

$$\sigma_{Bn}(B) = q^2 K_1, \tag{2.11}$$

and

$$\mu_{Hn}(\boldsymbol{B}) = \frac{q}{m^*} \frac{K_2}{K_1}. \tag{2.12}$$

For low magnetic induction defined by $\mu_n{}^2 B^2 \ll 1$, the kinetic transport coefficients of Eq. (2.9) can be approximated [12] by

$$K_1 \cong \frac{n}{q} (\langle \mu_n \rangle - \langle \mu_n{}^3 \rangle B^2), \tag{2.13}$$

$$K_2 \cong \frac{nm^*}{q^2} (\langle \mu_n{}^2 \rangle - \langle \mu_n{}^4 \rangle B^2). \tag{2.14}$$

By using Eqs. (2.13, 2.14), the effective conductivity of electrons $\sigma_{Bn}(\boldsymbol{B})$, Eq. (2.11), reduces, for a non-degenerated semiconductor material [12], to

$$\sigma_{Bn}(\boldsymbol{B}) \cong \sigma_0(1-\alpha\mu_{Hn}^2 B^2) \ , \quad \text{with} \quad \alpha = \frac{r_3}{r_2^2}, \tag{2.15}$$

were $\sigma_0 = q\mu_n n$ and r_i are the scattering factors (see Tab. 2.1). Analogously, the Hall mobility $\mu_{Hn}(\boldsymbol{B})$ for electrons, Eq. (2.12), can be expressed as

$$\mu_{Hn}(\boldsymbol{B}) = \mu_{H0n}(1-\beta\mu_n^2 B^2), \quad \text{with} \quad \beta = \frac{r_4}{r_2} - r_3, \tag{2.16}$$

where μ_{H0n} is the Hall mobility at zero magnetic induction, and is defined as

$$\mu_{H0n} = \mu_{Hn}(\boldsymbol{B}=0) = \frac{q}{m^*}\frac{\langle\tau^2\rangle}{\langle\tau\rangle^2} = \mu_n r_2 . \tag{2.17}$$

The scattering factors $r_m = \langle\tau^m\rangle/\langle\tau\rangle^m$ for semiconductors with spherical constant energy surfaces [2] are given in Tab. 2.1.

Scattering factor	*Acoustic phonon*	*Ionized impurities*
r_2	1.18	1.93
r_3	1.77	5.90
r_4	4.16	19.14

Tab. 2.1: Calculated scattering factors for different scattering mechanisms [2].

The Hall coefficient R_{Hn}, which determines the efficiency of the material to generate a Hall voltage, is given by [12]

$$R_{Hn} = R_{H0}(1-\gamma\mu_{Hn}^2 B^2) \quad \text{with} \quad \gamma = 1 - 2\frac{r_3}{r_2^2} + \frac{r_4}{r_2^3} \tag{2.18}$$

where R_{H0} is the Hall coefficient at zero magnetic induction and is defined as

$$R_H(\boldsymbol{B}=0) = R_{H0} = -\frac{r_2}{qn}. \tag{2.19}$$

In the above analysis, we have assumed a semiconductor with a spherical energy surface for which the effective mass is constant (isotropic). But the conduction band of silicon is non-spherical and multivalleyed resulting in an anisotropic effective mass. A correction in the scattering factors ($r_m = \langle\tau^m\rangle/\langle\tau\rangle^m$) due to anisotropic mobility needs to be introduced [12].

In addition to the Hall and magnetoresistance effects, other galvanomagnetic effects may occur in a semiconductor associated with the transport of charge carriers. They include the Ettinghausen-, Nernst- and Righi-Leduc-effects. These effects may interfere with the Hall field [1].

2.2 Input Resistance and Sensitivity

The geometrical correction factors G_R and G_S

In the study of the galvanomagnetic effects, we assumed an ideal Hall plate of infinite length and point sense contacts. However, due to design constraints, a physical Hall plate requires a correction for the magnetic sensitivity and the resistance to account for shape effects of the plate.

The sensitivity of a Hall plate S_a of arbitrary shape can be expressed as

$$S_a = G_S S_{a\infty} \quad \text{with} \quad S_{a\infty} = \frac{V_H(I)}{B} = \frac{R_{Hn} I}{t}, \tag{2.20}$$

where G_S is the geometrical correction factor for the sensitivity and $S_{a\infty}$ the sensitivity of a Hall plate of infinite length [21]. Furthermore, the input resistance of the Hall plate has to be considered to determine the operating point. Here, the geometrical correction factor G_R describes the correlation between a square ohmic plate described by its sheet resistance $R_\square$, and the physical Hall plate with resistance R,

$$R = G_R R_\square \quad \text{with} \quad R_\square = \frac{1}{\sigma_{Bn}} \frac{1}{t}. \tag{2.21}$$

In order to calculate the geometrical correction factors G_S and G_R, the basic equations for an n-type semiconductor in the presence of a magnetic induction $\boldsymbol{B}$ must be solved [14, 22]:

$$\begin{aligned}(\partial n/\partial t) + q^{-1}\nabla\bullet\boldsymbol{J}_n &= U\\ (\partial p/\partial t) + q^{-1}\nabla\bullet\boldsymbol{J}_p &= -U,\end{aligned} \tag{2.22}$$

$$\boldsymbol{J}_n = \sigma_{Bn}\boldsymbol{E} + qD_n\nabla n - \sigma_{Bn}\mu_{Hn}[\boldsymbol{E}\times\boldsymbol{B}] - \mu_{Hn}qD_n[\nabla n\times\boldsymbol{B}], \tag{2.23}$$

$$\nabla\bullet\boldsymbol{E} = -\nabla^2\phi = (q/(\varepsilon_0\varepsilon))(p - n + N_D - N_A). \tag{2.24}$$

Here, n denotes the electron concentration, p the hole concentration, $\boldsymbol{J}_n$ the electron current density, $\boldsymbol{J}_p$ the hole current density, N_D the donor concentration, N_A the acceptor concentration, $\boldsymbol{E}$ the electric field, ϕ the electric potential, μ_{Hn} the electron Hall mobility, σ_n the electron conductivity, D_n the diffusion coefficient, ε the dielectric constant, ε_0 the permittivity in vacuum, and U the net recombination rate. For a Hall plate, several assumptions can be made to simplify the analysis in the above equations.

Considering steady state operation, the divergence of the majority carrier current in the Hall plate with net recombination $U = 0$ reduces Eq. (2.22) to

$$\nabla\bullet\boldsymbol{J}_n = \nabla\bullet\boldsymbol{J}_p = 0. \tag{2.25}$$

Furthermore, with the assumption of a homogeneously doped n-type material there are no space charge effects and with $n = N_D$ and $p \ll n$, Poisson's equation (2.24) reduces to the simpler Laplace equation

$$-\nabla\bullet\boldsymbol{E} = -\nabla^2\phi = 0. \tag{2.26}$$

Similarly, Eq. (2.23) reduces to

$$\boldsymbol{J}_n = \sigma_{Bn}\boldsymbol{E} - \sigma_{Bn}\mu_{Hn}[\boldsymbol{E}\times\boldsymbol{B}]. \tag{2.27}$$

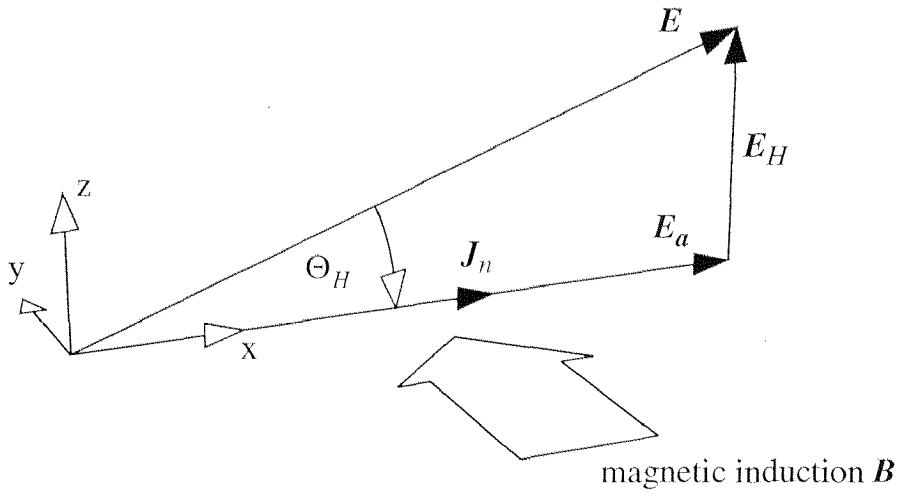


Fig. 2.3: Vector diagram illustrating the electric fields $\boldsymbol{E}_a$ and $\boldsymbol{E}_H$, the current density $\boldsymbol{J}_n$, and the corresponding Hall angle Θ_H in the presence of a magnetic induction $\boldsymbol{B}$.

Assuming $\boldsymbol{B} \perp \boldsymbol{E}$, the resulting electric field $\boldsymbol{E} = \boldsymbol{E}_a + \boldsymbol{E}_H$ consists of an applied electric field $\boldsymbol{E}_a$ and the Hall field $\boldsymbol{E}_H$, Eq. (2.27). This implies a rotation of the electric field by the Hall angle $\Theta_H = -\arctan(E_H/E_a)$ with respect to the current density $\boldsymbol{J}_n$ (see Fig. 2.3). One can show with Eqs. (2.25, 2.27) and the Maxwell equation $\nabla \times \boldsymbol{E} = 0$, that under a uniform σ_{Bn} over the active Hall plate region,

$$\begin{aligned} \nabla \bullet \boldsymbol{J}_n &= \sigma_{Bn} \nabla \bullet \boldsymbol{E} - \sigma_{Bn} \mu_{Hn} \nabla \bullet [\boldsymbol{E} \times \boldsymbol{B}] \\ &= \sigma_{Bn} \nabla \bullet \boldsymbol{E} - \sigma_{Bn} \mu_{Hn} [\nabla \times \boldsymbol{E}] \bullet \boldsymbol{B} \\ &= \sigma_{Bn} \nabla \bullet \boldsymbol{E} = 0. \end{aligned} \tag{2.28}$$

Consequently, the Laplace equation is satisfied.

Finally, the boundary conditions for above potential field problem in the presence of an applied magnetic field have to be defined. In general, for a Hall plate two types of boundaries can be identified: contact boundaries (*cb*) for ohmic contacts, and insulating boundaries (*ib*) for the insulating edge of the Hall plate [14]. Defining three mutually orthogonal unit vectors: $\boldsymbol{u}_t$ tangential to the boundary, $\boldsymbol{u}_n$ normal to the boundary, and $\boldsymbol{u}_B$ parallel to the applied magnetic induction $\boldsymbol{B}$, the boundary conditions can be written in the following compact form [14]

$$\boldsymbol{E} \bullet \boldsymbol{u}_t\big|_{(cb)} = 0, \text{ and } \quad \boldsymbol{J}_n \bullet \boldsymbol{u}_t\big|_{(cb)} = -\mu_{Hn} B(\boldsymbol{J}_n \bullet \boldsymbol{u}_n), \tag{2.29}$$

$$\boldsymbol{J}_n \bullet \boldsymbol{u}_n\big|_{(ib)} = 0, \text{ and } \quad \boldsymbol{E} \bullet \boldsymbol{u}_n\big|_{(ib)} = -\mu_{Hn} B(\boldsymbol{E} \bullet \boldsymbol{u}_t). \tag{2.30}$$

A useful method to solve Laplace's equation (2.26) is by the conformal mapping technique [15]. Here, one starts with a geometry whose solution can be determined by inspection. For example, a Hall plate parallelogram tilted by the Hall angle $\tan\theta_H = -\mu_n|\boldsymbol{B}|$, as shown in Fig. 2.4, satisfies Eq. (2.26) and the boundary conditions described in Eqs. (2.29, 2.30) [14]. Once Laplace's equation is solved for that geometry the geometrical correction factors G_S and G_R can be easily determined [14]. Next, any arbitrary geometrical shape which can be mapped conformally to the parallelogram has geometrical correction factors modified by the same conformal transformation function.

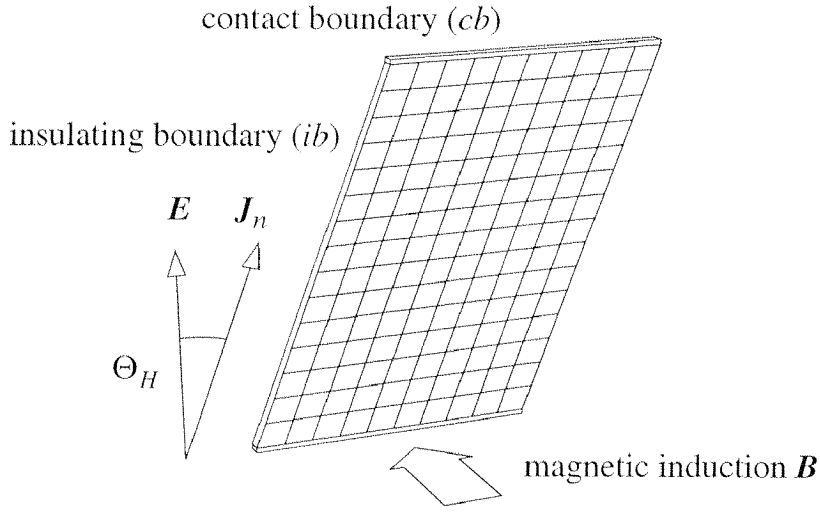


Fig. 2.4: Electric field and current lines in a Hall plate having the shape of a parallelogram. The geometry satisfies the Laplace equation and its boundary conditions.

In reality, the conformal transformation function for an arbitrary geometrical shape is, for most cases, difficult to find and hard to evaluate. Therefore, we start with a symmetrical circular Hall plate or an asymmetrical rectangular Hall plate (see Fig. 2.5). For these chosen shapes, the geometric correction factors G_S and G_R are known [23, 24]. Using a bilinear transformation or the Schwartz-Christoffel transformation, these two shapes can be mapped to the upper complex

half-plane [15]. Now, mapping the complex half plane to an arbitrary geometrical shape requires only the conformal transformation function, which are solutions that well known [15].

An overview of Hall plate shapes, with the corresponding geometric correction factors is shown in Tab. 2.2 [21, 23 to 30].

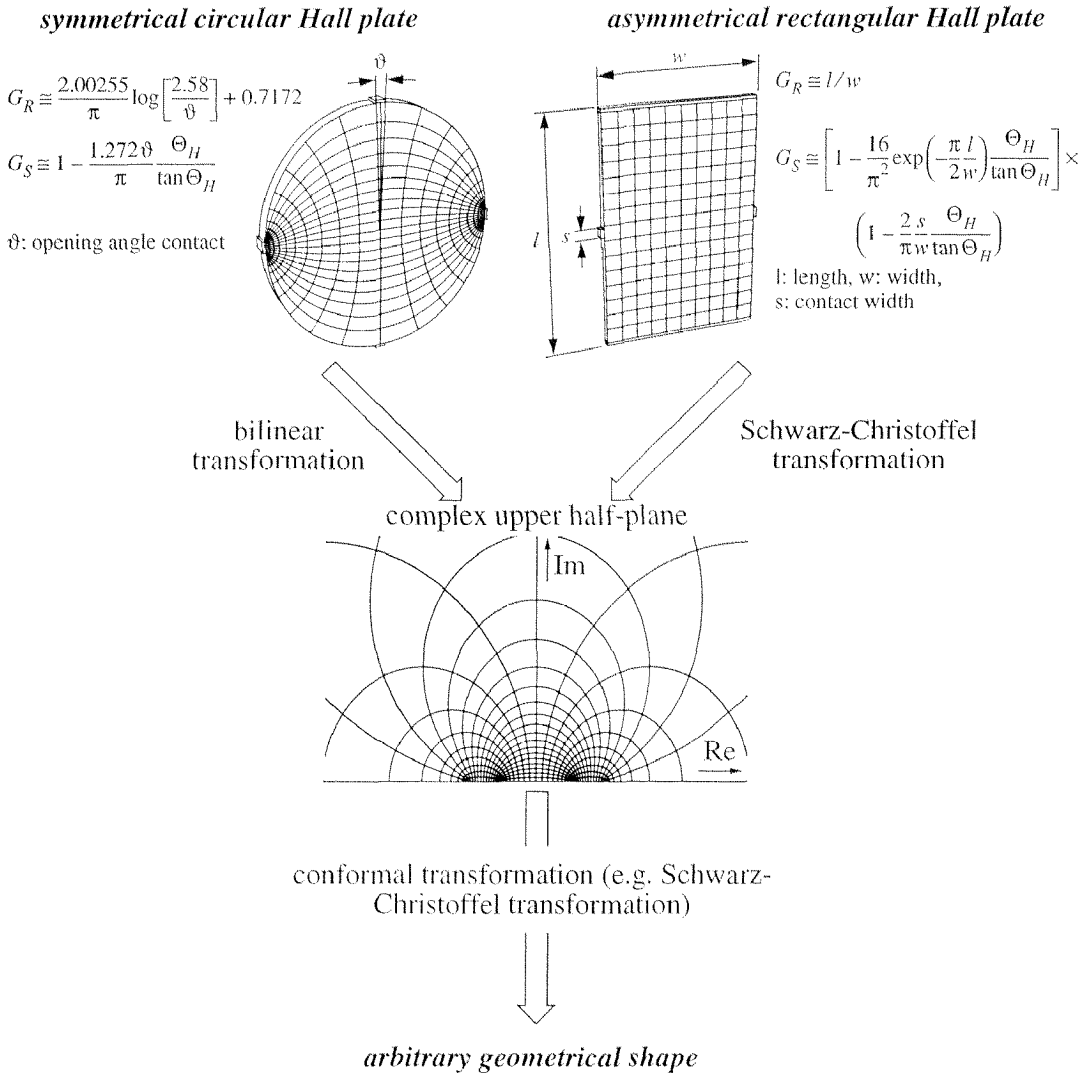
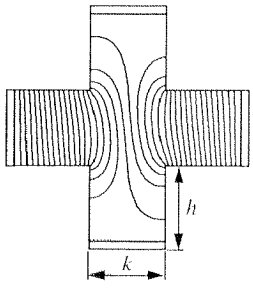
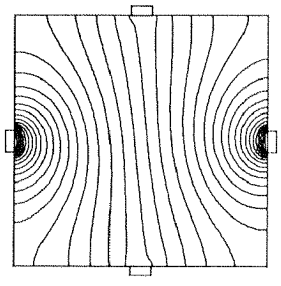
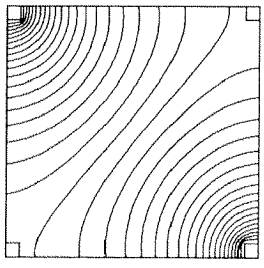


Fig. 2.5: Determination of G_S and G_R of Hall plates with arbitrary shape. The correction factors of a circular and a rectangular Hall plate are known [23, 24]. By means of conformal mapping using a bilinear or a Schwarz-Christoffel transformation, the correction factors can be calculated for any shape.

Geometrical shape	*Geometrical correction factor*	*Ref.*
Greek Cross  h: length side arm k: width side arm	$m = \frac{\tan[0.645\exp(-\pi h/k)]}{\tan[\pi/2-0.645\exp(-\pi h/k)]}$ $G_R = \frac{K(1-m^2)}{2K(m^2)} \cong 2.00\frac{h}{k} + 0.72$ $K(m^2)$: complete elliptic integral	[14, 23]
	$G_S = 1 - 1.045\exp(-\pi h/k)\frac{\Theta_H}{\tan\Theta_H}$	[25]
Square (Version A)  c: length contact b: circumferences active region	$m = \frac{\mathrm{sn}(K(m_c^2)c/b, m_c^2)}{\mathrm{sn}(K(m_c^2)(c/b+2i), m_c^2)}; m_c = 0.1716$ $G_R = \frac{K(1-m^2)}{2K(m^2)}$ $\cong 0.94 + 1.54\exp\left(\frac{-3.75c}{b}\right) + 0.018\frac{b}{c}$ sn(u,v): Jacobian integral function	[15, 23]
	$G_S = 1 - 1.062\frac{c}{b}\frac{\Theta_H}{\tan\Theta_H}$	[25]
Square (Version B) 	G_R and G_S have the same form as for the *Greek cross*, but with $\frac{h}{k} = -\frac{1}{\pi}\log\left[\frac{7.427\left(\frac{c}{b-2c}\right)^2}{\left(1+\frac{2c}{b-2c}\right)^2}\right]$,	[15]

Tab. 2.2: Calculated geometrical correction factors of symmetrical, lateral Hall devices. Geometrical shapes not published in prior literature are calculated according the method described in Fig. 2.5.

The Junction Field Effect

The sensitivity S_a and the input resistance R of a Hall plate depend on its geometrical dimensions according to Eqs. (2.20) and (2.21). Additionally, for a CMOS Hall device with an active region consisting of an n-doped region in a p-type substrate, the boundary of the Hall plate is limited by an insulating pn-junction. Since the thickness of the pn-junction is controlled by the applied electric field, the device geometry changes with changing biasing conditions.

We consider the case of an ideal lateral Hall device fabricated in CMOS technology with point sense contacts (see Fig. 2.6) [31]. The active region consists of a transistor n-well which is optionally covered by a p^+-layer. For such an arrange-

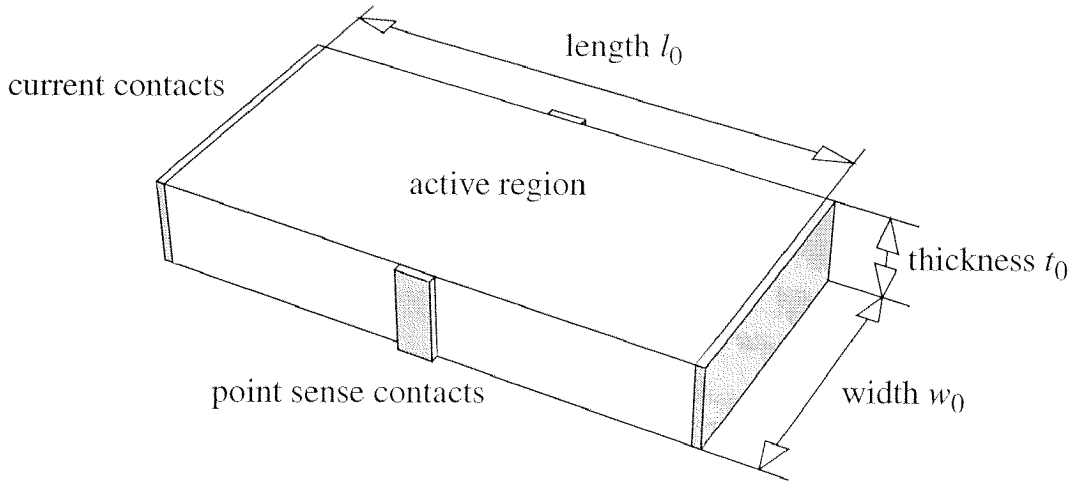


Fig. 2.6: Ideal lateral Hall device with point sense contacts. The geometry is defined by the length l_0, the width w_0, and the depth of the metallurgical junction of the transistor n-well denoted as thickness t_0. The device is covered by an optional p^+-layer.

ment, the effects of the junction field effect modify mainly the thickness t_0 of the n-well. However, the use of the conventional theory of a JFET [32] to describe the junction field effects predicts poor results since the theory is based on abrupt doping profiles for the active region. Lateral Hall devices realized in CMOS technology suggest a Gaussian function to describe the doping profile, and, consequently, require an improved JFET model.

The doping profile of a transistor n-well with an optional p^+-cover is simulated with finite element modeling. In accordance with the theory of ion implantation [33], the doping profile $n(x)$ of the donor concentration N_D can be approximated with a Gaussian function

$$n(x) = \frac{\Phi}{\sqrt{2\pi} \cdot \Delta R_p} \cdot \exp\left[-\left(\frac{x - R_p}{\sqrt{2} \cdot \Delta R_p}\right)^2\right] \cong N_D(x) \,, \tag{2.31}$$

where x is the doping depth, Φ the number of ions per unit area, R_p the projected range, and ΔR_p the projected straggle. With additional information from sheet resistance and SIMS measurements of the particular CMOS process (CXE process, Austria Mikro Systeme Int. AG), the doping distribution can be determined (see Fig. 2.7).

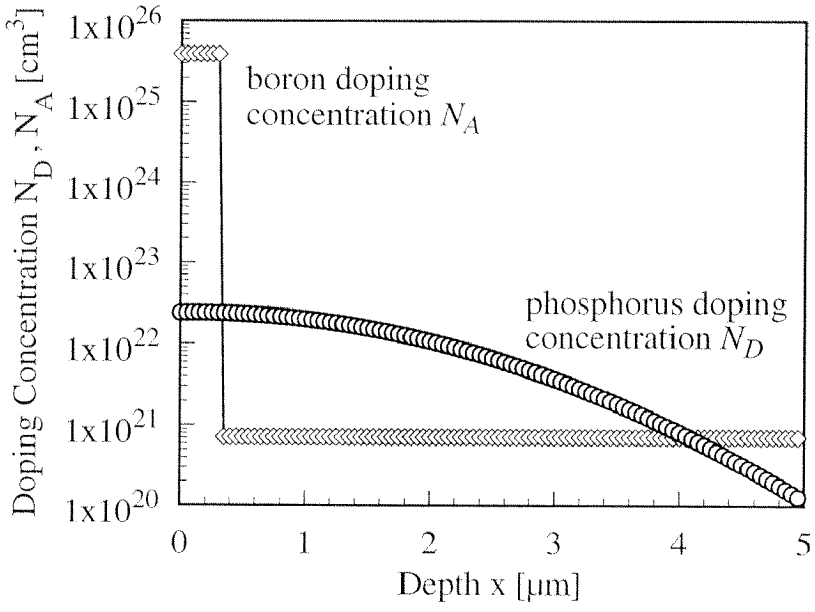


Fig. 2.7: Sample of a doping profile of an n-well with p^+-cover for a particular CMOS process.

With a similar approach, the doping profile $p(x)$ of the acceptor concentration N_A for the p^+ layer can be obtained. This results in an abrupt profile of the form

$$p(x) \cong N_A(x) \cong \begin{cases} p_p & x < t_p \\ p_0 & x > t_p \end{cases} \,, \tag{2.32}$$

where p_p is the peak doping concentration, t_p the depth of the profile, and p_0 the background doping concentration of the p-type substrate (see Fig. 2.7).

According to Eq. (2.21) the input resistance R of the Hall device depends on the thickness t of the active region, and so does the sensitivity S_a, as shown in Eq. (2.20). The actual thickness is the depth of the active region limited by the voltage dependent depletion layer of the isolating pn-junction to the substrate. In case of a shallow p^+-cover, the corresponding depletion layer limits the device thickness at the interface between the p^+- and n-well regions.

In order to calculate the voltage dependent depletion layer thickness $x_n(V)$ within the n-doped active region, the following set of equations need to be solved. By integrating Poisson's equation, the condition of charge conservation within the depletion layer is obtained

$$\int_{t_0}^{t_0+x_n(V)} N(x)dx = \int_{t_0-x_p(V)}^{t_0} P(x)dx \,. \tag{2.33}$$

Here, $x_p(V)$ is the junction thickness in the p-region, $N(x) = n(x)$ and $P(x) = p(x)$ the net doping concentrations in the n- and p-region, respectively, and t_0 the location of the metallurgical junction according to Fig. (2.7). Integrating Eq. (2.33) again results in the potential distribution over the depletion layer

$$V + V_{bi} = \frac{q}{\varepsilon_s} \int_{t_0-x_p(V)}^{t_0} d\xi \int_{\xi}^{t_0} P(x)dx + \frac{q}{\varepsilon_s} \int_{t_0}^{t_0+x_n(V)} d\xi \int_{t_0}^{\xi} N(x)dx \,, \tag{2.34}$$

where $\varepsilon_s = \varepsilon_0 \cdot \varepsilon_{Si}$ is the permittivity constant ε_0 times the relative dielectric constant of silicon ε_{Si}, and V_{bi} the built-in potential. Finally, the condition of zero net electron and hole currents across the depletion layer requires a constant Fermi level throughout the junction resulting in

$$V_{bi} = \frac{kT}{q} \ln\left[\frac{N(t_0+x_{n0}) \times P(t_0-x_{p0})}{n_i^2}\right], \tag{2.35}$$

where $x_{n0} = x_n(V = 0)$ and $x_{p0} = x_p(V = 0)$ denote the initial junction thicknesses in the absence of any biasing currents and n_i the intrinsic carrier distribution (see Fig. 2.8). The above relations can be improved by a correction factor $-2kT/q$ for the built-in voltage stemming from the intrinsic carrier distribution in addition to the impurity concentration [34].

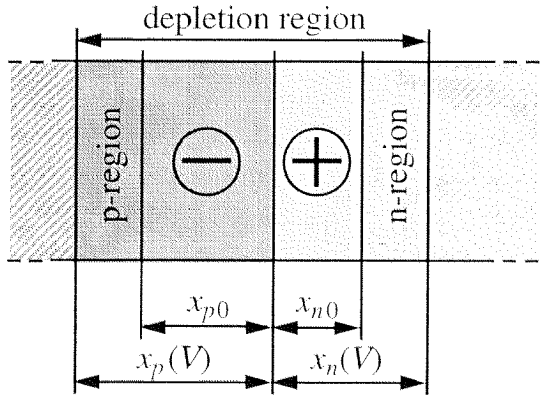


Fig. 2.8: Overview of different junction thicknesses.

In the case of a junction formed by the Gaussian doping profile, Eq. (2.31), and a constant background doping p_0, Eqs. (2.33, 2.34, 2.35) are correspondingly modified to read as

$$\left(-\frac{\phi}{2}\right)\mathrm{Erf}\left[\frac{x_n V + R_p - t_0}{\sqrt{2}\Delta R_p}\right] + p_0 x_n(V) = \frac{\phi}{2}\mathrm{Erf}\left[\frac{x_p V - R_p + t_0}{\sqrt{2}\Delta R_p}\right] + p_0 x_p(V)\,, \quad (2.36)$$

$$V + V_{bi} = \frac{q}{\varepsilon_s}\left(\frac{p_0}{2}(x_p(V)^2 - x_n(V)^2) - \right.$$

$$\frac{\phi(R_p - t_0)}{2}\left(\mathrm{Erf}\left[\frac{x_n(V) + R_p - t_0}{\sqrt{2}\Delta R_p}\right] + \mathrm{Erf}\left[\frac{x_p(V) - R_p + t_0}{\sqrt{2}\Delta R_p}\right]\right) +$$

$$\left.\frac{\phi\Delta R_p}{\sqrt{2\pi}}\left(-\mathrm{Exp}\left[-\frac{(x_n(V) + R_p - t_0)^2}{2\Delta R_p^2}\right] + \mathrm{Exp}\left[-\frac{(x_p(V) - R_p + t_0)^2}{2\Delta R_p^2}\right]\right)\right), \quad (2.37)$$

$$V_{bi} = \frac{kT}{q}\mathrm{Log}\left[\frac{1}{n_i^2}\left(\frac{\phi}{\Delta R_p\sqrt{2\pi}}\mathrm{Exp}\left[-\frac{(x_{n0}+R_p-t_0)^2}{2\Delta R_p^2}\right]-p_0\right)\right.$$
$$\left.\left(p_0-\frac{\phi}{\Delta R_p\sqrt{2\pi}}\mathrm{Exp}\left[-\frac{(x_{p0}-R_p+t_0)^2}{2\Delta R_p^2}\right]\right)\right], \tag{2.38}$$

$$0 \equiv p_0 - \frac{\phi\Delta R_p}{\sqrt{2\pi}}\mathrm{Exp}\left[-\frac{(R_p-t_0)^2}{2\Delta R_p^2}\right], \tag{2.39}$$

where Eq. (2.39) describes the condition for the metallurgical junction. However, with the Gaussian doping profile, Eq. (2.31), only numerical solutions to Eqs. (2.36 to 2.39) can be found for x_n and V_{bi}. On the other hand, in the case of an optional p^+-layer, the doping profile within the p^+-region is well approximated by an abrupt doping profile. Thus Eqs. (2.33 to 2.35) become

$$\frac{\phi}{2}\mathrm{Erf}\left[\frac{x_n V - R_p + t_0}{\sqrt{2}\Delta R_p}\right] - p_0 x_n(V) = \frac{\phi}{2}\mathrm{Erf}\left[\frac{t_p - R_p}{\sqrt{2}\Delta R_p}\right] + p_p x_p(V), \tag{2.40}$$

$$V + V_{bi} = \frac{q}{\varepsilon_s}\frac{p_p x_p(V)^2}{2} + \frac{q}{\varepsilon_s}\left(-\frac{p_0 x_n(V)^2}{2} + \right.$$
$$\frac{\phi}{2}\mathrm{Erf}\left[\frac{t_p-R_p}{\sqrt{2}\Delta R_p}\right](R_p-t_p) - \frac{\phi}{2}\mathrm{Erf}\left[\frac{x_n(V)-R_p+t_0}{\sqrt{2}\Delta R_p}\right](R_p-t_0) -$$
$$\left.\frac{\phi\Delta R_p}{\sqrt{2\pi}}\mathrm{Exp}\left[-\frac{(t_p-R_p)^2}{2\Delta R_p^2}\right] + \frac{\phi\Delta R_p}{\sqrt{2\pi}}\mathrm{Exp}\left[-\frac{(x_n(V)-R_p+t_0)^2}{2\Delta R_p^2}\right]\right), \tag{2.41}$$

$$V_{bi} = \frac{kT}{q}\mathrm{Log}\left[\frac{p_p}{n_i^2}\left(\frac{\phi}{\Delta R_p\sqrt{2\pi}}\mathrm{Exp}\left[-\frac{(x_{n0}-R_p+t_0)^2}{2\Delta R_p^2}\right]-p_0\right)\right]. \tag{2.42}$$

Fig. 2.9 shows the depletion layer thicknesses as a function of the applied voltage across the junction, calculated with Eqs. (2.36 to 2.42) for a junction with Gauss-

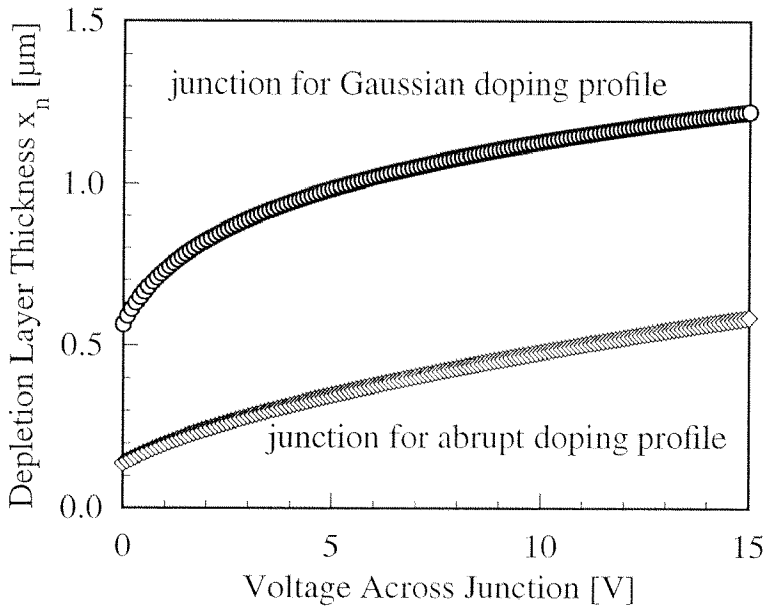


Fig. 2.9: Depletion layer thicknesses calculated with Eqs. (2.36 to 2.40) for junctions with a Gaussian and an abrupt doping profile. The doping concentrations and the corresponding depths are according to Fig. (2.7).

ian and abrupt doping profiles. The doping profiles are as given in Fig. 2.7. In a Gaussian doping profile near the junction at the n-/p-interface, larger values of the depletion layer thickness occur which are due to the lower absolute doping level according to Eq. (2.34).

Once the voltage dependent thickness of the depletion layer is known, the input resistance of the ideal Hall plate can be calculated (see Fig. 2.10). According to Ohm's law, the resistance can be described by a differential equation

$$dR = \frac{dV}{I} = \frac{dx}{\overline{N_D}(V)\overline{\mu_n}(V)\overline{w}(V)t(V)q}, \tag{2.43}$$

with dV as the voltage drop, I the biasing current, $\overline{N_D}(V)$ the equivalent doping concentration over the conductive thickness of the active region $t(V)$, $\overline{\mu_n}(V)$ the equivalent electron mobility, and $\overline{w}(V)$ the equivalent width of the active region.

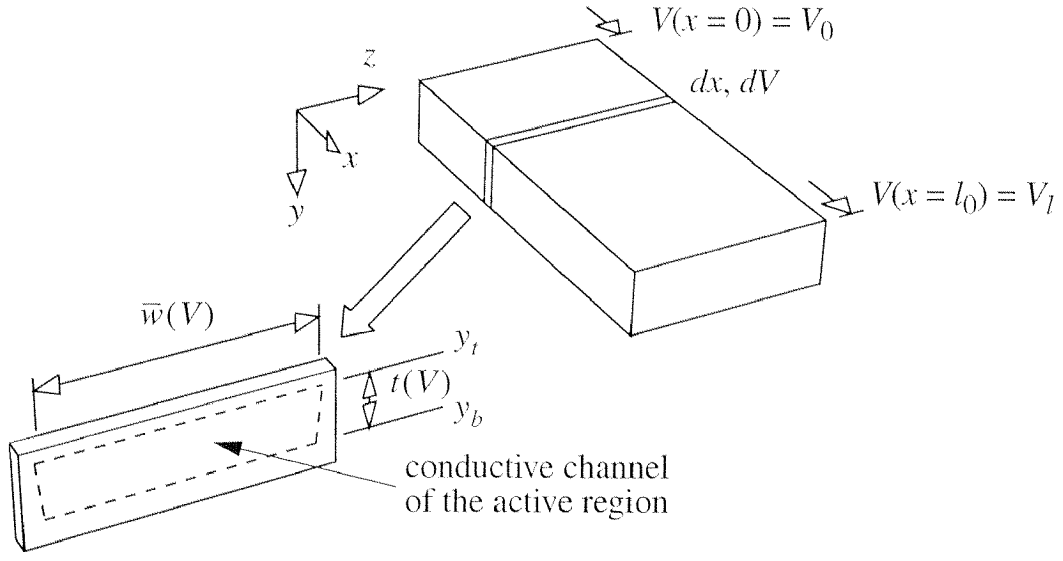


Fig. 2.10: Integration over the conductive channel of the active region. Current flow in a volume element of length dx occurs in a channel of width $\overline{w}(V)$ and thickness $t(V)$.

The denominator on the right-hand side of Eq. (2.43) follows from the integration over the thickness $t(V)$

$$\overline{N_D}(V)\overline{\mu_n}(V)t(V) = \int_{y_t(V)}^{y_b(V)} N_D(y)\mu_n(N_D(y))dy, \tag{2.44}$$

with

$$N_D(y) = \frac{\phi}{\sqrt{2\pi}\cdot\Delta R_p}\cdot\exp\left[-\left(\frac{y-R_p}{\sqrt{2}\cdot\Delta R_p}\right)^2\right], \tag{2.45}$$

and [35]

$$\mu_n(N_D(y)) = 232 + \frac{1180}{1 + ((N_D(y))/8 \times 10^{16})^{0.9}} \text{ [cm}^{-3}\text{]}. \tag{2.46}$$

The integration boundaries in Eq. (2.44) are

$$y_t(V) = \begin{cases} t_m & \text{without p}^+\text{-cover} \\ t_p + x_n^t(V) & \text{with p}^+\text{-cover} \end{cases} \quad \text{and} \quad y_b(V) = t_0 - x_n^b(V), \tag{2.47}$$

with

$$y_t(V) + t(V) = y_b(V). \tag{2.48}$$

Here, $y_t(V)$ is the top boundary and $y_b(V)$ the bottom boundary of the active region, t_m the top boundary without p^+-cover layer, $x_n^t(V)$ the depletion layer in the active region due to the p^+-cover layer, and $x_n^b(V)$ the depletion layer due to the Gaussian doping profile at the bottom of the active region.

The equivalent width of the active region $\overline{w}(V)$ is due to the junction field effect a voltage dependent function. Furthermore, the equivalent width changes in the perpendicular y-direction because of a changing depletion layer thickness. In order to simplify the model, the width $\overline{w}(V)$ is approximated by a factor λ

$$\overline{w}(V) = w_0 - \lambda x_n^b(V), \tag{2.49}$$

where λ is determined by experimental results. Finally, a solution of Eq. (2.43) is found by integrating the voltage drop in the x-direction

$$\int_{V_0}^{V(x)} (w_0 - \lambda x_n^b(V)) \int_{y_t(V)}^{y_b(V)} N_D(y)\mu_n(N_D(y))dydV = \frac{Ix}{q}, \tag{2.50}$$

with the boundary conditions

$$\begin{aligned} V(x = 0) &= V_0 \,, \\ V\left(x = \frac{l_0}{2}\right) &= V_m \,, \\ V(x = l_0) &= V_l \,, \end{aligned} \tag{2.51}$$

to yield the input resistance $R = V_l/I$ and the common-mode voltage V_m generated at the point sense contacts (see Fig. 2.6).

In order to calculate the sensitivity S_a of an ideal Hall plate in the presence of the junction field effect, Eq. (2.20) is modified by the equivalent doping concentration $\overline{N_D}(V)$ and the thickness of the conducting active region $t(V)$

$$S_a = \frac{r_H I}{q\overline{N_D}(V)t(V)}, \tag{2.52}$$

where $r_H = r_2$ is the Hall scattering factor (see Tab. 2.1). For a simplified model, we assume an active region of uniform thickness of a value corresponding to that in the middle in the Hall plate (i.e. at V_m). Therefore, Eq. (2.52) needs to be evaluated at $V = V_m$,

$$S_a = \frac{r_H I}{q \int\limits_{y_t(V_m)}^{y_b(V_m)} N_D(y)dy}. \tag{2.53}$$

2.3 The Theory of the Spinning Current Method

A major drawback of Hall plates is their high offset voltage, i.e. the output voltage at the sense contacts in the absence of a magnetic induction. Also contributing to the offset are all physical effects which cause an asymmetry in the potential distribution of the active region. Possible sources include piezoresistive effects, geometrical errors, temperature gradients, non-linear material properties, etc. [36]. Additionally, the various offset sources may change over the lifetime of the sensor.

Several methods for offset reduction in Hall plates are known [37 to 40]. However, one of the most powerful techniques, which reduces the offset dynamically is the spinning current method. First proposed in [38], it has been subject for many publications [36, 41 to 43]. The basic idea of the spinning current method deals with measuring the output voltage of, e.g., a multi-contact Hall plate for different directions of the biasing current I (see Fig. 2.11). Averaging the output signal over one full switching period of 360° separates the spatially periodic offset voltage from the Hall voltage.

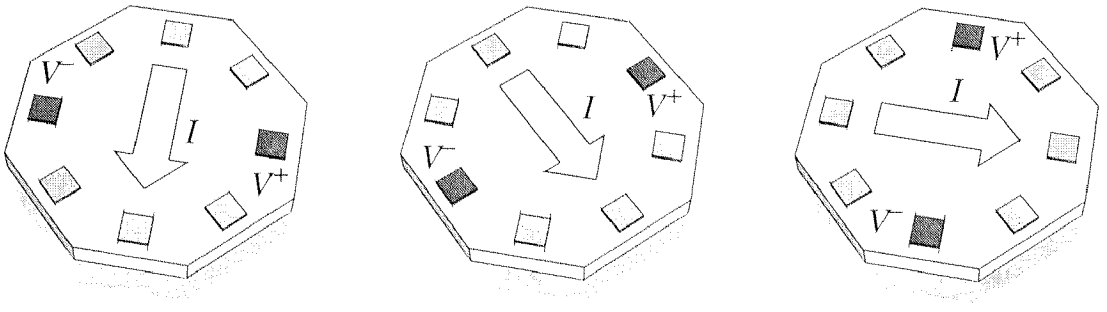


Fig. 2.11: Symmetric spinning current Hall plate with eight contacts [41]. The output voltage is measured at the contact pair perpendicular to the direction of the biasing current.

The spinning current offset reduction scheme results in a limited frequency response due to the discrete sampling [44]. Therefore, a detailed knowledge of the offset sources becomes indispensable in order to choose, e.g., the minimum sampling frequency in order to cancel all significant contributions.

Basic Considerations

The first step towards a better understanding of the offset sources is a proper mathematical description of the problem. In general, the output voltage of a Hall plate $V_{H,O}$ can be separated into the Hall voltage V_H and an offset voltage V_O with a spatial dependence on φ such that

$$V_{H,O}(B, I, \varphi) = V_H(B, I) + V_O(I, \varphi). \tag{2.54}$$

According to [41] the offset voltage is of a periodic nature

$$V_O(I, \varphi) = V_O(I, \varphi + 2\pi), \tag{2.55}$$

and, therefore, can be described by a Fourier series [36]

$$V_O(I, \varphi) = \sum_{n=0}^{\infty} a_n(I) \cdot \sin(n\varphi + \nu_n). \tag{2.56}$$

However, experimental results as will be seen in section 3.2, suggest that the significant contributions to the offset voltage occur only up to $n = 6$ in the Fourier series expansion. This coincides with the fact that in crystalline silicon rotational symmetries can occur up to the sixth order [45]. Furthermore, odd components can be neglected since they can always be cancelled by a reverse bias

$$V_O(I, \varphi) + V_O(I, \varphi + \pi) = V_O(I, \varphi) + V_O(-I, \varphi) =$$

$$\sum_{n=0,2,4,6} 2a_n(I) \cdot \sin\left(n\varphi + \nu_n + \frac{n\pi}{2}\right) \cdot \cos\left(\frac{n\pi}{2}\right). \tag{2.57}$$

Assuming the magnetic induction equals zero, the Fourier components can be divided into components originating from physical effects independent of the biasing current, and, into components resulting from effects of a linear or a non-linear dependence on the biasing current, similar to [46]. However, any physical effects which induce an offset that is independent of bias is equivalent to superimposing voltages to the voltage measured at a contact pair of the Hall

plate. Consequently, they only occur in odd orders in the Fourier series, and, therefore, can be neglected.

The case of a four contact Hall plate with an active region of ohmic material in the absence of a magnetic induction is considered. This Hall plate structure can be described by an equivalent circuit consisting of six ohmic resistors [47] (see Fig. 2.12). Since all offset voltages with a linear current dependence can be described by a ohmic resistor, they can also be taken into account in the equivalent circuit. The difference of the contact voltages V_{ij} can be defined as

$$V_{ij} = V_i - V_j = R_{ij} \cdot I_{ij}, \tag{2.58}$$

where $V_{i,j}$ is the contact voltage, I_{ij} the applied current and R_{ij} the resistance between contact i and j. The six ohmic resistors of the equivalent circuit are described by their conductances g_{hk} (see Fig. 2.12).

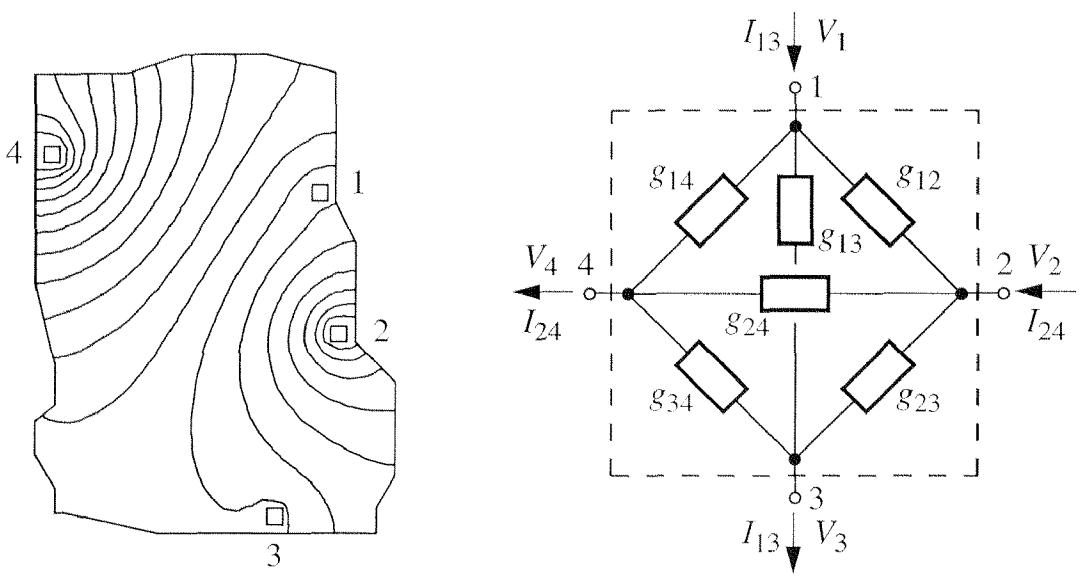


Fig. 2.12: Layout of a four contact Hall plate (left) and the corresponding equivalent circuit with six ohmic resistors. Current is applied either at contact pair (1,3) or at pair (2,4). The offset voltages are measured at the contact pair (2,4) or at (3,1), respectively.

A biasing current at the appropriate contact pair leads to

$$V_{24} = \frac{g_{12}+g_{14}+g_{23}+g_{34}}{g_{12}g_{34}-g_{14}g_{23}} I_{13} + V_{13\text{const.}} \cdot R_{24} ,$$
$$V_{31} = \frac{g_{12}+g_{14}+g_{23}+g_{34}}{g_{14}g_{23}-g_{12}g_{34}} I_{24} - V_{24\text{const.}} \cdot R_{13} , \qquad (2.59)$$

resulting in

$$I_{13} = I_{24} = I \quad \Rightarrow \quad V_{24}+V_{31} = 0 . \qquad (2.60)$$

Therefore, offset voltages with a linear current dependence are always cancelled by spinning the biasing current of a four contact Hall plate of arbitrary shape.

The influence of non-linear offset contributions on the components of the Fourier series is of a more complex nature. Hence, only a simple model is considered to approximate the non-linear behavior of a Hall plate (see Fig. 2.13). A simple way is to use a Wheatstone bridge with generic, non-linear resistances k_{ij} described by

$$k_{ij} = a_{ij}R(I) \quad \text{with} \quad R(I) = \frac{c_1}{1-c_2 I} . \qquad (2.61)$$

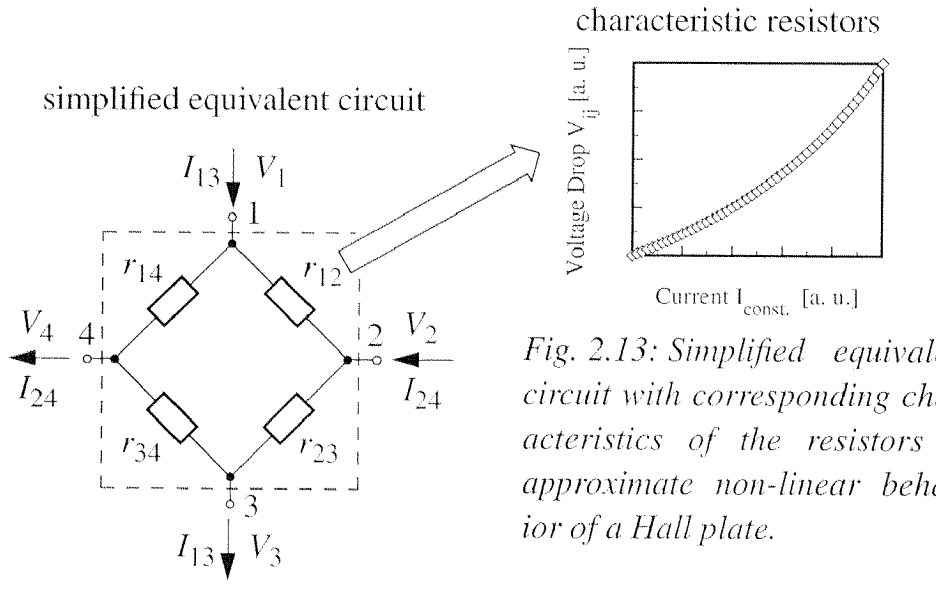


Fig. 2.13: Simplified equivalent circuit with corresponding characteristics of the resistors to approximate non-linear behavior of a Hall plate.

Here, I denotes the biasing current, and, a_{ij}, c_1 and c_2 arbitrary constants. The voltages caused by the biasing current at opposite contacts are calculated as:

$$V_{24} = V_2(I_{13}) - V_4(I_{13}) = \frac{f(c_1, c_2)}{\left(1 - \frac{c_2}{2} I_{13}\right)(a_{12} - a_{23})(a_{14} - a_{34})}, \quad (2.62)$$

$$V_{31} = V_3(I_{24}) - V_1(I_{24}) = -\frac{f(c_1, c_2)}{\left(1 - \frac{c_2}{2} I_{13}\right)(a_{12} - a_{14})(a_{23} - a_{34})}, \quad (2.63)$$

$$V_{42} = V_4(-I_{13}) - V_2(-I_{13}) = V_{24}, \quad (2.64)$$

$$V_{13} = V_1(-I_{24}) - V_3(-I_{24}) = V_{31}. \quad (2.65)$$

Depending on the value of a_{ij} different cases for the offset voltages can be distinguished (see Tab. 2.3). Case *A* requires at least one symmetry axis through a contact pair. In case *B*, two orthogonal symmetry axes between contact pairs are required. All other cases (case *C*) result in offset voltages which are not cancelled by the spinning current method.

A	***B***	***C***
$\frac{a_{14}}{a_{12}} = \frac{a_{34}}{a_{23}}$	$a_{14} = a_{23}$ $a_{12} = a_{34}$	***others***
$V_{24} = V_{31} = 0$	$V_{24} = -V_{31}$	$V_{24} \neq V_{31}$

Tab. 2.3: Different cases of the occurrence of non-linear offset-voltages.

To conclude, in the ideal case, offset voltages caused by physical effects independent of, or linear to, the biasing current are cancelled by spinning a four contact Hall plate. However, to cancel or reduce offset voltages with a non-linear current dependence, a Hall plate with maximum possible symmetry is needed with respect to the layout and the physical properties acting on the plate. The number of contact pairs required will be the subject of the following chapters.

The Theory of Continuous Spinning Current Offset Reduction Method

In order to generate a spinning current vector with more than four directions per complete switching period of 360°, a multi-contact Hall plate is necessary [41]. However, a more elegant method is by the continuous spinning current scheme [18]. This method allows the offset voltage of a four contact Hall device to be to decomposed into its Fourier components of arbitrary order.

Sinusoidal biasing currents, phase shifted by 90°, are applied to the two contact pairs (13) and (24) of a symmetrical four contact Hall plate (see Fig. 2.14):

$$I_{13}(\varphi) = I_0 \cdot \cos(\varphi) , \tag{2.66}$$

$$I_{24}(\varphi) = I_0 \cdot \sin(\varphi) , \tag{2.67}$$

where I_0 is the current amplitude and φ the switching angle. The superposition results in a net-current I_0 in the Hall plate whose direction is continuously spinning with the unit vector $\hat{n}$.

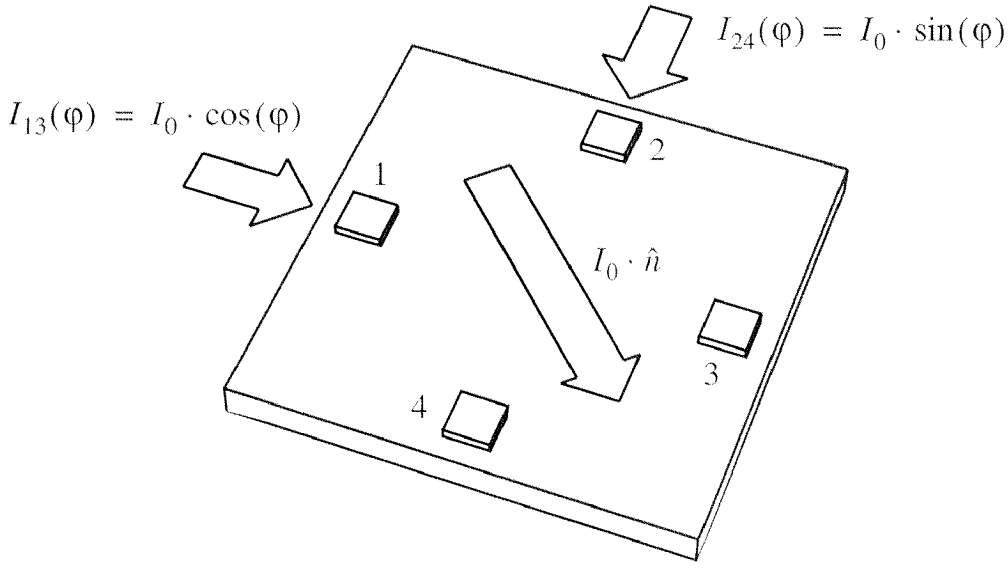


Fig. 2.14: Schematic view of a symmetrical four contact Hall plate with Greek cross shape and contact pairs (1,3) and (2,4). Harmonic biasing currents $I_{13}(\varphi)$, and $I_{24}(\varphi)$ are applied to the Hall plate. These result in a continuous spinning current vector.

Between corresponding contact pairs, the voltages

$$V_{13}(B, \varphi) = V_R(\varphi)\cos(\varphi) - V_{H,O}(B, \varphi)\sin(\varphi), \tag{2.68}$$

$$V_{24}(B, \varphi) = V_R(\varphi)\sin(\varphi) + V_{H,O}(B, \varphi)\cos(\varphi), \tag{2.69}$$

are measured. These consist of a resistive part $V_R(\varphi)$ in phase with the unit vector $\hat{n}$, and a superposition of the Hall and the periodic offset voltage $V_{H,O}(B, \varphi) = V_H(B) + V_O(\varphi)$, orthogonal to the unity vector $\hat{n}$ (see Figs. 2.15 and 2.16). The value of $V_{H,O}(B, \varphi)$ can be determined using

$$V_{H,O}(B, \varphi) = V_{24}(B, \varphi)\cos(\varphi) - V_{13}(B, \varphi)\sin(\varphi). \tag{2.70}$$

The Hall voltage and the superimposed periodic offset voltage are expressed as a Fourier series

$$V_{H,O}(B, \varphi) = \sum_{k=0}^{\infty} V_k(B) \cdot \sin(k\varphi + \lambda_k). \tag{2.71}$$

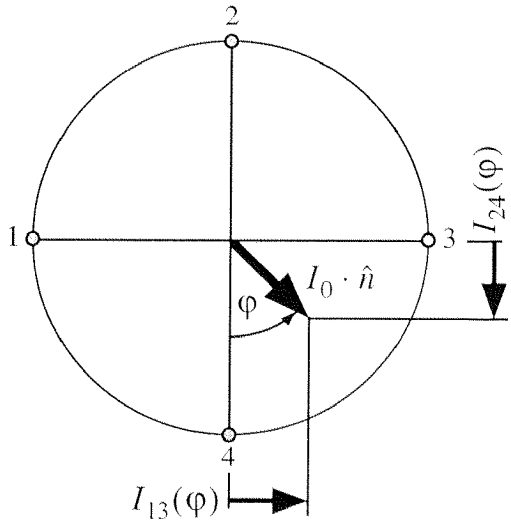


Fig. 2.15: Vector diagram of the two biasing currents $I_{13}(\varphi)$ and $I_{24}(\varphi)$ resulting in the net current $I_0 \cdot \hat{n}$.

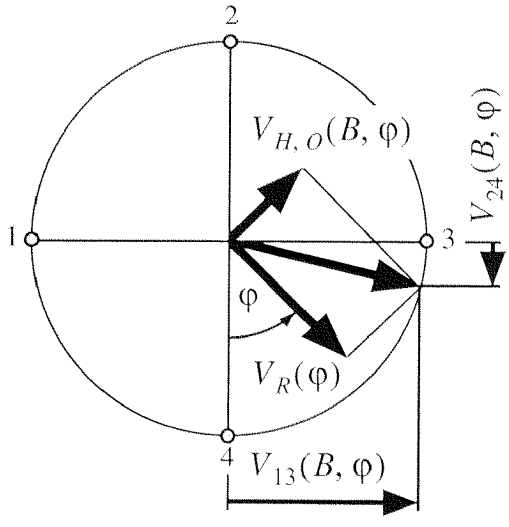


Fig. 2.16: The voltage drop $V_R(\varphi)$ due to I_0, its orthogonal part $V_{H,O}(B, \varphi)$, and the projections $V_{13}(B, \varphi)$ and $V_{24}(B, \varphi)$.

Thus, the offset voltage is described in terms of amplitudes $V_k(B)$, and phase shifts λ_k of various Fourier components.

The Hall voltage $V_H(B)$ and the residual offset V_O which cannot be cancelled with the spinning current method is obtained by averaging Eq. (2.71) over one full switching period of 2π. This results in

$$\int_0^{2\pi} V_{H,O}(B, \varphi) d\varphi = V_0(B) = V_H(B) + V_O. \tag{2.72}$$

Symmetry considerations of the silicon crystal and experiments suggest that only a limited number of Fourier components contribute to the offset voltage [45], i.e., $V_k(B) \equiv 0$ for $k > k_{\text{limit}}$. Then, a limited number of measurements of $2k_{\text{limit}}$ per period is sufficient for a substantial offset reduction.

Physical Effects Causing Offset Voltages

A multitude of physical effects causes asymmetry in the potential distribution of a Hall plate to produce an offset voltage. The following considerations focus only on effects such as geometrical errors, piezoresistive effects, and non-linearities due to the junction field effect. These sources will be identified as the main players in contributing to the offset voltage as shown in *chapter 3*. Other effects, mainly thermal in nature, are of minor influence as described in [42].

i) geometrical errors

Geometrical errors are mainly caused by imperfections in the fabrication process [42]. Furthermore, external mechanical forces may change the physical shape of the Hall plate. However, in the absence of non-linearities, geometrical errors can be treated as a linear source of offset, and, therefore, can be described by an equivalent circuit of six resistors as shown in Fig. 2.12. In a similar sense, material inhomogeneities can be treated the same way and can also be classified as geometrical errors. According to Eq. (2.59) and corresponding symmetry considerations, geometrical errors influence the second order terms in the spatial Fourier series of Eq. (2.56), and, are cancelled by spinning the biasing current of a four contact Hall plate.

ii) mechanical stress

The effect of mechanical stress is the main cause of the offset voltage of a Hall sensor [42]. In the presence of stress, the band structure of an n-type active region results in energy shifts, distortion and non-degeneracy [48]. The transport of electrons becomes anisotropic and the current flow may no longer be perpendicular to the electric field. The effects of mechanical stress on electrical transport can be due to piezoresistivity, piezo-Hall and piezojunction effects [1, 49 to 51]. The piezo-Hall effect occurs only in the presence of an applied magnetic induction $\boldsymbol{B}$ and does not contribute to the offset voltage by definition. The piezojunction effect is only significant close to the fracture limit of silicon and can be neglected in realistic situations [52].

The multitude of stress effects, such as energy band shifts, change of effective mass, or alteration in mobility, on the majority carrier current flow in a semicon-

ductor can be attributed to the piezoresistive effect. For not too large stress levels, the change in electrical conductivity is linearly related to the mechanical stress. The stress dependence of the offset voltage has been described by use of a Wheatstone bridge as an equivalent circuit model for the Hall plate [53,54]. This model is inaccurate since the current distribution in the active region of a Hall plate is far more complex in nature (see Fig. 2.17). Here, conduction in the Hall plate is governed by the generalized Ohm's law for an anisotropic material. This approach is using analytical means usually evaluated employing numerical finite element simulations. For a simplified analysis, we consider a finite region in the middle of the Hall plate far from all boundaries (see Fig. 2.17).

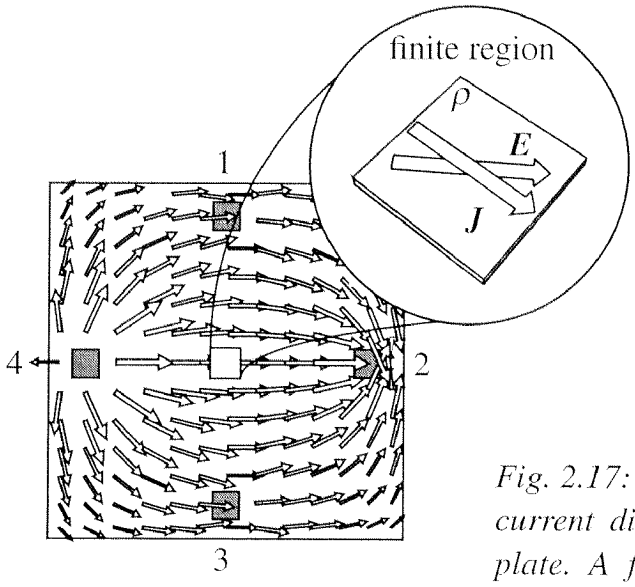


Fig. 2.17: Finite element simulation of the current distribution of a rectangular Hall plate. A finite active region is shown in exploded view. In the presence of a magnetic induction $\boldsymbol{B}$*, the resistivity is anisotropic and the electric field* $\boldsymbol{E}$ *and the current density* $\boldsymbol{J}$ *are not necessarily co-linear.*

The electric field $\boldsymbol{E}$ and current density $\boldsymbol{J}$ are related by Ohm's law

$$\boldsymbol{E} = \rho \boldsymbol{J} \tag{2.73}$$

where ρ is the resistivity tensor. In the presence of mechanical stress at zero magnetic induction, the resistivity ρ is anisotropic and described by a symmetric second rank tensor. For sufficiently small stress levels [55 to 57], the resistivity components are linear functions of the stress components and can be expressed, in reduced index notation where 1, 2, 3, 4, 5, 6, corresponds to 11, 22, 33, 13, 23, 12, respectively, [58, 59], as

$$\rho_\alpha = \rho_\alpha^0 + \Delta\rho_\alpha = \rho_\alpha^0 + \bar{\rho} \cdot \pi_{\alpha\beta} \cdot \sigma_\beta \quad \text{with} \quad \bar{\rho} = \frac{\rho_1^0 + \rho_2^0 + \rho_3^0}{3}, \tag{2.74}$$

where the ρ_α^0 are the resistivity components for a stress free material, $\pi_{\alpha\beta}$ the piezoresistive coefficients and σ_β the mechanical stress.

Using standard tensor transformation rules [59], Eq. (2.73) can be expanded to read as

$$E'_1/\bar{\rho} = \left[[\pi_{11} - \pi_{12}]\sigma_{s6}\sin(2n\varphi) + \frac{1}{2}\pi_{44}(\sigma_{s1} - \sigma_{s2})\cos(2n\varphi)\right]J'_1 + \left[1 + \frac{1}{2}[\pi_{11} + \pi_{12}](\sigma_{s1} + \sigma_{s2}) + \pi_{12}\sigma_{s3}\right]J'_1 \quad , \tag{2.75}$$

$$E'_2/\bar{\rho} = \left[[\pi_{11} - \pi_{12}]\sigma_{s6}\cos(2n\varphi) - \frac{1}{2}\pi_{44}(\sigma_{s1} - \sigma_{s2})\sin(2n\varphi)\right]J'_1 \quad , \tag{2.76}$$

$$E'_3/\bar{\rho} = [\pi_{44}\sigma_{s4}\cos(n\varphi) + \pi_{44}\sigma_{s5}\sin(n\varphi)]J'_1 \quad , \tag{2.77}$$

in accordance to the axes system given in Fig. (2.18). The mechanical stress in the above system of equations is expressed in terms of reduced index notation.

In Eq. (2.75), we recognize the stress dependence of the resistivity along the direction of current J'_1. For purpose of illustration a graphical representation of Eq. (2.75) is shown in Fig. 2.19. A detailed discussion can be found in [60, 61]. Relevant to this work is Eq. (2.76), which shows the electric field generated perpendicular to the current flow. This can be identified as a source of offset. The direction dependence appears in the second harmonic of the rotation angle φ (see Fig. 2.20).

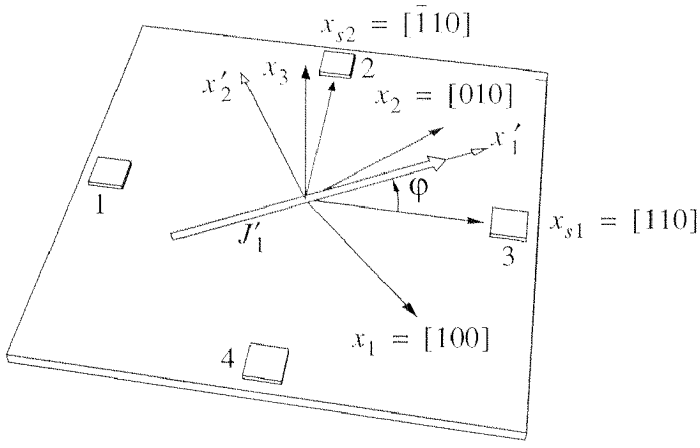


Fig. 2.18: Illustration of the axes system used in Eqs. (2.75 to 2.77). Unprimed system (x_1, x_2, x_3) *aligned with the principal symmetry axes of the cubic crystal, the system* (x_{s1}, x_{s2}, x_{s3}) *aligned with coordinate axes of the Hall sensor and the primed system* (x_1', x_2', x_3') *which rotates in phase with the spinning current vector. The phase angle* φ *is defined between the primed system and the coordinate system of the Hall sensor.*

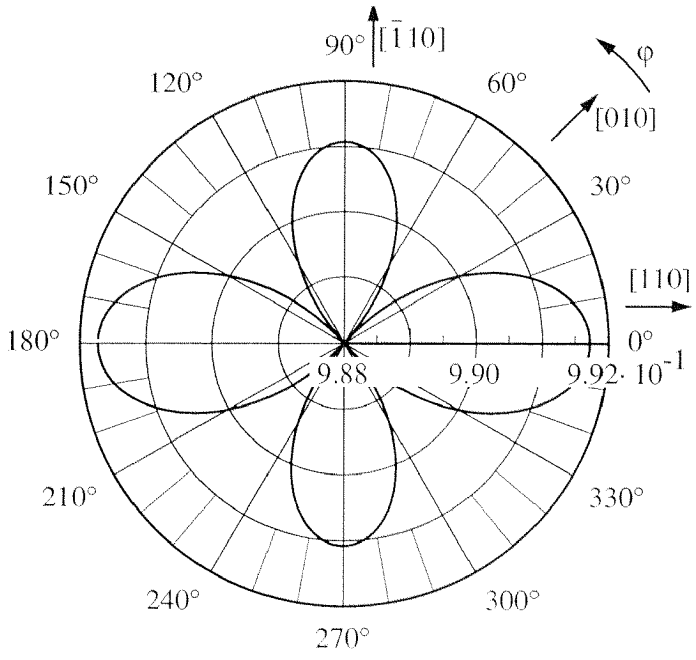


Fig. 2.19: The normalized piezoresistance function $f_{\pi,\sigma}(n\varphi_s)$ *of an n-type Hall plate with* $E_1' = f_{\pi,\sigma}(n\varphi_s)J_1'$ *and the π-coefficients according to [48] under uniaxial tensile stress* σ_{s1} *of 50 MPa.*

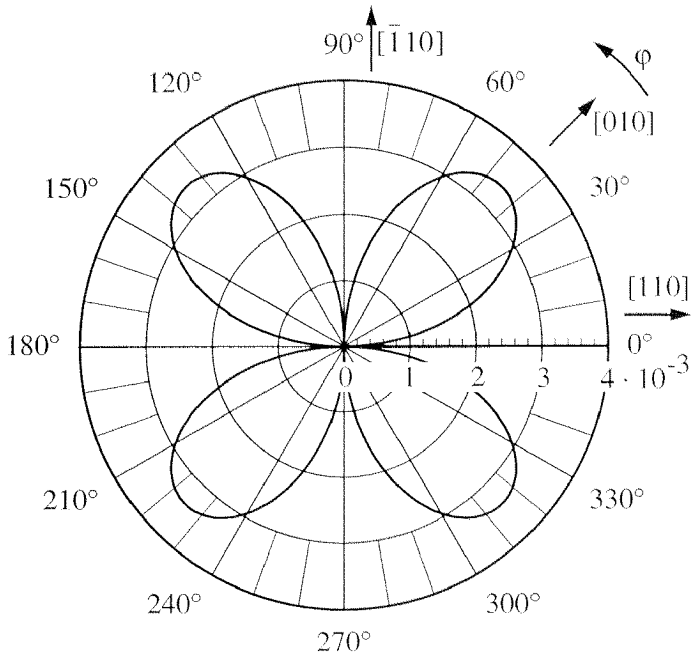


Fig. 2.20: The normalized perpendicular piezoresistance function $g_{\pi,\sigma}(n\varphi_s)$ of n-type Hall plate with $E'_2 = g_{\pi,\sigma}(n\varphi_s)J'_1$ and the π-coefficients according to [48] under uniaxial tensile stress σ_{s1} of 50 MPa.

The expression given in Eq. (2.76) consists of a part which is linear to the axial mechanical stress $(\sigma_{s1} - \sigma_{s2})$, and a part that is linear to shear stress σ_{s6}. Depending on the mechanical stress distribution in the real physical device, e.g. from the packaging [58], an appropriate device orientation has to be chosen to minimize the offset. Note that the angular dependence on φ in Eq. (2.76) is similar to that in Eq. (2.75), but phase shifted by 45°. In addition, the current flow J'_1 in x'_1-direction generates an electric field E'_3 in the x'_3-direction.

iii) junction field effect

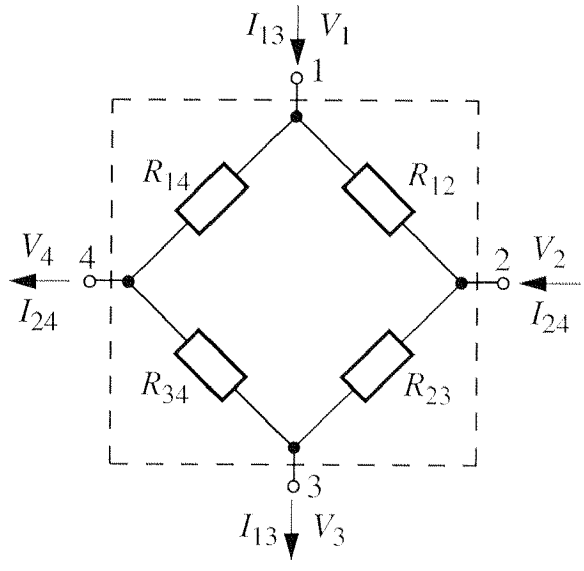
Due to the junction field effect (see section 2.2) the geometry of a Hall device is changed by external biasing conditions and by the voltages generated across the isolating junction as seen in Eq. (2.77). These voltages give rise to periodic offset voltages in the first to sixth order of the switching angle φ. Additionally, the non-linear junction field effect, in combination with geometrical errors, may cause offset voltages which are not cancelled by the spinning current method (see section 2.3). In the following discussion only the ideal case of perfect symmetry for the device geometry will be considered. However, calculations concerning the

junction field effect result in an implicit solution. Therefore, only a simplified numerical model is introduced for behavioral description.

Assuming an abrupt doping profile, the input resistance of an ideal Hall plate can be calculated according to [32]

$$\frac{dV(x)}{dx} = I \cdot \frac{\rho(\sigma)}{w_0} \cdot \frac{1}{t_0 - c\sqrt{V_I - V(x)}}, \tag{2.78}$$

with a stress dependent resistivity $\rho(\sigma)$ (see Figs. (2.6) and (2.10) for notation used). In Eq. (2.78) c denotes a material constant, V_I an internal voltage such as the built-in voltage (see Eq. (2.35)), and $V(x)$ the voltage drop in the x-direction due to the biasing current I. Once the input resistance of the active region due to the junction field effect is known, a simplified equivalent circuit according to Fig. (2.13) gives a behavioral description of the Hall device when operated by continuous spinning current (see Fig. 2.21). For symmetric biasing conditions, the averaged voltage of V_1 to V_4 is kept constant at V_{Center}. Additionally, the electric field of Eq. (2.77) is taken into account by superimposing the internal voltage V_I of resistor R_{12} and R_{34} by a voltage $\propto \sin(\varphi + \lambda)$, and voltage V_I of resistor R_{14} and R_{23} by a phase shifted voltage $\propto \cos(\varphi + \lambda)$.



$$I_{13}(\varphi) = I \cdot \cos(\varphi)$$
$$I_{24}(\varphi) = I \cdot \sin(\varphi)$$

Fig. 2.21: Simplified equivalent circuit model with non-linear resistances R_{ij} calculated according Eq. (2.78) and operated by continuous spinning current. For symmetric biasing conditions, the averaged voltage of V_I to V_4 is kept at a constant voltage V_{Center}.

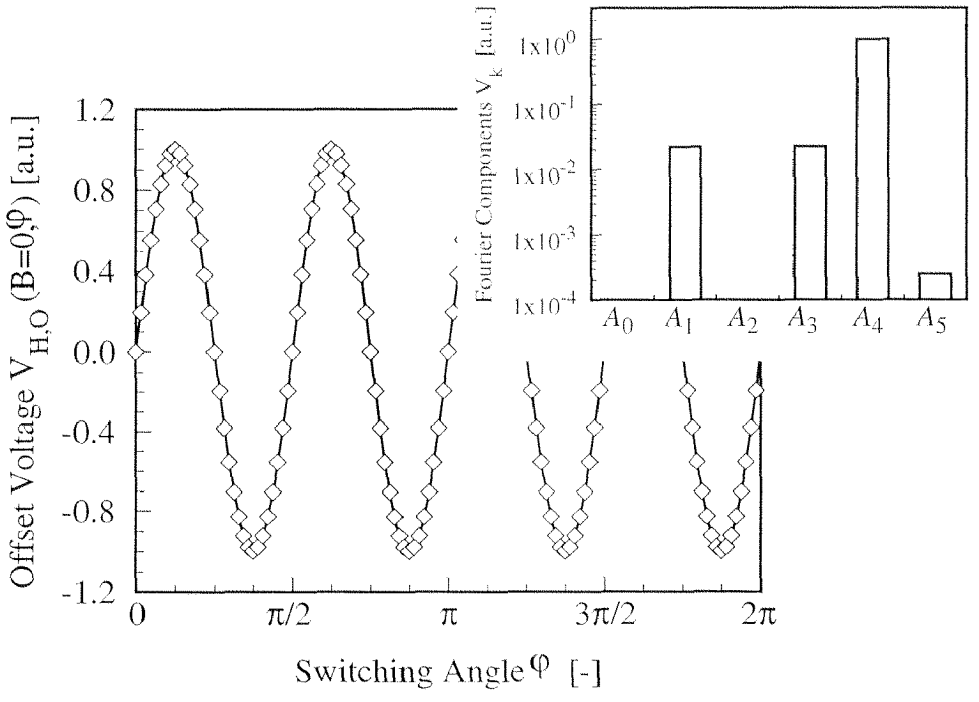


Fig. 2.22: Periodic offset voltage $V_{H,O}(B, \varphi)$ in arbitrary units due to the junction thickness modulation. The inset shows the Fourier components A_k up to the sixth order ($V_{H,O}(B, \varphi) = \sum_n A_n \sin(n\varphi + \lambda_n)$).

The calculations predict a periodic offset voltage $V_{H,O}(B, \varphi)$ with contributions to the fourth order terms. The zero transitions coincide with the symmetry axis along the contacts of the Hall device. This indicates that fourth order contributions are unique to the continuous spinning current method and the phase angle is set by device symmetry. Additionally, contributions to the odd order terms occur as a result of the superimposed electric field of Eq. (2.77).

The angular dependence of the piezoresistivity in the second order term generates aliasing products. These products give rise to small contributions in the Fourier spectrum of second and sixth order in the switching angle φ. Note that aliasing effects due to piezoresistance are not taken into account in the above model.

2.4 The Theory of the Double-Hall Sensor

In addition to the initial calibration of the output voltage of a Hall plate, there are several dynamic offset reduction techniques. A common method is based on the orthogonal coupling of two identical Hall plates [37]. While in the ideal case, the Hall plates have equal magnetic responses and offset voltages of opposite sign, in practice this offset reduction technique is strongly limited by the matching of the physical properties of the active regions of the two Hall plates. As an improvement, the same active region is measured twice by orthogonally switching the operating regime, such as in the spinning current method [31] (see section 2.3.). However, this method exhibits only a limited frequency range due to switching. A different dynamic offset reduction method has been proposed for the double-Hall sensor [40]. It is similar to the method described in [39] and combines the advantages of known reduction techniques, whereby the same active region is simultaneously measured twice.

The double-Hall sensor consists of two single ended Hall devices A and B sharing the same active region (see Fig. 2.23). Device A is controlled from the contacts in the left row by the current I_A which generates a field dependent Hall voltage V_A. Device B is controlled from the contacts in the row on the right by current I_B delivering signal V_B.

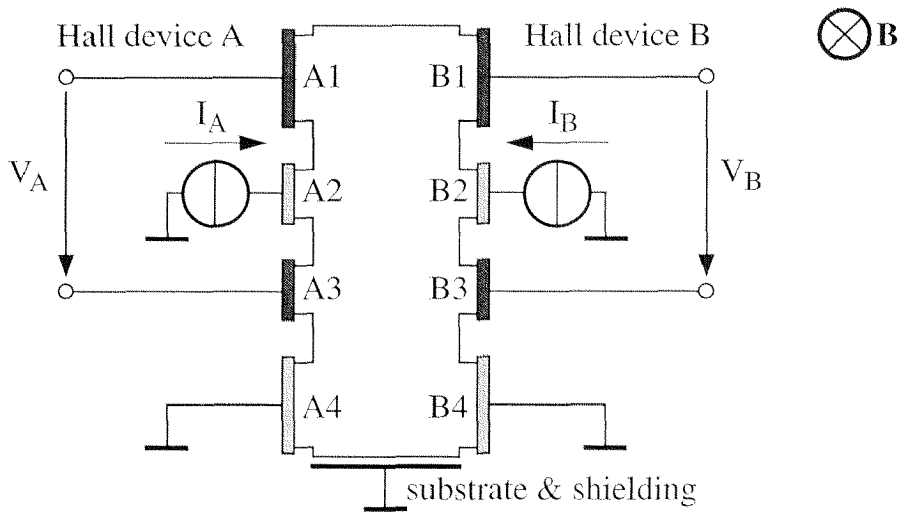


Fig. 2.23: Operating principle of the double-Hall sensor. The current I_A of Hall device A generates a field dependent output $V_A(B)$, and the current I_B of device B results in a field dependent output $V_B(B)$.

Hall devices *A* and *B* operate independently from each other in terms of changes of the Hall voltage, due to the changing biasing currents as shown by FEM (see Fig. 2.24). A variation of the current I_A only influences the sensitivity of device *A*, which is given by the slope of the curves, and depends linearly on I_A. At the same time, the sensitivity of device *B* operated at a constant current of $I_B = 100$ µA remains constant.

The effect of independent operation can be understood by means of the van der Pauw theorem [62]. According to the theorem, the occurrence of a Hall voltage for an active region of arbitrary shape requires an alternating arrangement of biasing and sense contacts. Therefore, a biasing current I_A at the contacts *A2* and *A4* generates a Hall voltage V_A between contact *A3* to any other contact (see Fig. 2.23). Consequently, no magnetic response is measured at the sense contacts *B1* and *B3* of Hall device *B*. The same applies for the biasing current I_B which has no influence on the magnetic response of Hall device *A*. To conclude, the sensitivity of each Hall device can be arbitrarily set, e.g., to sensitivities of opposite signs.

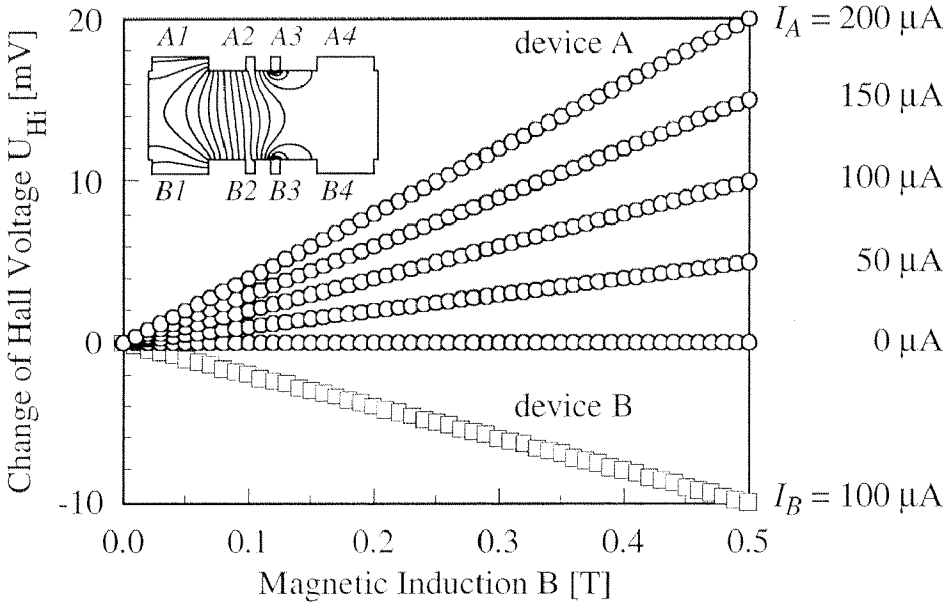


Fig. 2.24: The magnetic response of Hall device A and B simulated using FEM. The devices operate independently of each other. A variation of current I_A changes only the sensitivity of device A, which corresponds to the slope of the curve. The inset shows the calculated equipotential lines of a double-Hall sensor operated according to Fig.2.23.

The offset voltage can be reduced by taking advantage of the double-Hall sensor structure symmetry. The sensor consists of two single ended Hall devices merged on the same active region as shown in Fig. 2.23. The single ended Hall devices with contacts on one side of the device can be achieved by a transformation of a conventional rectangular Hall plate, as shown in Fig. 2.25, using the conformal mapping technique defined in section 2.2.

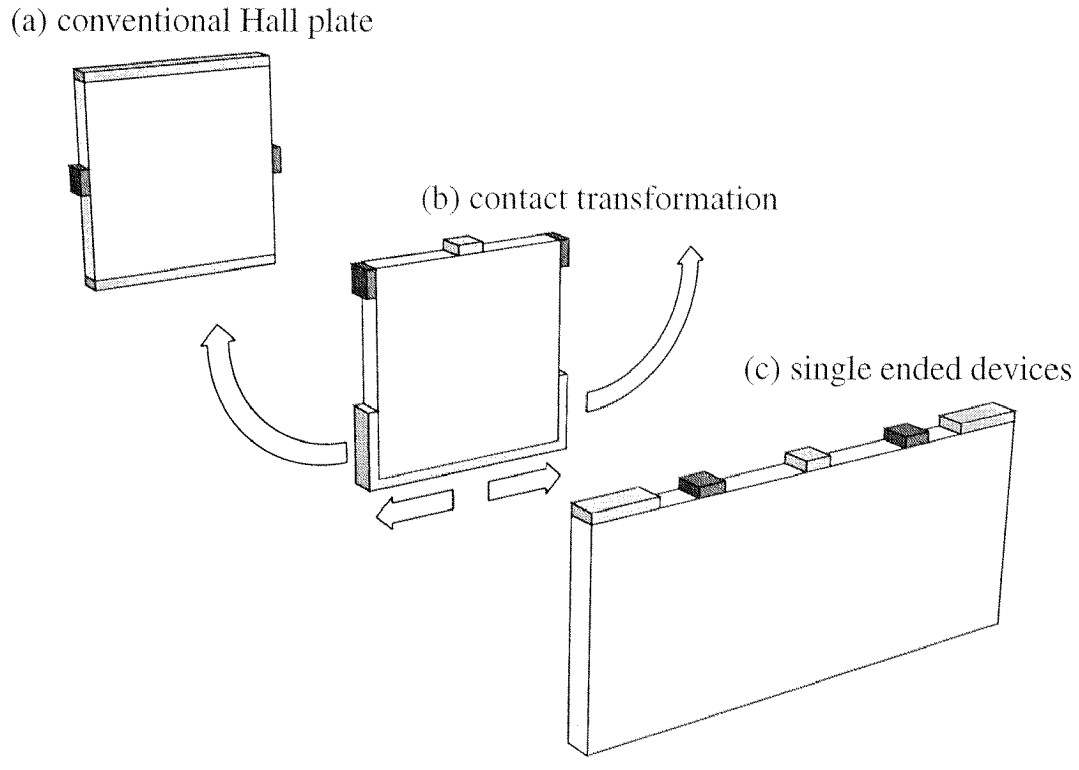


Fig. 2.25: The transformation of a rectangular Hall plate to a single ended device. In the first step, the contacts of the conventional Hall plate (a) are deformed in following way (b): the upper current contact (light grey) is shrunk, the sense contacts (dark grey) move to one side of the active region, and the lower current contact is pulled over its nearby edge and split into two half contacts. Finally, the active region (white) is understood as a rubber-like material; it is bent and stretched until all contacts end up on one side of the device (c).

The symmetry consideration starts with two single ended Hall devices A and B. Both Hall devices have the same orientation of current and voltage contacts with respect to the magnetic field direction. This results in an equal orientation of the Hall voltages $V_H^i(\boldsymbol{B})$ and the offset voltages $V_O^i(\boldsymbol{B})$ $(i = A, B)$ (see Fig. 2.26a). In Fig. 2.26b, Hall device A including its magnetic field direction is rotated by 180°. Then the magnetic field direction, and hence, the sign of $V_H^A(\boldsymbol{B})$ is reversed in order to have the same field orientation as Hall device B (see Fig. 2.26c). Finally, the active regions of both Hall devices are merged together to form the double-Hall sensor (Fig. 2.26d). For a given magnetic field direction and $I_A = I_B$, the Hall voltages are of opposite signs and the offsets of the single Hall devices are almost equal

$$V_H^A(\boldsymbol{B}) = -V_H^B(\boldsymbol{B}), \tag{2.79}$$

$$V_O^A = V_O^B. \tag{2.80}$$

The output signal of the double-Hall sensor is defined as the voltage difference

$$V_{AB} = V_A - V_B = 2V_H^{A,B}(\boldsymbol{B}) + (V_O^A - V_O^B). \tag{2.81}$$

The residual signal offset of the double-Hall sensor is expected to be very low. Offsets of the individual devices are mainly due to unavoidable geometrical errors [12]. Furthermore, errors due to manufacturing non-idealities do occur, as well as stress induced offset voltages (see section 2.3). However, since the individual Hall devices share the same active region, any drifts of the individual offset voltages over temperature are perfectly matched. Therefore, after a simple and low-cost calibration at any *arbitrary* temperature, a low offset over a wide temperature range can be obtained.

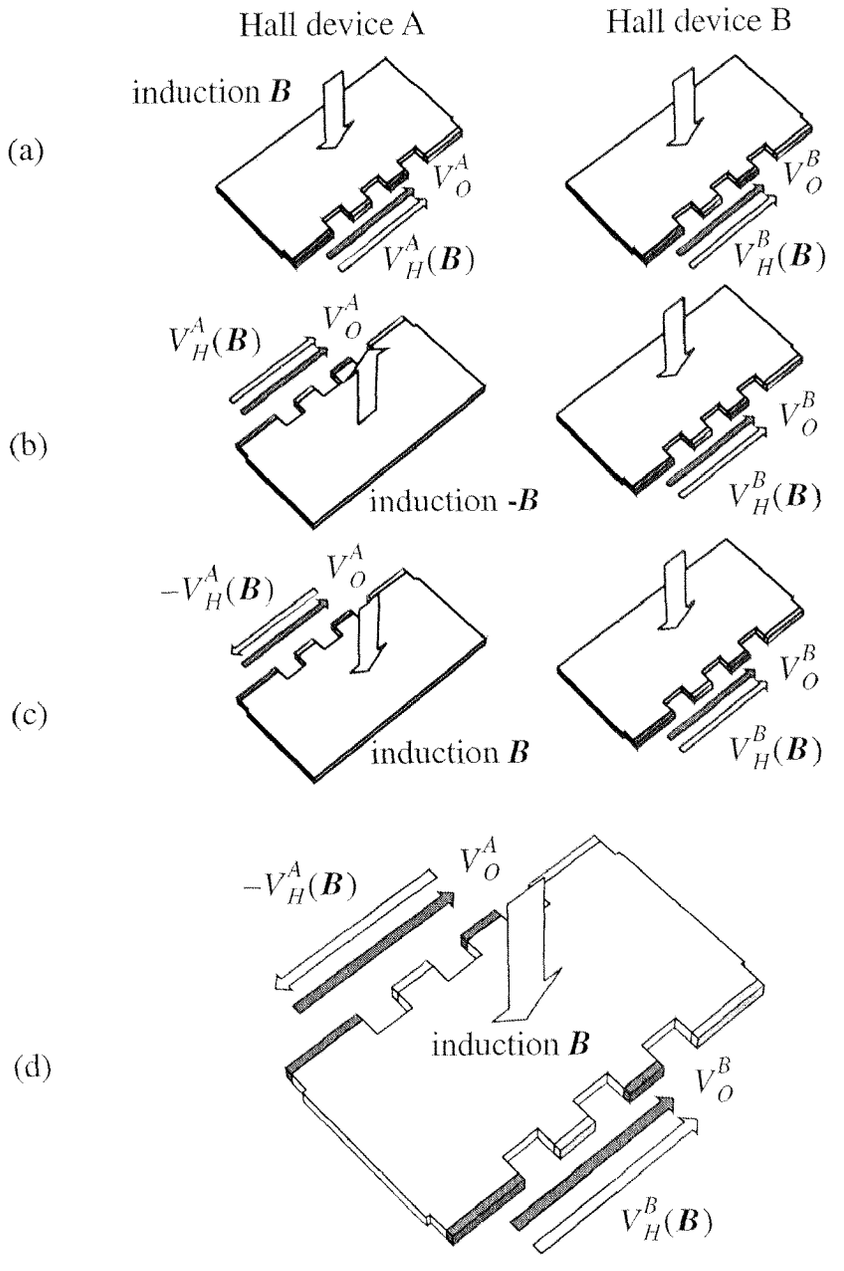


Fig. 2.26: The double-Hall sensor is a combination of two equal single ended Hall devices (a). Device A including its magnetic field direction is rotated by 180° (b). Then the magnetic field direction is reversed in order to have the same field orientation as Hall device B (c). Finally, the active regions of both single Hall devices are merged together to form the double-Hall sensor (d).

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3 LATERAL CMOS HALL DEVICES

This chapter deals with the design and characterization of lateral Hall devices in CMOS technology. The necessary layers for designs using this technology are described in this chapter in section 3.1. Additionally, different device geometries and structures are compared. The electrical and magnetic performance of Hall devices is investigated through the two resistor model developed in section 2.2. Furthermore, offset reduction methods based on the continuous spinning current method and by use of a double-Hall sensor are investigated. The investigations take into account mechanical stress and temperature effects.

3.1 Design Considerations

CMOS Technology

The technology used for the implementation of the lateral Hall devices reported in this thesis are the 0.8 µm CMOS processes CYE and CXE offered by Austria Mikro Systeme International AG, Austria. The starting material of the above processes are four inch <100> p-type silicon wafers. Fig. 3.1 shows a cross section of a CMOS inverter together with a poly-poly capacitor realized in CYE or CXE process technology.

Although, material properties determine the performance of Hall devices presented here, the operating principle of the sensor applies to all standard CMOS processes [1 to 4]. These processes provide at least the following layers: a transistor n-well, n- and p-diffusions for source-/drain-contacts, a gate oxide layer, and metallization. The transistor n-well will serve as the conducting channel of the Hall device, i.e., the active region. The active region is contacted by n^+-source-/drain-diffusions and covered either by a p^+-source-/drain-diffusion or a polysilicon layer. Metallization and various dielectric layers are used for electrical interconnection. The design and manufacture of lateral Hall devices depend only on the process steps provided by the CMOS technology. Therefore, no addi-

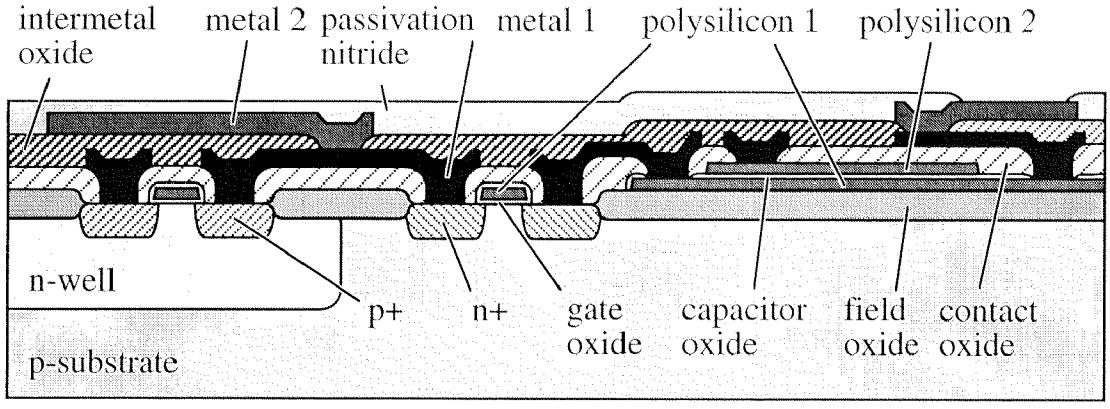


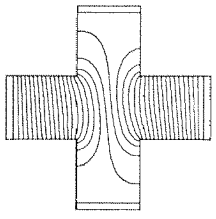
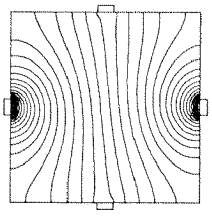
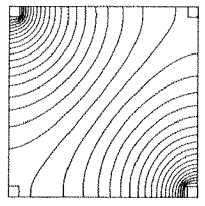
Fig. 3.1: Cross section of a CMOS inverter and a poly-poly capacitor in CYE or CXE technology.

tional post-processing is necessary, as it can be in other sensor structures based on a CMOS process. Furthermore, fabrication of Hall devices in an industrial CMOS process provides many reliability aspects such as long term stability of the sensor.

Geometry

The physical layout of the Hall device determines its performance in terms of the input resistance R (see Eq. (2.21)), sensitivity S_a (see Eq. (2.20)), and linearity of the magnetic response. For practical applications, the Hall device consists of a plate-like active region of homogeneous conductivity, and four contacts positioned near the boundary of the plate. The contacts are divided in pairs for biasing and another for sensing the output voltage. Thereby, the two sense contacts are placed in a way where approximately equal potential at zero magnetic field is attained. The corresponding common mode voltage should equal half of the voltage drop over the input resistance. As a result, and in terms of the spinning current offset reduction method, a symmetrical shape with a two fold symmetry realized with the homogeneously doped transistor n-well is recommended.

Concerning the galvanomagnetic properties, all singly-connected Hall plate shapes are equivalent and described by their geometrical correction factors [5 to 7]. However, design constrains of the CMOS process propose certain geometries which are better suited when manufactured in this technology [1 to 4].

	Greek Cross (GK)	*Square A*	*Square B*
Layout Area Consumption $64 \cdot 64\ \mu m^2$			
Input Resistance R^i/R^{GK}	1.00	0.835 sim. 0.849 calc. 0.627 meas.	1.141 1.143 1.070
Sensitivity $S_a{}^i/S_a{}^{GK}$	1.00	0.952 0.957 0.832	1.021 1.022 0.992

Tab. 3.1: Comparison of the input resistance R and the sensitivity S_a of symmetrical Hall plate geometries scaled by the figures of a Greek cross (GK).

An overview of possible symmetric Hall plate geometries is given Tab. 3.1. The simulated, calculated, and measured input resistance R and sensitivity S_a is compared. The corresponding measurement setup, which will be additionally used for the following measurements of the same properties, is shown in Fig. 3.2. Good agreement is achieved between simulation and calculation (see Tab. 3.1). The dis-

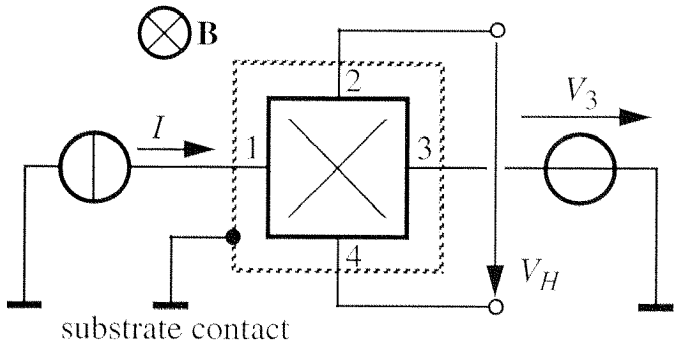


Fig. 3.2: Setup to measure the input resistance R and the sensitivity S_a of a Hall device in this work.

crepancy with the measurement result is due to the junction field effect not considered in the theoretical studies.The results do not propose a particular shape for the above geometries. However, the Greek Cross arrangement with highest sensitivity and considerable input resistance is used in the following designs. The active region and the electrical contacts are fabricated with two different layers of the CMOS process. These layers may have a mismatch resulting in a perturbation of the potential distribution in the active region. Combined with non-linear effects (see section 2.2) this causes offset voltages which can not be cancelled dynamically. Mismatch of different layers has the least impact for the Greek Cross arrangement since voltage gradients in the surrounding area of the contacts are the lowest [8].

Another important design aspect is the cover layer of the active region. The CMOS fabrication process allows two possibilities, these are: a polysilicon gate oxide, or a p^+-diffusion cover layer (see Fig. 3.3). The polysilicon layer serves as an electrical shield and improves EMC. The p^+-diffusion layer also serves as an electrical shield, but reduces the thickness of the active region. As a result, a higher input resistance R and a higher sensitivity S_a is achieved at the expense of

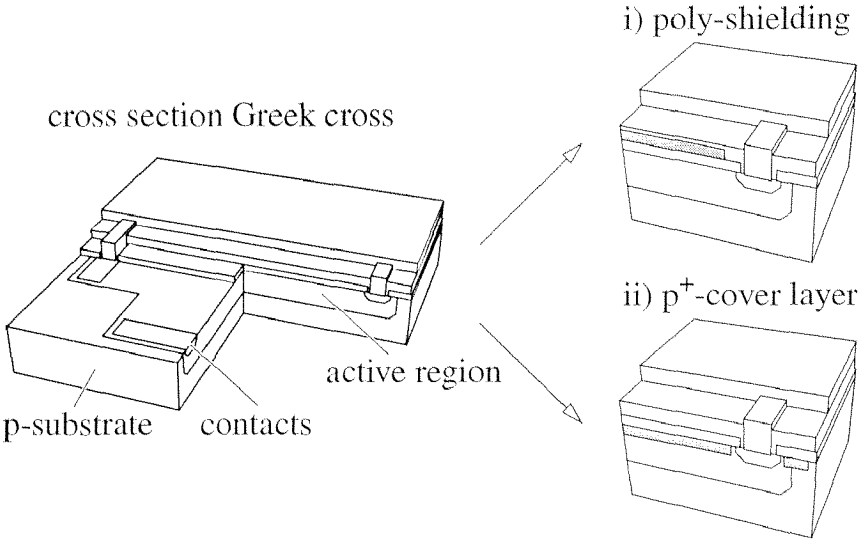


Fig. 3.3: Different cover layers for a Hall device shaped as a Greek cross. The CMOS fabrication process suggest either a polysilicon gate oxide, or a p^+-diffusion layer.

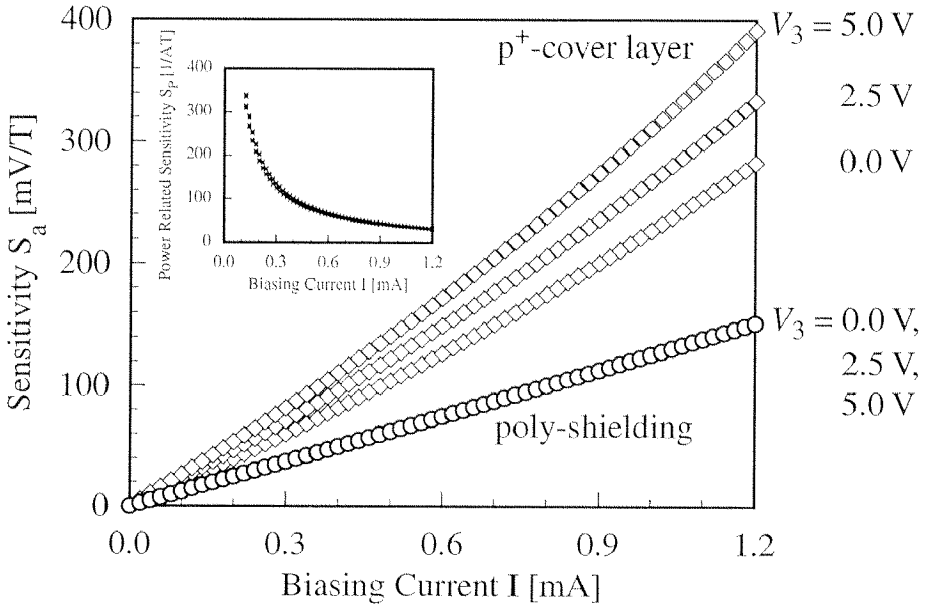


Fig. 3.4: Measured sensitivity S_a of Hall devices shaped as Greek Cross for different cover layers and biasing conditions. Additionally, the inset shows the corresponding power related sensitivity plotted for all conditions in the same graph.

a more non-linear behavior. Measurement results on different layout possibilities are shown in Fig. 3.4. A p^+-diffusion cover layer results in more non-linear dependence of the sensitivity on the biasing current than with poly-shielding. Additionally, a large influence on the voltage difference between the active region and the substrate can be observed due to the JFET effect [9]. However, in terms of the power related sensitivity $S_p = S_a/I^2R$ no improvement in the performance is achieved (see inset of Fig. 3.4).

In summary, a Greek cross shape is the most suited, to design a Hall device fabricated in a CMOS process. Combining high sensitivity and low input resistance, the layout is least dependent on fabrication non-idealities, such as layer mismatch. In order to cover the active region, a polysilicon gate oxide is recommended. The gate oxide allows shielding of electric fields with low influence on the linearity of the device performance. However, to study non-linear effects a p^+-diffusion layer was used.

3.2 Electrical and Magnetic Performance

Linearity of the Magnetic Response

In addition to offset voltages, the absolute accuracy of Hall devices is determined by the linearity. According to [10] the non-linearity is defined as the deviation of a set of measured Hall voltages from a corresponding linear fit. The dimensionless non-linearity is classified in two groups: a material non-linearity and a geometrical non-linearity [10]. The material non-linearity is caused by the dependence of the Hall scattering factor on the Hall angle (see Eq. 2.18). Assuming G_S/t as a constant value (see Eq. 2.20), the material non-linearity is given by

$$NL_M \cong -\gamma \mu_{Hn}^2 B^2, \tag{3.1}$$

where γ is the material non-linearity coefficient [10]. With $\alpha = 0.35$ [10] and the Hall angle $\mu_{Hn}B < 0.01$, values of NL_M are in the range of < 50 ppm. On the other hand, non-linearity is also caused by the dependence of the geometry factor

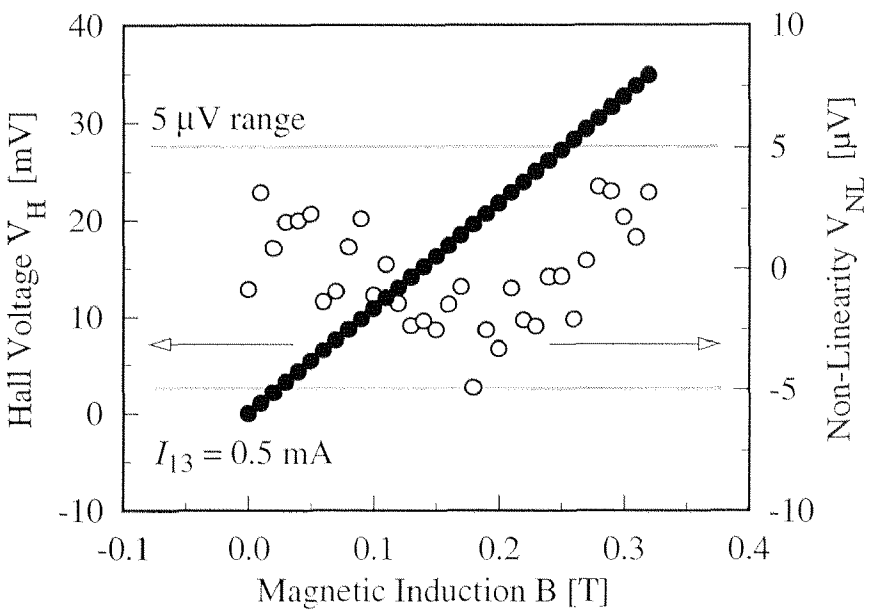


Fig. 3.5: Linearity measurement of four contact Hall device shaped as Greek cross with p^+-cover. With a biasing current of $I_B = 0.5$ mA the linearity error is below 5 µV which corresponds to 150 ppm in a ±0.3 T range.

on the magnetic induction, i.e. the geometrical non-linearity (see Tab. 2.2). Assuming R_{Hn}/t is a constant value (see Eq. 2.20), the geometrical non-linearity results in

$$NL_G \cong -\beta\mu_{Hn}^2 B^2 , \tag{3.2}$$

where β is a numerical coefficient [10]. With a Greek cross arrangement of the Hall devices with $h/k = 1$ values of $\beta < 0.02$ are expected [10]. Consequently, the geometrical non-linearity is in the order of 5 ppm. The measured non-linearity of a Hall device shaped as a Greek cross with $h/k = 1$ is shown in Fig. 3.5. At a biasing current of 0.5 mA the deviation from a linear fit is below 5 µV, which corresponds to a full scale non-linearity of 150 ppm for field strengths up to 0.3 mT.

Variation of Device Geometry

The electrical and magnetic performance of Greek cross Hall devices is investigated in terms of a variation of the aspect ratio h/k and the absolute size h. The aspect ratio ranged from 0.5 (10 µm/20 µm) to 1.5 (30 µm/20 µm), whereas the

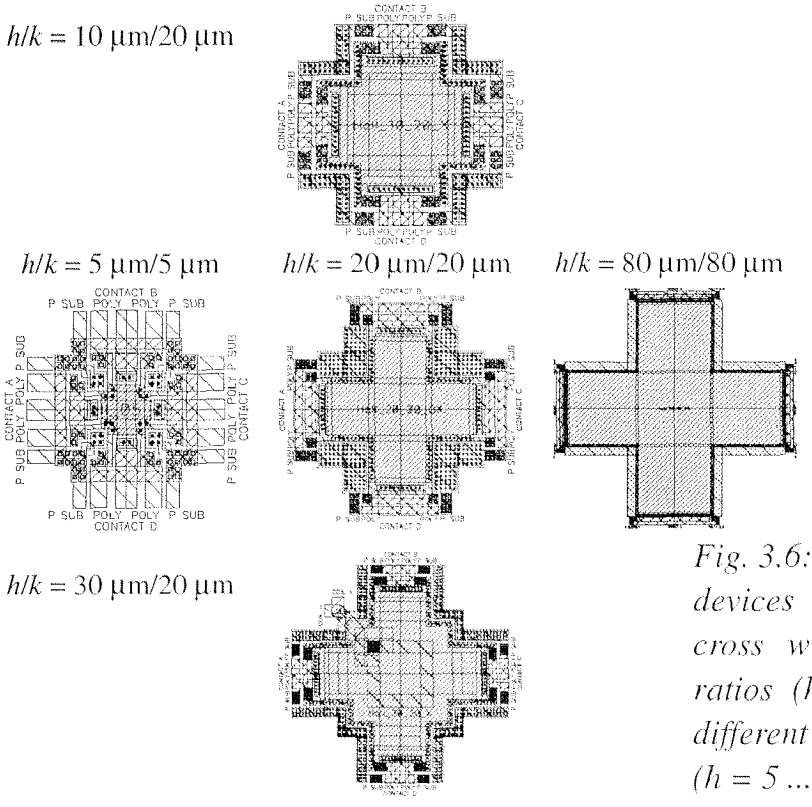


Fig. 3.6: Layout of Hall devices shaped as a Greek cross with different aspect ratios ($h/k = 0.5 \ldots 1.5$) and different absolute sizes ($h = 5 \ldots 80$ µm).

absolute size varied from 5 µm to 80 µm at $h/k = 1$ (see Fig. 3.6). The biasing conditions for the current I changed from 0 to 2 mA with a change in substrate voltage V_3 from 0 to 5 V (see Fig. 3.2).

The analytical model derived in section 2.2 allows an approximate calculation of the input resistance and the sensitivity of a Hall device of arbitrary shape. In a first step the Hall device with its Greek cross shape is transformed into a rectangular device by conformal mapping. In the next step, the model of the junction field effect is applied. In order to compare the measurement results with the model, the doping profiles have to be known. These profiles were derived from fabrication process modeling [11] (see Fig. 3.7). However, doping profiles and the corresponding sheet resistances have large variations, in the order of 40%, due to fabrication constraints. Therefore, only fair agreement between measurement and simulation results can be expected.

With doping profiles as presented in Fig. 3.7 and their extracted parameters (see Tab. 3.2) the input resistance and the sensitivity of a Greek cross Hall device with an aspect ratio of $h/k = 20$ µm/20 µm was calculated and compared with mea-

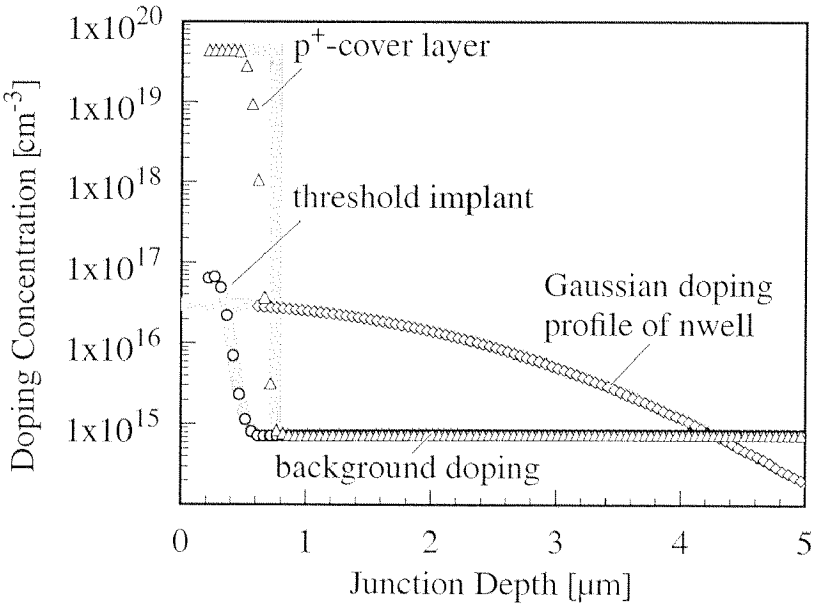


Fig. 3.7: Doping profiles derived from fabrication process simulations [11]. The active region is defined to be the Gaussian doping profile of the transistor nwell. The p^+ layer is used as cover of the nwell.

surement data. Two additional parameters must be introduced: the reduction value RF_{nwell} and RF_{nplus}. They describe the mean deviation of a designed length from the actual physical value.

Quantity	*Value*	*Quantity*	*Value*
ϕ	$1.21 \cdot 10^{13}$ cm^{-2}	p_p	$4.4 \cdot 10^{19}$ cm^{-3}
ΔR_p	1.51 µm	t_p	0.75 µm
R_p	0.21 µm	RF_{nwell}	-0.85 µm
t_m	0.15 µm	RF_{nplus}	0.11 µm
p_0	$7.6 \cdot 10^{14}$ cm^{-3}	λ	1

Tab. 3.2: Parameters extracted from the doping profiles of Fig. 3.7 (see also Eqs. (2.21 to 2.53)).

The input resistance expressed by the input voltage drop, and the sensitivity were compared with the possible range for these results determined by minimum and maximum sheet resistance values achieved from the process specification (see Fig. 3.8). Good agreement is achieved for the sensitivity, whereas the input resistance is predicted to be too low. However, the deviation is much smaller than the possible range due to process variations.

Measurements and simulations of the input voltage drop ΔV_{24} and the sensitivity S_a for different absolute sizes h are shown in Figs. 3.9 and 3.10. For smaller feature sizes of the Hall device, a more non-linear behavior can be observed, but, the sensitivity improves only moderately. An explanation for this can be found in the junction field effect. Relative changes of the device geometry, due to the bias dependent insulating junction, increase for smaller devices. Thus, simulations show excellent agreement with measured values within the accuracy of the parameters of the doping profiles used as boundary values. Plotting the sensitivity S_a against the device size for different voltage drops ΔV_{24}, recommends a length h between 10 µm and 20 µm (see Fig. 3.11). A drop in performance is observed, for length h smaller than 10 µm.

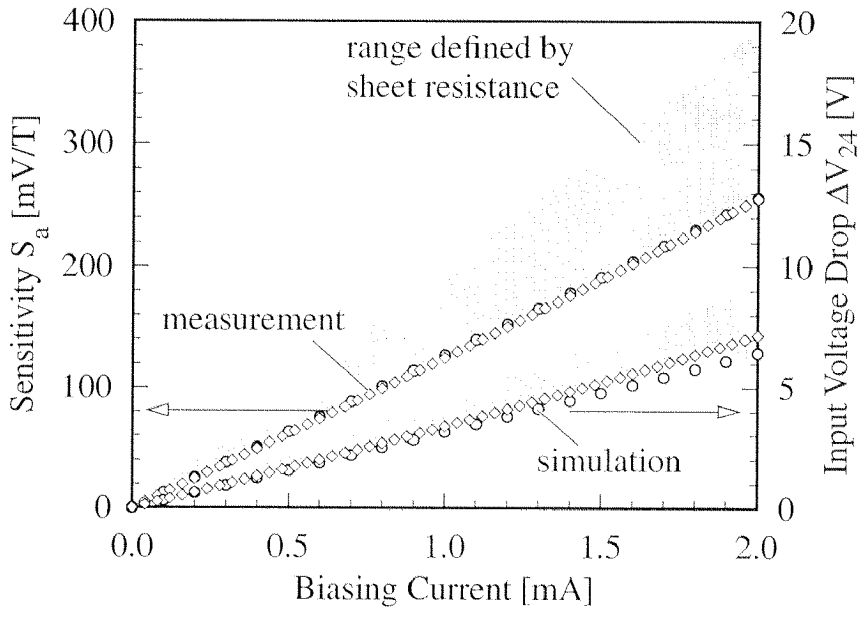


Fig. 3.8: Calculated input voltage drop and sensitivity of a Greek cross Hall device with h/k = 20 µm/20 µm compared with measurement results. The values are shown within their possible range determined by minimum and maximum sheet resistances of the doped areas.

Changing the aspect ratio h/k of a Greek cross Hall device towards smaller values reduces the input voltage drop (see Fig. 3.12). At the same time, the relative change in sensitivity is not as large (see Fig. 3.13). However, according to [10], the geometrical non-linearity of a Greek cross is defined as

$$\beta \cong \frac{\exp[-\pi h/k]}{2.871 - 3\exp[-\pi h/k]}, \tag{3.3}$$

which limits the aspect ratio to a range of $h/k = 0.5$ .... 1.0 to maintain reasonable linearity of the device. Again, the sensitivity S_a is plotted against the aspect ratio for different voltage drops ΔV_{24} (see Fig. 3.14).

As a conclusion, the geometry of a Hall device has to be optimized in terms of high sensitivity for a certain biasing voltage, low non-linearity, and minimal influence of the bias dependent insulating junction. Therefore, aspect ratios of $h/k = 0.5$ ... 1.0 and absolute sizes of $h = 10$ µm ... 20 µm are recommended for a Hall device shaped as Greek cross.

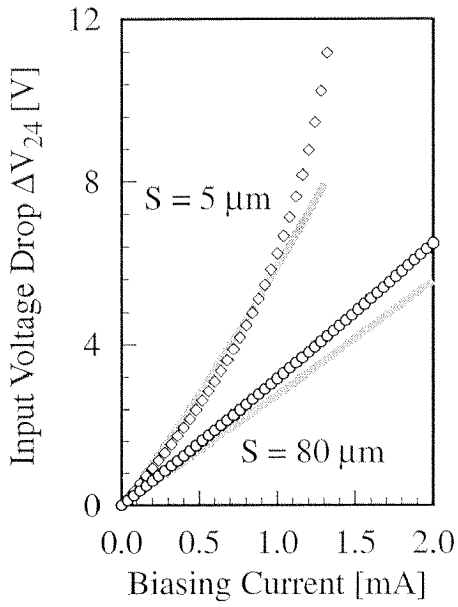


Fig. 3.9: Voltage Drop ΔV_{24} of different absolute sizes S of a Greek Cross Hall device (simulation: grey line).

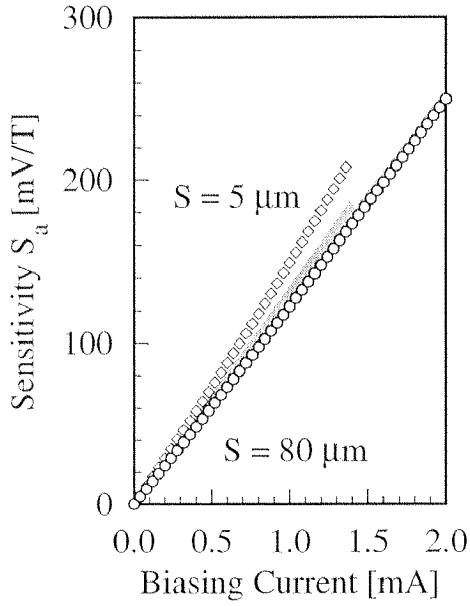


Fig. 3.10: Sensitivity S_a for different absolute sizes S. Only a small influence can be observed.

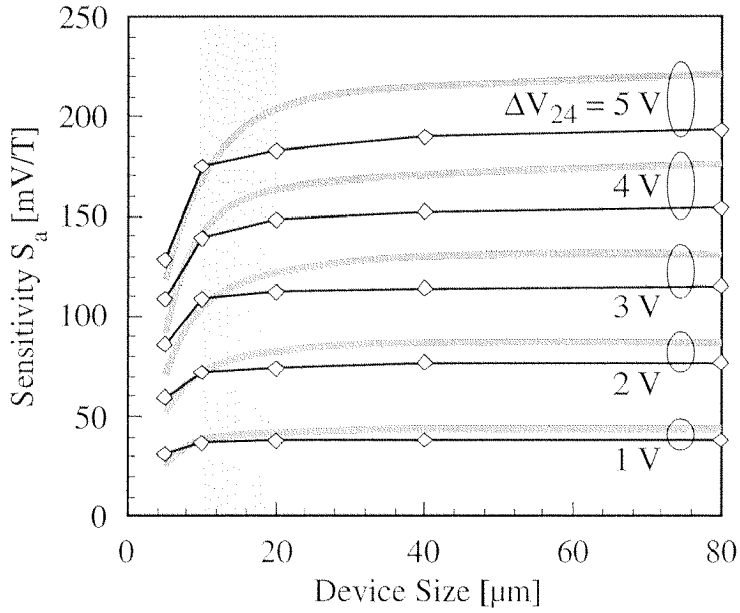


Fig. 3.11: Sensitivity S_a as a function of the device size for different values of the voltage drop ΔV_{24}. The deviation between measurement results and simulation is due to a voltage drop which is predicted too low. A range of h = 10 ... 20 µm is recommended for a Greek cross Hall device.

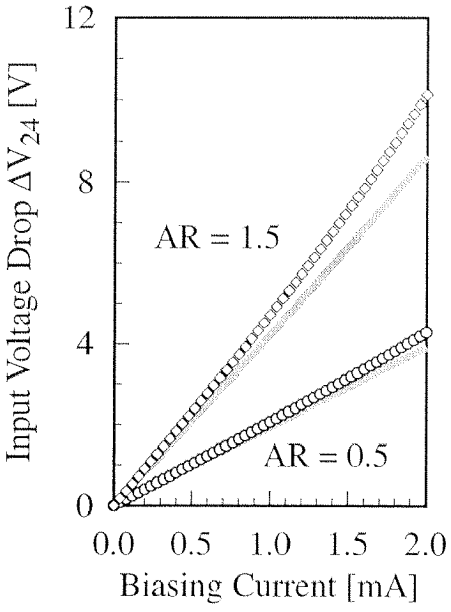


Fig. 3.12: Voltage Drop ΔV_{24} of different aspect ratios of a Greek Cross Hall device (simulation: grey line).

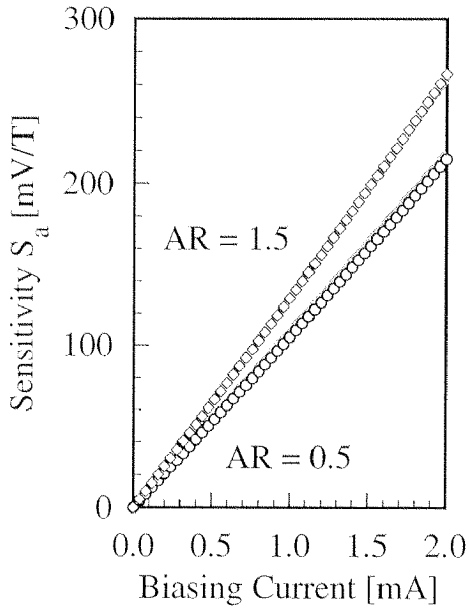


Fig. 3.13: Sensitivity S_a for different aspect ratios. Excellent agreement of simulation and experiment is shown.

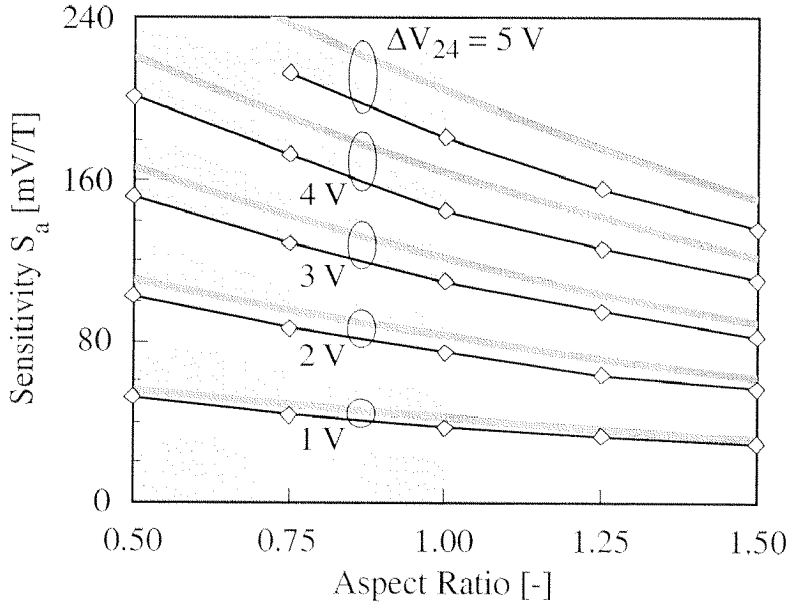


Fig. 3.14: Sensitivity S_a as a function of the aspect ratio for different values of the voltage drop ΔV_{24}. Due to linearity considerations range of h/k = 0.5 ... 1.0 µm is recommended for a Greek cross Hall device.

3.3 Implementation of Offset Reduction by Continuous Spinning Current

Basic Measurements

The continuous spinning current method is demonstrated with a CMOS Hall device, shaped as a Greek cross, that is sensitive to magnetic fields perpendicular to the chip plane [8]. The method is based on four contact Hall devices arranged in contact pairs (13) and (24), as shown in Fig. 3.15. The specific active region of the device consists of a weakly-doped n-well resistor of a CMOS process and is fabricated in a p-substrate. The active region has a ratio h/k of 33 µm/22 µm (see section 2.2). A shallow p^+ diffusion, covering the active region and contacted to the substrate, reduces the thickness of the conductive layer and thus increases its sensitivity.

Insulation between the active region and the p-substrate occurs due to a reverse biased pn-junction. The biasing current causes an electrical potential difference between the contacts and the substrate, which changes with the distance from the

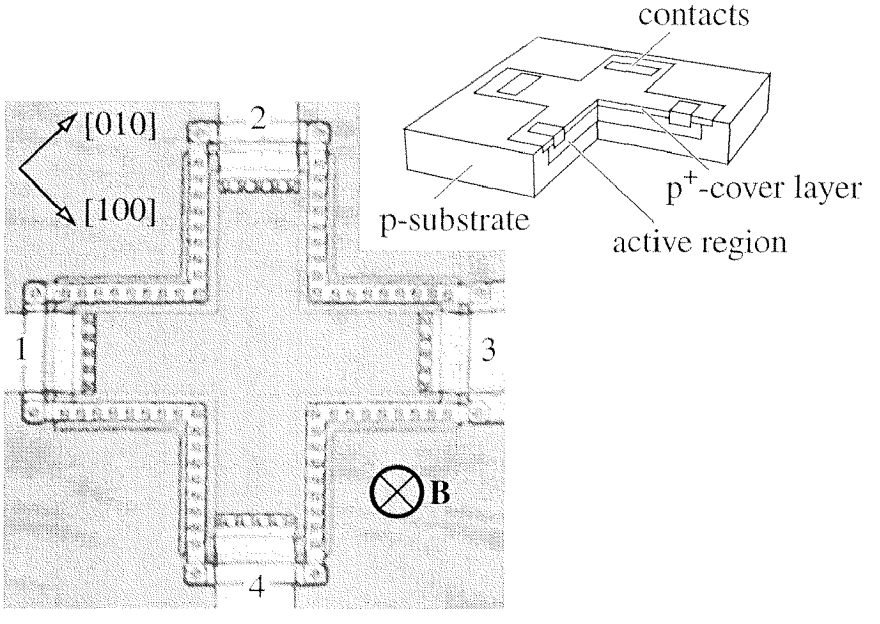


Fig. 3.15: A four contact CMOS Hall device consisting of an n-well resistor as an active region fabricated in a (100)-p-substrate. The orientation of the Greek cross shaped device is in [110]-direction. Additionally, the active region is covered with a shallow p^+ diffusion.

contacts. This change causes a variation in the depletion layer width and, consequently, a variation in the thickness of the Hall plate [9, 12]. Therefore, the thickness of the active region is modulated by the harmonic biasing currents I_{13} and I_{24} (see Eqs. (2.66) and (2.67)). In a measurement setup as shown in Fig.3.16 the voltage V_3 is kept constant. As a result, the Hall plate, with its non-linear resistance due to the junction field effect (see section 2.2), is biased asymmetrically with respect to the substrate voltage V_{sub}. For example, in the case of, e.g., $I_{13} = I_0$ or $I_{13} = -I_0$ the mean thickness of the active region differs (Fig. 3.16b and 3.16c). This causes an additional source of offset which is not cancelled when $V_{H,O}(B, \varphi)$ is averaged over a full switching period of φ.

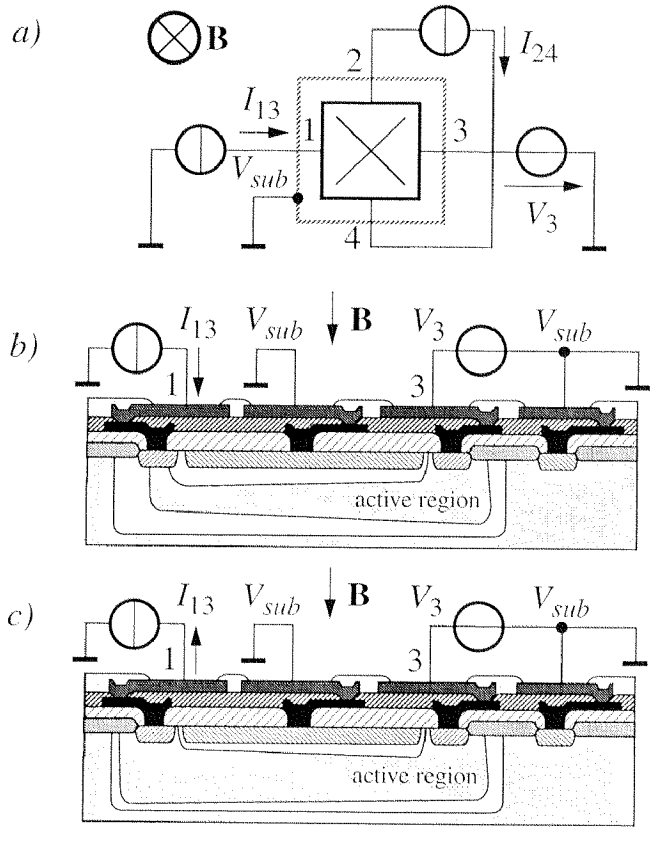


Fig. 3.16: a) Setup which causes asymmetric biasing conditions for the Hall device. The mean thickness of the active region differs in the case of, e.g., b) $I_{13} = I_0$ and c) $I_{13} = -I_0$. This causes an additional source of offset due to non-linearities which does not cancel. The layers shown in the Hall device cross section are according to Fig. 3.1.

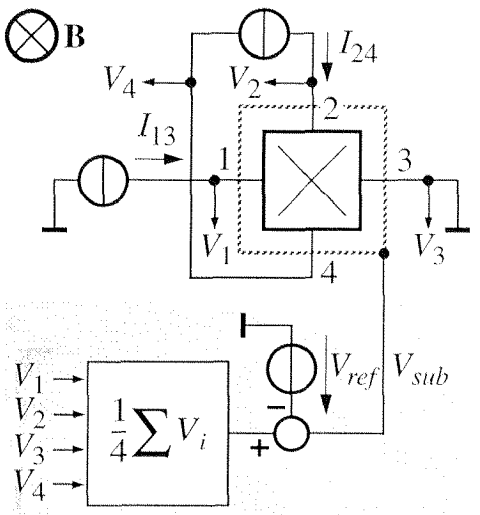


Fig. 3.17: Measurement setup with circuitry to control the substrate voltage V_{sub}, ensuring symmetric operation.

In order to overcome the measurement induced offset, the setup was modified as shown in Fig. 3.17. The control circuitry keeps the potential difference between the average value of the contact voltages V_i ($i = 1, 2, 3$, and 4) and the substrate V_{sub} at a constant value V_{ref}. As a result, the operating regime is symmetrical and

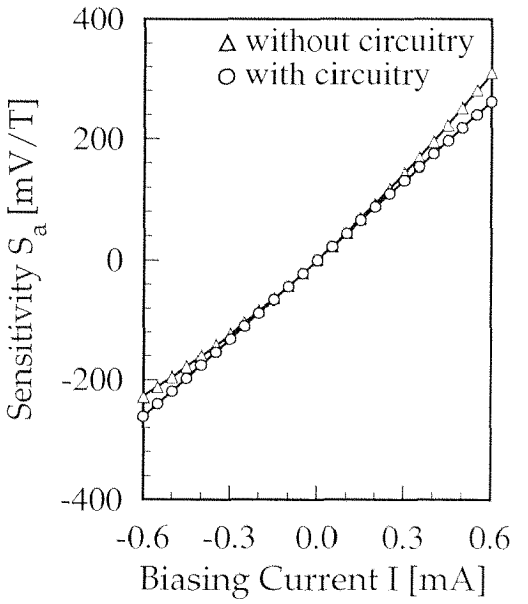


Fig. 3.18: Measurement sensitivity S_a with (○) and without (Δ) circuitry to control the substrate voltage V_{sub}.

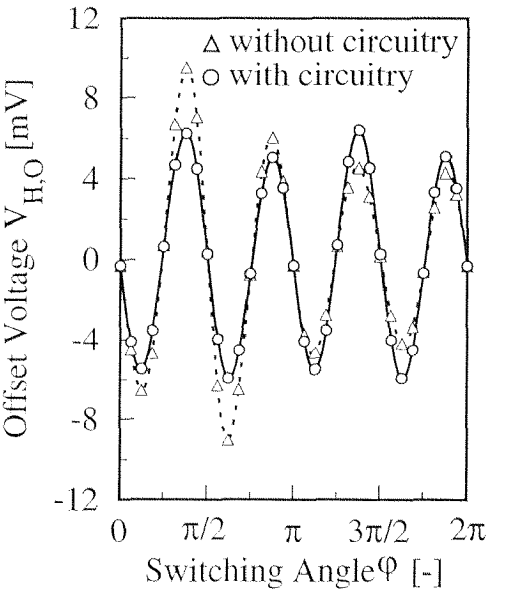


Fig. 3.19: Change of residual offset V_O due to symmetric biasing conditions with (○) and without (Δ) control circuitry.

no offset is induced by the biasing due to non-linearities. This can be shown by determining the thickness dependent sensitivity S_a of the Hall device as a function of the biasing current I_{13}. With the control setup, the non-linearity of S_a is reduced below 0.2% (see Fig. 3.18).

Using above setup the signal $V_{H,O}(B, \varphi)$ can be measured for any angle φ with only four contacts (Eqs. (2.68) and (2.69)). It allows a more detailed investigation of the offset behavior than discrete sampling as shown in [13]. However, according to theory the Fourier series of the residual offset V_O is of limited order. Therefore, only a limited number of measurements per period of the signal $V_{H,O}(B, \varphi)$ are necessary and determined to be 32 steps experimentally [14]. An example of the measured response $V_{H,O}(B, \varphi)$ is shown in Fig. 3.19. It is measured with and without control circuitry. For a biasing current of $I_0 = 0.5$ mA, the residual offsets expressed in an equivalent magnetic field below 10 µV were measured [8]. These measurements indicated that a range of ±10 µT was approximately the noise level of the sensor together with the measurement setup.

Finally, the magnetic response of 6 Hall devices operated with continuous spinning current method was measured (Fig. 3.20). In the range of ±0.3 mT, an excel-

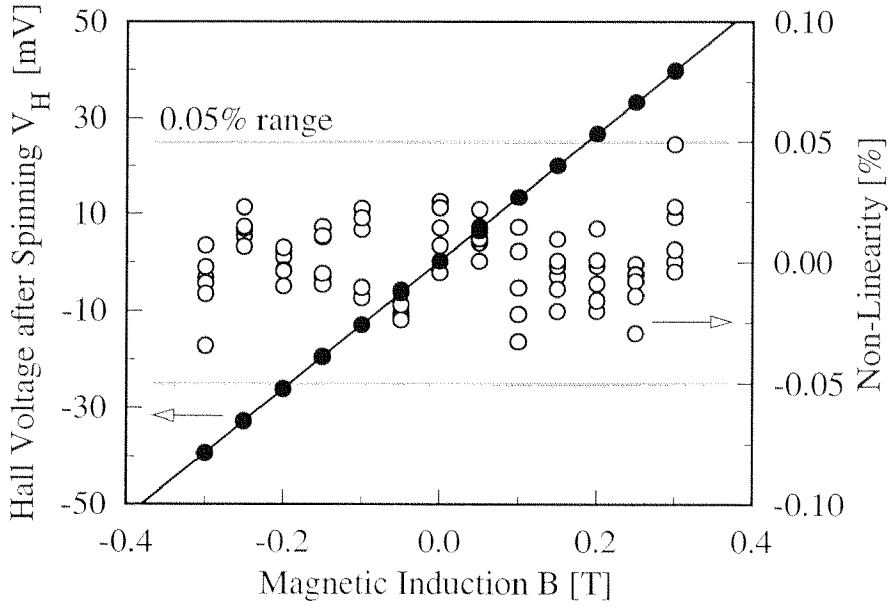


Fig. 3.20: Magnetic response of 6 Hall devices operated with the continuous spinning current method. A full scale non-linearity below 0.05% is achieved.

lent non-linearity below 0.05% is achieved. The non-linearity is caused by the sensor itself, the setup for the offset reduction, and the reference magnet. Comparing the result with the non-linearity of the bare Hall device ($NL < 0.015\%$), only a factor of 3 due to the offset reduction method is observed.

Influence of Mechanical Stress Dependence on the Offset Voltage

Hall devices suffer from a large offset voltage which degrades the performance of the sensors. Although the offset voltage is caused by a wide variety of effects, such as fabrication processes and environmental properties, the main contribution is caused by mechanical stress to which the device is subjected [16]. Sources of mechanical stress are introduced by the packaging process and during fabrication due to intrinsic stress caused by overlying dielectric and conducting thin films [15, 17]. Furthermore, the stress distribution changes over the life-time of the device. Therefore, stress effects cannot be cancelled by initial factory trimming and affect the long-term stability of the device. However, cancelling the offset voltage dynamically with the switched or continues spinning current method limits the frequency response due to the discrete sampling [18]. Therefore, a detailed knowledge of the stress dependence of the offset components in terms of their spatial Fourier expansion is essential to choose the minimum sampling frequency to cancel all stress contributions. Furthermore, a precise understanding of the stress induced offset voltage may suggest preferred orientations of the Hall sensor with respect to the crystal orientation for minimal initial offset. The validness of the theory developed in section 2.3 is verified by measurements using the continuous spinning current method [8] and a four point bending bridge that applies a well-defined mechanical stress on the device [15]. However, the investigation focuses on the angular frequency and the phase angle of the offset voltage components rather than absolute amplitudes, which would require a large, statistically relevant number of samples.

In a four-point bending calibration experiment, a Hall sensor is placed in a state of well-defined stress and the resultant voltages, according the continuous spinning current method, are measured. A schematic illustration of the experimental setup is shown in Fig. 3.21. The Hall device die is bonded on a steel bar by epoxy glue. To achieve high reproducibility and an uniform interface between the steel

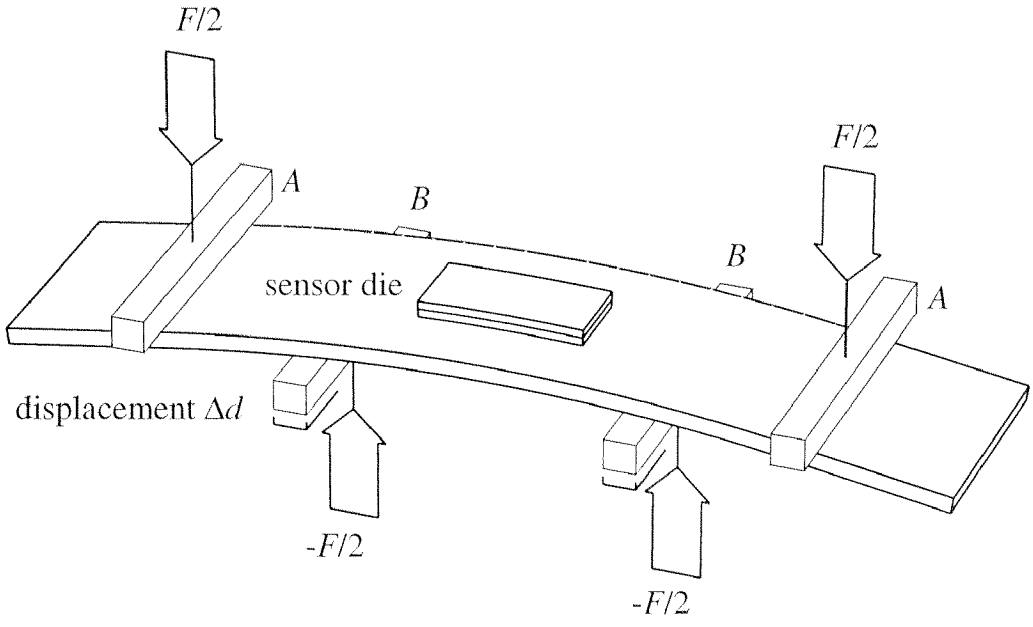


Fig. 3.21: Four-point bending bridge with a steel bar under load. The sensor die is attached in the center of the bar and the supports to apply a force arranged symmetrically.

bar and the die, the bonding process was completed on a commercial die bonder, offered by *ESEC S.A.*, Switzerland. The steel bar is supported by two knife edges at locations *A*, spaced by a known distance. A force couple is applied to the steel bar at positions *B*, where the supports to introduce the forces on the bar are aligned with the center of the Hall sensor die. Accordingly, the steel bar and sensor die freely deform under the force load and a mechanical stress is introduced defined by the displacement Δd, the geometry of the four-point bending setup and the mechanical properties of the sample under investigation.

The common application of the four-point bending calibration requires a silicon strip with an integrated Hall sensor to analytically calculate the stress distribution in the die [15]. However, the approach with a sensor die bonded on a steel bar gives more realistic conditions of the stress distribution in devices conventionally packaged, e. g., by incorporating a lead frame and plastic molding [19]. The mechanical stress distribution in the sensor die as a function of the displacement Δd, is calculated using finite element modeling. The stress components are calculated in the coordinate system of the sensor die, which is aligned with the Greek cross shaped active region (see section 2.3). The main contribution of mechanical

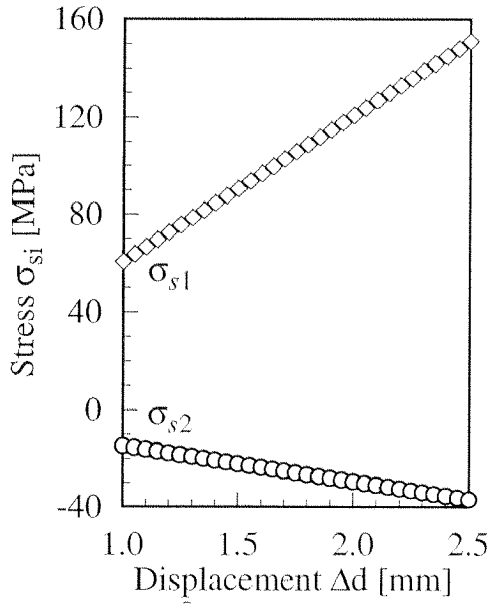


Fig. 3.22: Calculated axial stresses in the sensor die as a function of the displacement of the four-point bending bridge determined by finite element modeling.

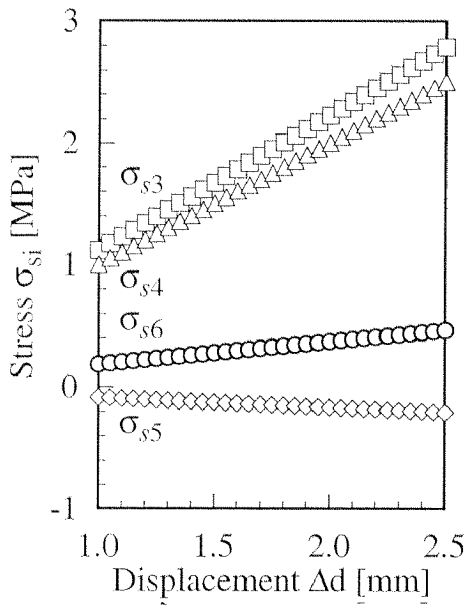


Fig. 3.23: Calculated off-plane axial stress and shear stresses introduced in the sensor die as a function of displacement.

stress originates from the in-plane axial components σ_{s1} and σ_{s2} (see Fig. 3.22). The stress component σ_{s3}, perpendicular to the die surface, and the shear stresses σ_{s6}, σ_{s4} and σ_{s5} are of minor importance with a contribution in the range of 1% of σ_{s1} (see Fig. 3.23). However, the resulting stress tensor is a linear combination of its non-zero components. Therefore, the following measurement results will be discussed in terms of the displacement Δd of the four-point bending bridge rather than by the absolute values of the mechanical stress.

First, the mechanical stress dependence is discussed considering the spatial dependence in the switching angle φ of the periodic offset voltage $V_{H,O}$ (see Eq. (2.68)) and the periodic resistive voltage $V_{R,O}$ (see Eq. (2.69))

$$V_{H,O} = V_{24}(\boldsymbol{B}, \varphi)\cos(\varphi) - V_{13}(\boldsymbol{B}, \varphi)\sin(\varphi) = \sum_n A_n \sin(n\varphi + \lambda_n), \quad (3.4)$$

$$V_{R,O} = V_{24}(\boldsymbol{B}, \varphi)\sin(\varphi) + V_{13}(\boldsymbol{B}, \varphi)\cos(\varphi) = \sum_n B_n \sin(n\varphi + \upsilon_n). \quad (3.5)$$

The initial condition at a deflection Δd = 1mm is shown in Fig. 3.24. As expected from theory, offset and resistive voltage have similar amplitudes with different phase angles (see Eqs. (3.4) and (3.5)). The periodic offset voltage exhibits zero transitions for phase angles approximately along the symmetry axes of the device contacts, i.e., at $\varphi = 0, \pi/2, \pi, 3\pi/2, 2\pi$. In contrast, zero transitions for the resistive voltage can be observed at angles φ phase shifted by $\pi/4$ at, i.e., $\varphi = \pi/4, 3\pi/4, 5\pi/4, 7\pi/4$, resulting from the orthogonal nature of the above voltages. The angular dependence was measured in 32 discrete steps of the switching angle φ. As a result, the periodic voltages can be represented by a Fourier series (see Eqs. (3.4) and (3.5)) allowing to discuss sources of offset in terms of voltages of different periodic orders in the switching angle φ. Calculated components A_n and B_n of the Fourier series for $V_{H,O}$ and $V_{R,O}$, respectively, are shown in Fig. 3.25. The Fourier series is dominated by components in the second and fourth order in the switching angle φ, appearing with same amplitude for

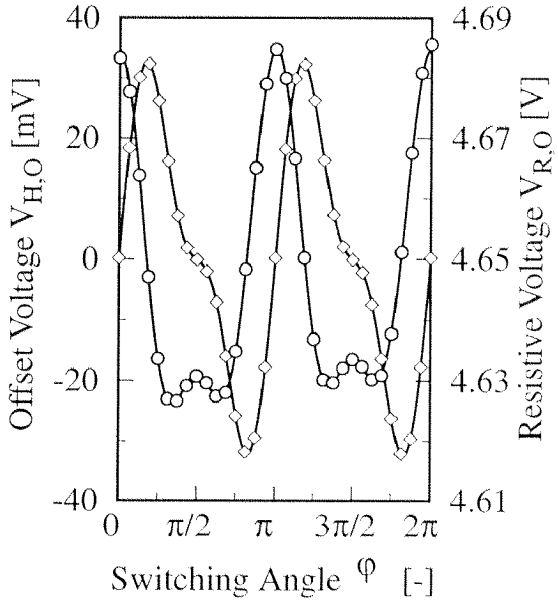


Fig. 3.24: Spatial representation of the offset voltage $V_{H,O}$ and the resistive voltage $V_{R,O}$ measured in 32 steps of the switching angle φ. The resistive voltage exhibits a phase shift of $\pi/4$ with respect to the offset voltage

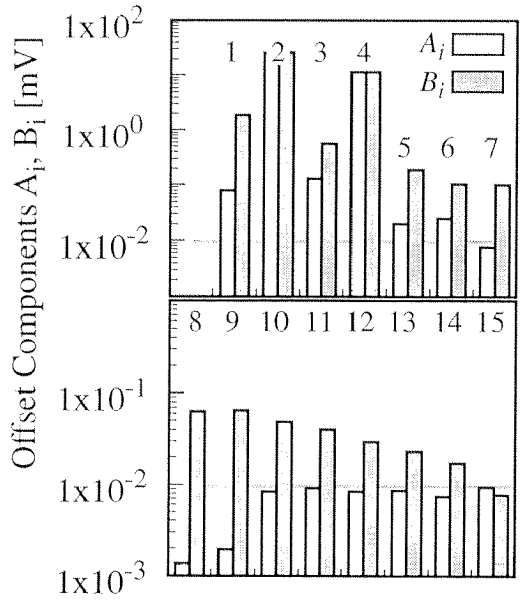


Fig. 3.25: Spatial spectrum of the offset voltage $V_{H,O}$ and the resistive voltage $V_{R,O}$ up to the fifteenth order. The main contribution to the spectrum can be observed in the second and fourth Fourier orders.

offset and resistive voltage, i. e., $A_2 = B_2$ and $A_4 = B_4$. Furthermore, contribution of components in the first, third, fifth and sixth orders can be observed which will be discussed later. However, components of the seventh order and higher have only a minor impact on the Fourier series with values below 10 µV.

i). Zero order contribution

The zero order contribution of the Fourier series A_0, also called the residual offset, determines the performance of the offset reduction method since one can not distinguish between the offset voltage and the Hall voltage. Nevertheless, in the case of the spinning current method, the contribution is several orders smaller than for the uncompensated case resulting in values of a few microvolts [20]. In the example shown in Fig. 3.24, the number of samples taken allows the cancellation of Fourier components up to the fifteenth order. However, a small dependence on mechanical stress can still be observed, possibly resulting from non-linear effects caused by the junction field effect (see Fig. 3.26 and section 2.3). However, the change in the residual offset voltage, over a wide range of mechanical stress values, is below the noise level of the appropriate front-end circuitry used to perform the spinning current system configuration [21].

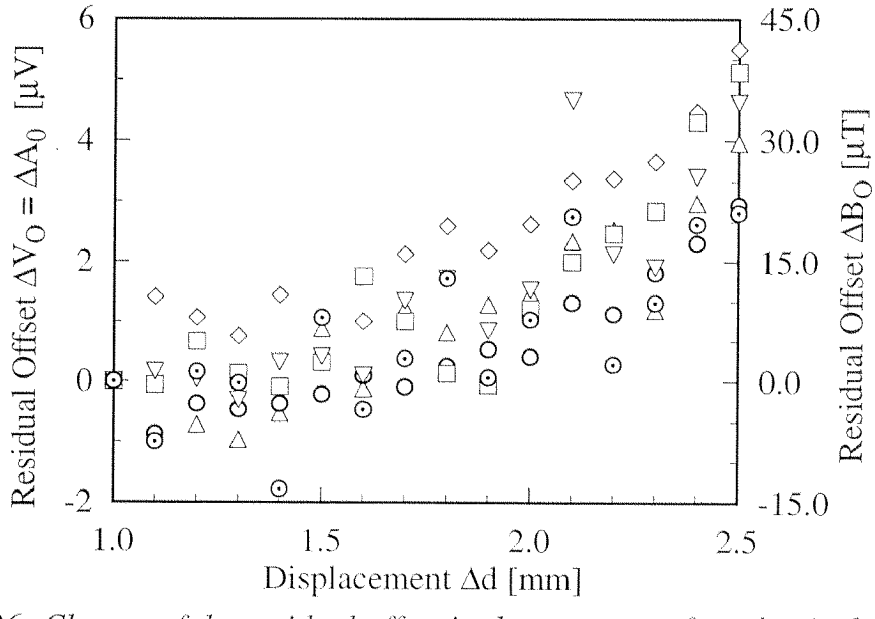


Fig. 3.26: Change of the residual offset in the presence of mechanical stress for six test samples. The number of samples taken per period allows the cancellation of Fourier components up to the fifteenth order.

ii). First and third order contributions

Although the spinning current Hall sensor under test cancels offset voltages, in odd harmonics of the switching angle φ, due to device symmetry (see section 2.3), an investigation is necessary to confirm the theoretical prediction of their occurrence. According to Eq. (2.78) and the subsequent numerical calculations, odd harmonic offset voltages are due to junction thickness modulation with only a minor stress dependence of offset amplitude. Furthermore, the phase shift, which is given by device layout shows no stress dependence (see Fig. 3.27 and 3.28). Since the first and third harmonic offset voltages have the same origin, their stress dependence has to be of similar order, but, not necessarily of same phase angle λ_n.

iii). Second order contribution

The main contribution to the offset voltage is of the second harmonic order in the switching angle φ caused by piezoresistive effects, as already reported in literature [16] (see Fig. 3.29). According to theory (see Eq. (2.76)) and numerical simulation the stress dependence suggests the orientation of the CMOS Hall device.

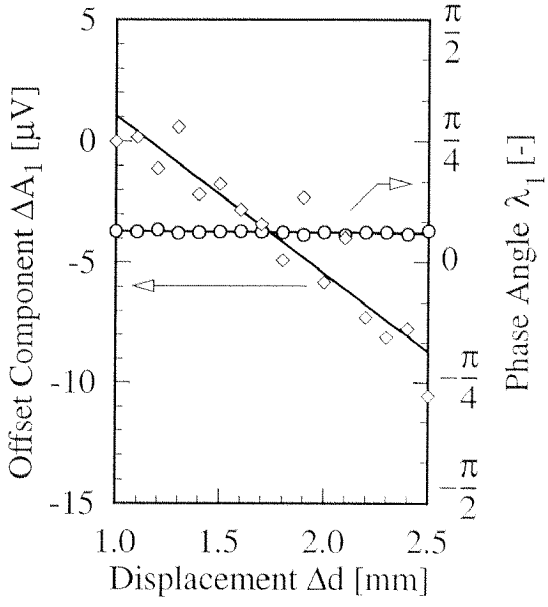


Fig. 3.27: Stress dependence of the offset component of the first order in the switching angle φ. The phase angle is given by the device layout and shows no stress dependence.

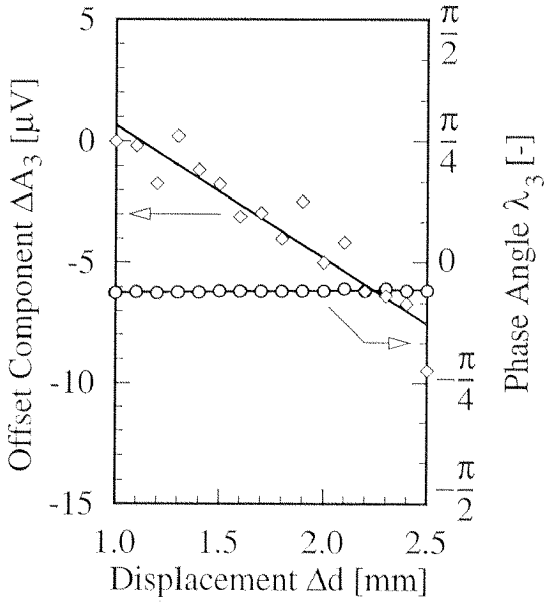


Fig. 3.28: Stress dependence of the third order offset components. The behavior is similar to offset voltages occurring in the first order.

For predominant axial stresses, an orientation in the [110] direction with respect to the device contacts is recommended. However, comparing experimental results with theoretical values of the piezoresistive coefficients [22] and the simulated mechanical stresses (see Figs. 3.22, 3.23), the offset component ΔA_2 and the phase angle λ_2 are predicted four times too small. The discrepancy is difficult to predict because the assumed piezoresistive coefficients depend on the fabrication process. Furthermore, numerical stress simulation gives only an indication of the mechanical stress properties in a packaged device.

iv). Fourth order contribution

Offset voltages of the fourth harmonic order in the switching angle φ result from junction thickness modulation. For symmetric biasing conditions, i.e., when the biasing current flow agrees with the symmetry axes of the active region thickness distribution in two dimensions, no offset voltages are generated. This is the case for the conventional switched spinning current method. In the case of continuous spinning current, biasing currents in directions off-axis with geometrical symmetries of the device result in asymmetric junction thickness distributions. Offset voltages unique for this operating scheme are possible.

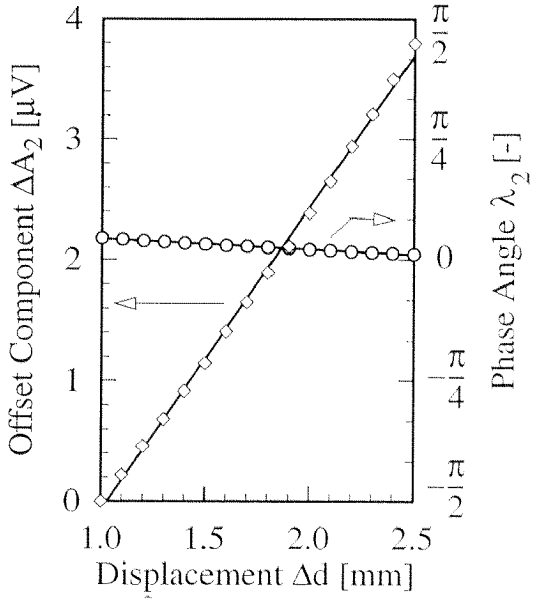


Fig. 3.29: Stress dependence of the second order offset ΔA_2 and phase λ_2. The non-zero phase angle is due to the applied shear stress σ_{s6}.

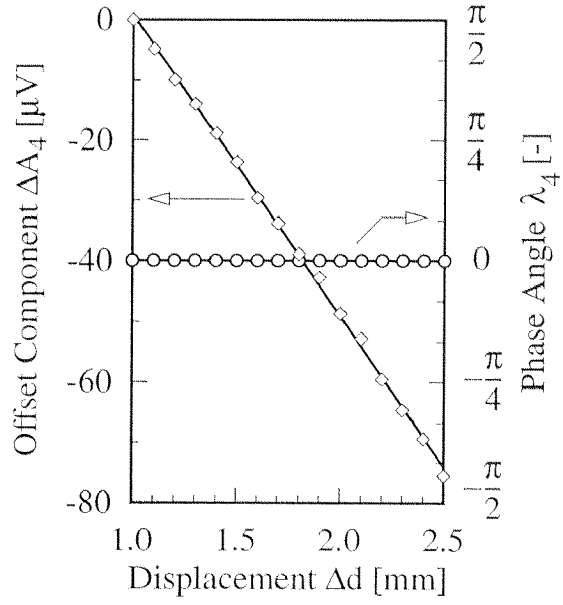


Fig. 3.30: Stress dependence of the fourth order offset components ΔA_4. As predicted by theory, $\lambda_4 = 0$ exhibits no shift over the displacement Δd.

The mechanical stress dependence on the fourth order effects is mainly due to a change of resistivity of the active region, i.e., a change of the biasing conditions of the isolating junction (see Fig. 3.30). On the other hand, the phase angle λ_4 is given by device layout. Consequently, theoretical predictions suggest an angle $\lambda_4 = 0$ independent of stress, according to definitions of switching angles based on Fig. 3.30. Although fourth order offset voltages, in the switching angle φ, are unique to the continuous spinning current method, the periodic offset voltage acts as a source for aliasing products of various orders for the switched spinning current method.

v). Higher order contributions

In terms of spinning current the highest order of mechanical stress dependent periodic offset voltages determines the sampling rate of the offset voltage to avoid aliasing. With the continuous spinning current method, the Fourier spectrum of the offset voltage was measured up to the fifteenth order. However, for offset components of fifth order ΔA_5 up to fifteenth order ΔA_{15}, no mechanical stress dependence could be observed.

Order ΔA_i	***Source of offset***	***Stress dependence*** $\Delta A_i / \Delta A_2$
1	aliasing from 1st order piezoresistivity and junction thickness modulation	< 0.30 %
2	piezoresistivity and junction thickness modulation	100 %
3	aliasing from 1st order piezoresistivity and junction thickness modulation	< 0.25 %
4	junction thickness modulation (only continuous spinning current)	< 2.00 %
5	aliasing from 1st order piezoresistivity and junction thickness modulation	< 0.03 %
6	aliasing from 2nd order piezoresistivity and junction thickness modulation	< 0.03 %
7...15	-	< 100 ppm

Tab. 3.3 Offset dependence of different fourier orders ΔA_i.

To conclude, periodic offset components up to the fifteenth order in the spatial switching angle φ were investigated and compared with theory. The cause of offset stems from the effects of mechanical stress changing the piezoresistive properties of the active region of the Hall sensor. Furthermore, stress related changes of the biasing conditions of the insulating pn-junction defining the geometry of the device contribute to the offset voltage. However, only contributions up to the sixth order are measured and identified by theory. Periodic offset voltage of higher order exhibit negligible dependence on mechanical stress (see Tab. 3.3). Consequently, in terms of the spinning current method a spatial sampling rate of four samples is sufficient to cancel all stress related offset voltages.

3.4 Implementation of Offset Reduction Using a Double-Hall Sensor

A micrograph of the double-Hall sensor is shown in Fig. 3.31. The sensor detects the magnetic induction perpendicular to the chip plane and is operated according to the theory given in section 2.4. It is fabricated in a standard CMOS process which provides a transistor n-well and source/drain diffusions. This n-well has a

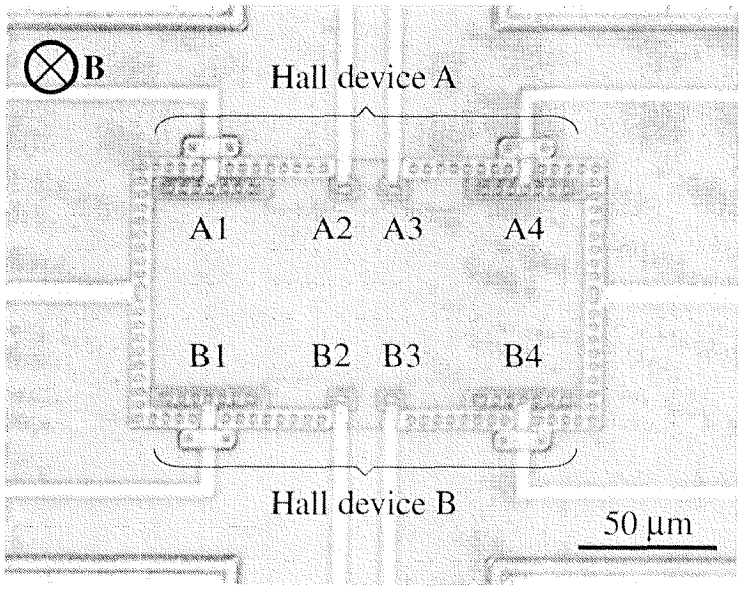


Fig. 3.31: Micrograph of the double-Hall sensor fabricated in CMOS technology. The structure is a combination of two Hall devices with their contacts on only one side.

size of 50 x 130 μm^2 and is electrically insulated from the substrate by a pn-junction. The single Hall devices are operating independently from each other as shown in Fig. 3.32. A variation of the current I_A only changes the sensitivity of device *A* which is given by the slope of the curves and depends linearly on I_A. At the same time, the sensitivity of device *B* operated at a current of $I_B = 100\ \mu A$ remains almost constant (less than 5% deviation). Modeling the device, with a FEM (*SOLIDIS*) with the complete set of dynamic equations, does not reveal any deviation. However, the influence of the pn-junction is neglected in the simulation. Therefore, the effect of I_A on the sensitivity of device *B* is due to modulation of the thickness of the isolating pn-junction [12] (see section 2.2).

For a given magnetic field direction and $I_A = I_B$, the Hall voltages are of opposite signs and the offsets of the single Hall devices are almost equal (see Fig. 3.33 and also section 2.4). The residual signal offset of the double-Hall sensor is measured to be below 2 mT at room temperature. This is 500 times smaller than that of the single Hall devices. The offsets of the individual devices are mainly due to geometrical errors introduced by the transformation of the active region [23]. An analytical solution of the above investigations can be found by means of confor-

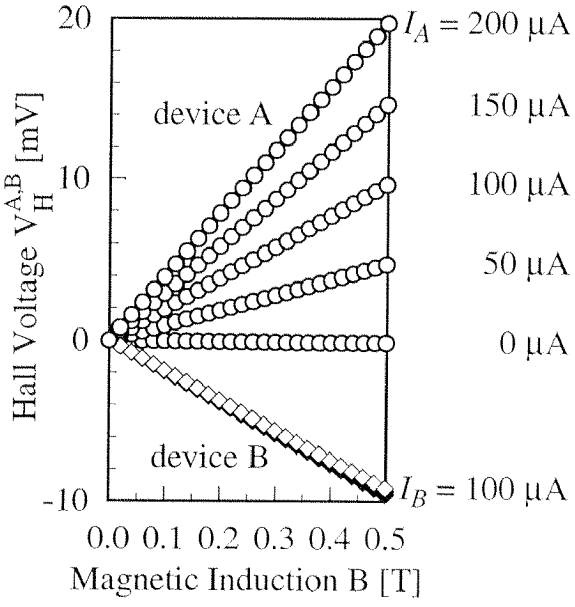


Fig. 3.32: Magnetic response of device A and B while neglecting offset. The devices operate independently of each other.

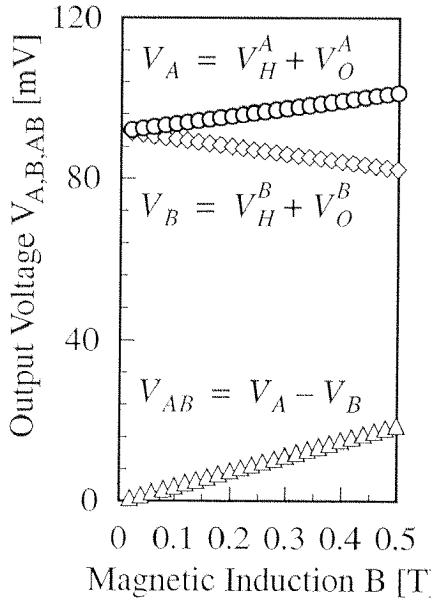


Fig. 3.33: Output of Hall device A and B with $I_A = I_B = 100\ \mu A$. The Hall voltages are of opposite signs, the offsets of equal sign.

mal mapping (see section 2.2). As a result, the offset caused by geometrical errors is due to the boundaries of the device and vanishes if the active region has infinite size. However, the large geometrical offset voltage is reduced by optimizing the contact dimensions [23].

The thermal behavior of the offset voltages is shown in Fig. 3.34. Since the single Hall devices act on the same active region, the thermal offset drifts are perfectly matched. The double-Hall sensor exhibits an offset drift below 10 µV/°C at a biasing current of $I_A = I_B$ = 100 µA. This corresponds to an improvement by a factor of 600 compared to the single device offset drift. The biasing of the double-Hall sensor can be simplified by replacing the two current sources by a single voltage source. In this voltage mode, the offset drift is further reduced to values smaller than 6 µV/°C at the expense of a higher absolute offset as shown in Fig. 3.35.

Finally, the dependence of the residual offset B_O of four devices on temperature was determined. First, the temperature dependent sensitivity S_a of the double-Hall sensor operated in the voltage mode has to be measured (see inset of Fig. 3.36). The negative temperature coefficient is due to the temperature depen-

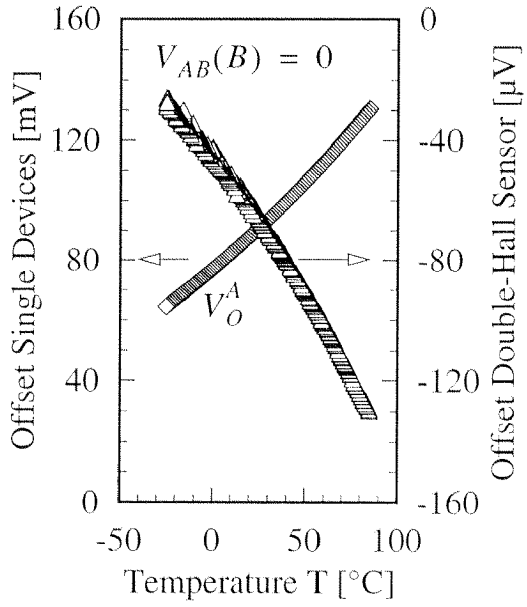


Fig. 3.34: Thermal behavior of the offset voltage of device A and the double-Hall sensor with $I_{A,B}$ = 100 µA.

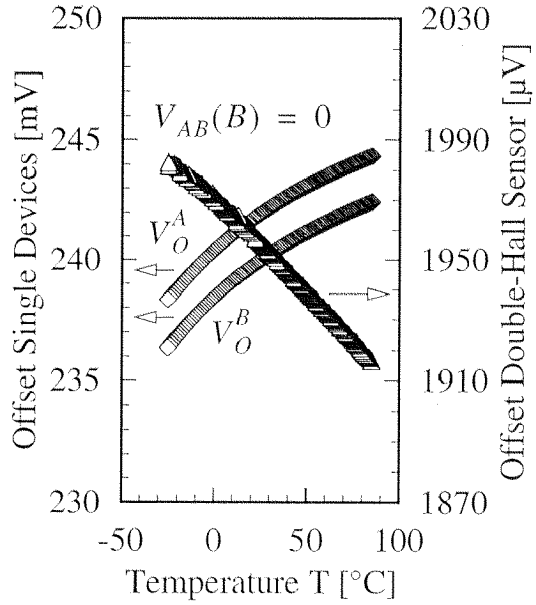


Fig. 3.35: Thermal behavior of U_{Off} of the double-Hall sensor biased with a single voltage source at 2.0 V.

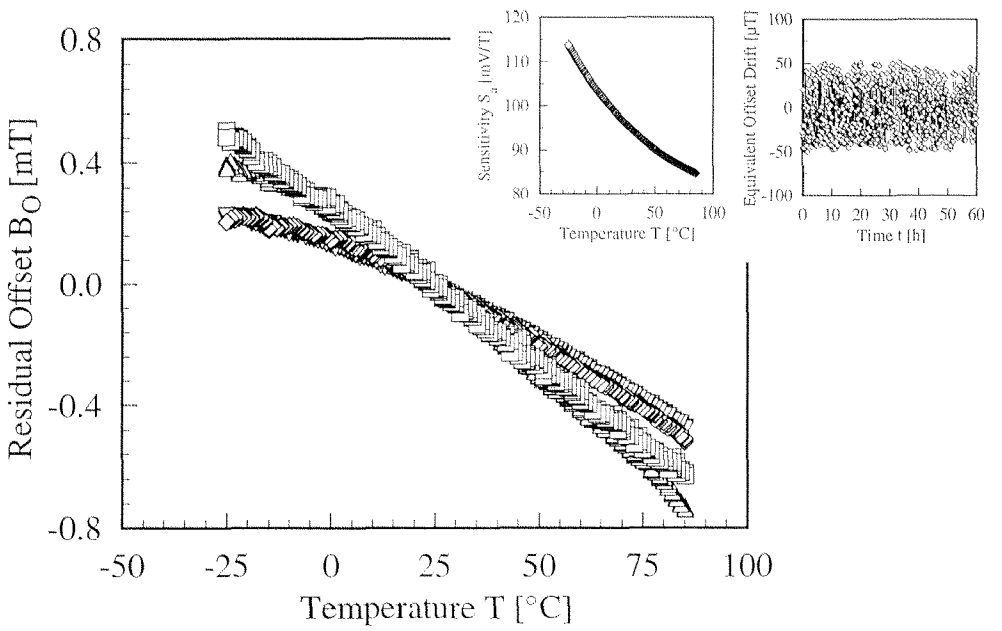


Fig. 3.36: Residual offset B_O of four double-Hall sensors calibrated at 20°C. The offset drifts range from -10.6 to -5.3 µT/°C. The top inset shows the corresponding sensitivity for the double-Hall sensor at a biasing voltage of 2.0 V. The bottom inset shows the drift of the calibrated residual offset B_O with time at 120°C for one device.

dence of the input resistance of the double-Hall sensor. From this data and the measured offset voltage $V_{AB}(B) = 0$, the residual offset B_O is calculated. This is shown in Fig. 3.36 for four different sensors calibrated at 20°C. The residual absolute offset is below 0.7 mT and the maximum thermal drift is smallerthan 11 µT/°C. After calibration, the offset drift with time limits the accuracy of the sensor. An accelerated test at 120°C was performed on the double-Hall sensor. The offset is constant within ±50 µT over 60 hours at this elevated temperature (see inset Fig. 3.36).

In conclusion, the double-Hall sensor requires only a small amount of electronic circuitry and allows implementation of an inexpensive and accurate magnetic sensor microsystem. The offset drift is self-compensated and can additionally be calibrated at any *arbitrary* temperature. Consequently, low offsets over a wide temperature range are obtained with no restriction on the cut-off frequencies due to the operation scheme of the sensor, such as in the case of spinning current.

3.5 References

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4 VERTICAL CMOS TRENCH-HALL DEVICES

Although lateral Hall devices show excellent performance for many applications, a sensitivity parallel to the chip surface is requested [1 to 3]. A sensitivity parallel to the chip surface is achieved with the so called vertical Hall device [4 to 10]. However, conventional vertical Hall devices suffer from a strong cross-sensitivity due to an insufficient carrier path confinement [4]. In contrary, the presented trench-Hall devices show very small cross-sensitivity due to the thin active region defined by the two parallel trenches. Additionally, trench-Hall devices offer the possibility of dynamic offset compensation as demonstrated in section 2.3. This makes them superior to, e.g., magneto-transistors which suffer from a large offset [11, 12]. For applications where the absolute value of the magnetic field is of interest, the additional process steps needed for the trench-Hall devices are justified. A major advantage of the presented trench-Hall devices is its compatibility to the CMOS process [13]. Consequently, front-end electronics for sensor operation can be co-integrated on the same chip enabling an accurate and inexpensive microsystem for magnetic field measurements [14].

In this chapter, the basic design considerations are derived to estimate the input resistance R and sensitivity S_a of a trench-Hall device for a specific contact arrangement. The considerations deal with two types of sensors: devices with all contacts on the chip surface; and devices requiring contacts which electrically connect to the bottom of the active region. The device fabrication is explained in details along the different manufacturing steps related to pre-processing and the following standard CMOS-process. The additional manufacturing steps are in line with the thermal budget of the subsequent CMOS processing. Finally, the feasibility of fabrication of trench-Hall devices is proven by measurement results. The measurement results demonstrate, that trench-Hall devices are well suited as magnetic vector probes for induction in the range of several milli-teslas.

4.1 Design Considerations

In order to achieve a sensitivity to magnetic induction parallel to the chip surface, the active region of a conventional lateral Hall device is rotated towards a vertical orientation with respect to the chip surface (see Fig. 4.1). However, for technological reasons the position of the contacts has to be re-arranged. Two cases are considered: i) all device contacts at the chip surface, and, ii) contacts on the chip surface and deep contacts electrically connected to the bottom of the active region by access pillars. Arranging all contacts at the chip surface results in design constraints concerning a symmetric device geometry. These constraints are eliminated by introducing deep contacts at the expense of lower sensitivities for a given range of the biasing voltages as discussed later.

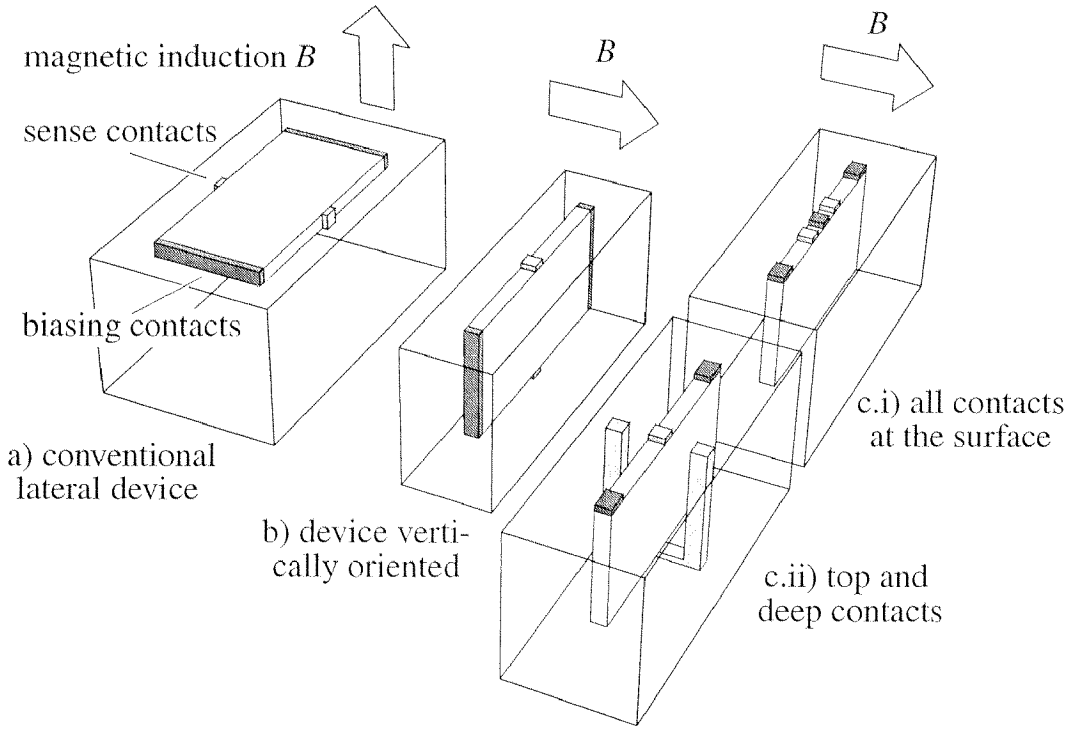


Fig. 4.1: a) Conventional lateral Hall device sensitive to magnetic induction perpendicular to the chip surface. b) Hall device with a vertical orientation with respect to the chip surface. The sensitivity is parallel to the chip surface. c.i) Hall device with all contacts at the chip surface, and, c.ii) device with top and deep contacts.

i). Single ended device with all contacts on the chip surface
For simpler processing all contacts of a vertically oriented Hall device are transformed to the chip surface (see Fig. 4.1.c.i). Through means of conformal mapping, approximate expressions for the geometric corrections factor can be determined (see section 2.2). The expressions are calculated with help of a corresponding circular Hall plate with known resistance R and sensitivity S_a.

A conformal, bilinear transformation maps a circular Hall plate to a single ended device of infinite size of the active region [15]. Therefore, the expression

$$x = \tan\left(\frac{\vartheta}{2}\right) \tag{4.1}$$

gives a correspondence between points on the boundary of the circular Hall plate described by an angle ϑ. Locations on the surface of the single ended device are represented by the coordinate x [15] (see Fig. 4.2). However, a physical device has a limited extension, which results in circular areas cut out of the active region of the corresponding circular Hall plate [15]. The missing parts cause a perturbation of the symmetry, which is illustrated in Fig. 4.2 by a non-symmetric rectangular Hall device.

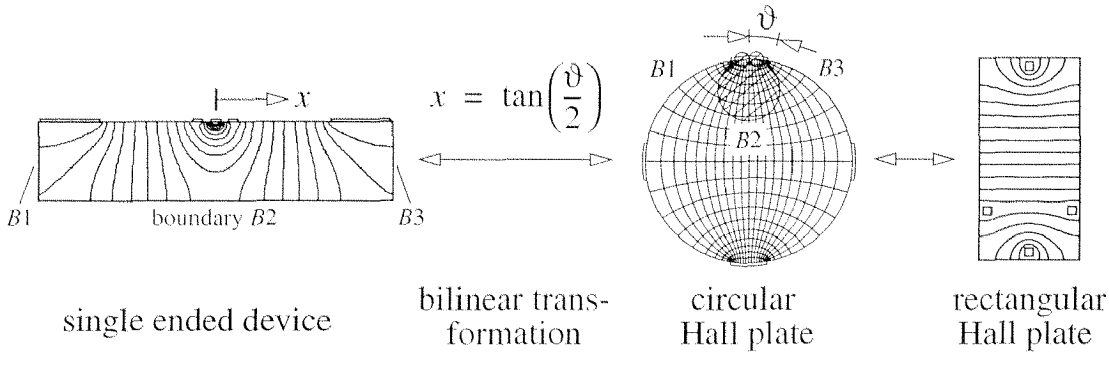


Fig. 4.2: Single ended device with corresponding circular Hall plate. The correspondence is defined by a bilinear transformation. A limitation of the active region of the single ended device by the boundaries B1 to B3 causes a perturbation of the device symmetry illustrated by the rectangular Hall device on the right.

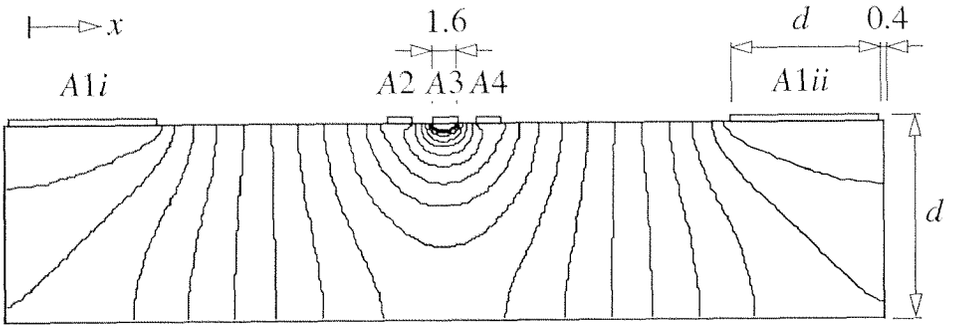


Fig. 4.3: Design rules for a single ended Hall device. Defining the width of contact A1i, A1ii, and A3, and using a bilinear transformation determines the geometry of the device (dimensions in µm).

In order to calculate the geometry correction factors, the following design rules are defined: a center contact $A3$ of 1.6 µm width, and contacts $A1i$ and $A1ii$ with widths equal to the trench etch depth d. The contact position is calculated from a circular Hall plate with contacts having an opening angle of (2ϑ) and corre-

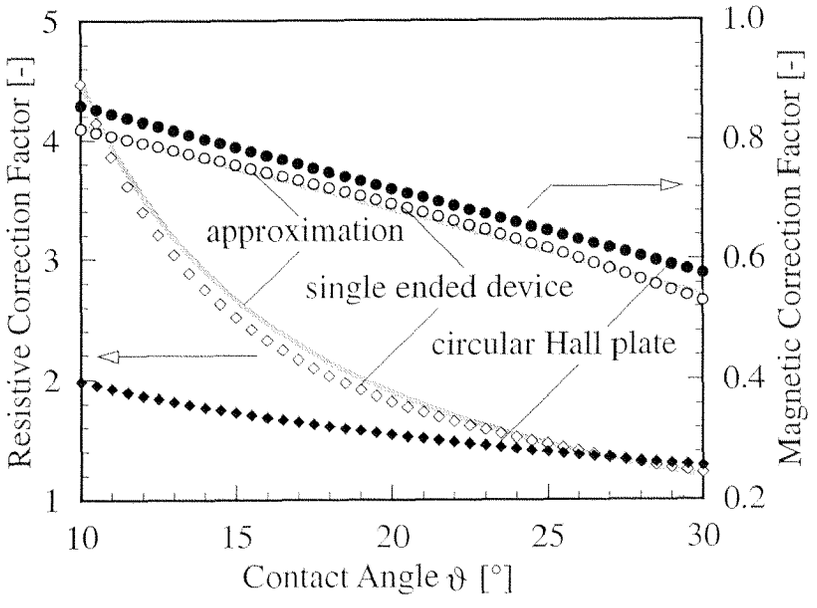


Fig. 4.4: Calculated geometry correction factors by means of FEM. The results are compared with correction factors of a circular Hall plate according to [15]. Furthermore, the FEM results are parameterized resulting in analytical approximations for G_R and G_S.

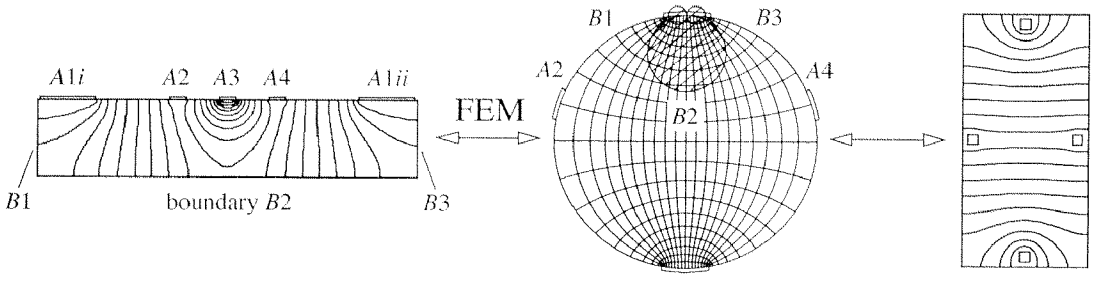
sponding scaling. Through the use of FEM, geometric correction factors are calculated according to the above design rules. This method shows good agreement with analytical calculations as shown in section 3.1. Operating the device with a biasing current applied to contacts $A1i$-$A1ii$ and $A3$, and sensing the response at contacts $A2$ and $A4$, G_R and G_S are estimated as

$$G_R = -0.200 \cdot 10^{-3} d\vartheta - 11.1 \cdot 10^{-3} \vartheta + 6.44 \cdot 10^{-3} d + 0.870, \tag{4.2}$$

$$G_S = \frac{7.22}{0.0844d + 0.221\vartheta - 1.87}, \tag{4.3}$$

with a trench etch depth $d = 10 \ldots 20$ µm and a contact angle $\vartheta = 10 \ldots 30°$. In the above range, the deviation of G_R and G_S from the FEM-results is below 6.4% and 2.9%, respectively (see Fig. 4.4). However, these deviations are below the tolerances of the CMOS fabrication process.

To overcome the lack of layout symmetry, the geometry of a single ended Hall device is optimized by FEM. The sense contacts $A2$ and $A4$ of a single ended device are rearranged until the single ended device corresponds to a rectangular device with two mirror axes. The corresponding transformation for a circular device is achieved by rotating and scaling of the contacts $A2$ and $A4$ (see Fig. 4.5). The layout of an optimized single ended Hall device is shown in Fig. 4.6. The correction factors are calculated to be $G_R = 1.612$ and $G_S = 0.684$.



single ended device | circular Hall plate | rectangular Hall plate

Fig. 4.5: Optimizing the geometry by rearranging the contacts A2 and A4. The corresponding change of the layout is shown for a circular and a rectangular Hall device. Optimization results in a layout with two mirror axes that are easily recognized by the rectangular Hall device on the left.

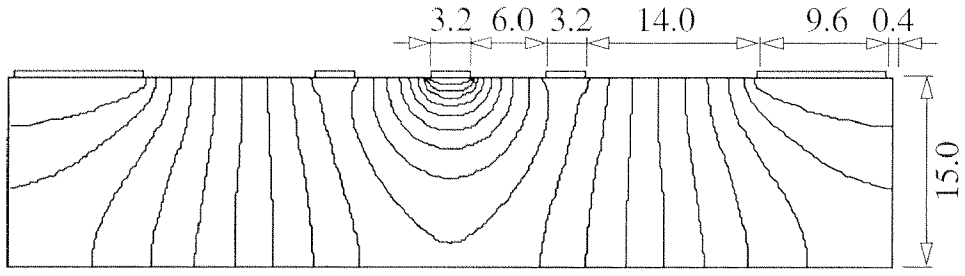


Fig. 4.6: Layout with corresponding dimensions of an optimized single ended Hall device (dimensions in μm).

ii). Device with top and deep contacts

An electrical connection to the bottom of the active region of a trench-Hall device (i.e. a deep contact) is assumed. It allows the design of Hall devices which are invariant under a rotation of π/2. In terms of current spinning, this allows a more effective offset reduction in the presence of non-linearities (see section 2.3). However, determining the geometry analytically is laborious. Therefore, the problem was solved using FEM. Two possible layouts were considered: a) a design with two deep contacts, and, b) a design with a single deep contact (see Fig. 4.7). Considering a trench etch depth of 15 μm the contacts *A*2 and *A*4 of

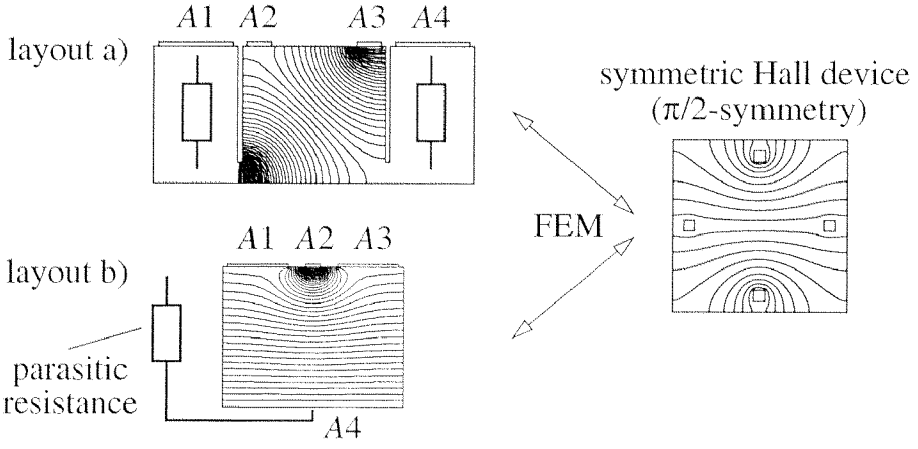


Fig. 4.7: Possible layouts of trench-Hall devices with deep contacts having a π/2-symmetry. Additionally, the technology presented in the next chapter introduces a parasitic series resistance in the contact path which has to be compensated electronically.

layout a) have a width of 3.2 µm and a distance of 10.7 µm. This results in geometric correction factors of $G_R = 2.776$ and $G_S = 0.955$ and a contact angle $\vartheta = 6.4°$ of a corresponding circular Hall plate. For layout b) the width of contact $A1$ and $A3$ is calculated to be 6.5 µm and the width of contact $A2$ to be 1.6 µm. With a distance of contacts $A1$ and $A2$ equal to 1.8 µm, the geometric correction factors are calculated to be $G_R = 1.356$ and $G_S = 0.641$. This corresponds to a circular Hall plate with a contact angle $\vartheta = 25.4°$

The access pillar which connects the deep contact with the chip surface causes a parasitic resistance in the contact path. Using a contact to sense voltage, the contact resistance has no influence on the device operation. For current contacts the resistance results in a voltage drop. This voltage drop causes a change of the common mode voltage at the sense contacts for different biasing currents. These changes have to be compensated electronically. Furthermore, for a given biasing voltage range, the resistance reduces the biasing current, and, therefore, the sensitivity [15].

4.2 Fabrication Technology

The manufacturing scheme for the trench-Hall device consists of various pre-processing steps followed by the industrial CMOS-process of Austria Mikro Systeme International AG [16]. This differs from the common approach where structures or sensors are manufactured in a CMOS process and then post-processed to add additional features [17]. Pre-processing is used for reasons of incorporating high temperature steps that are required for the Hall device fabrication. These steps are only compatible with the thermal budget of the CMOS process if performed in advance.

To summarize on device fabrication, pre-processing is basically used to etch a vertically oriented active region by trench etching, which is similar to the fabrication of DRAM memory cells [18]. In subsequent processing electrical contacts for the active region are defined and front-end electronics for sensor operation can be co-integrated. In order to design the front-end electronics the entire design environment of the particular CMOS process is accessible.

Manufacturing starts with the deposition of a hard-mask on a (100)-p-substrate (see Fig. 4.8). The hard mask is a sandwich of dielectric CMOS layers - a silicon oxide of 500 Å thickness, a silicon nitride layer of 1500 Å thickness, and a thicker silicon oxide of 20'000 Å thickness. The thickness of the thick silicon oxide layer is mainly defined by the trench etch depth as will be discussed later. The hard mask serves two purposes: first, as a mask for the trench etching, and second, to protect the region of the silicon substrate not used for sensors.

In a next step, the hard mask is opened by plasma etching using CHF_3/CF_4 chemistry [19]. Then, parallel trenches are etched to a depth up to 20 µm. The trenches have a width of 0.8 µm and a distance of 2.4 µm, which will be the thickness of the device active region. Bromine-based chemistry was chosen for the etching due to the high silicon etch rate and high etch selectivity to the oxide hard mask [20]. With a selectivity larger than 1:20, a hard mask oxide layer of 20'000 Å was sufficient. During trench etching, a passivation oxide is grown at the side-walls which has to be removed [21]. Additionally, a sacrificial oxide is grown and removed to reduce contamination in the etch grooves [22].

All side-walls of the trenches are doped by ion-implantation. To improve the deposition on the side-walls, a quad mode implant of phosphorous ions with a tilt

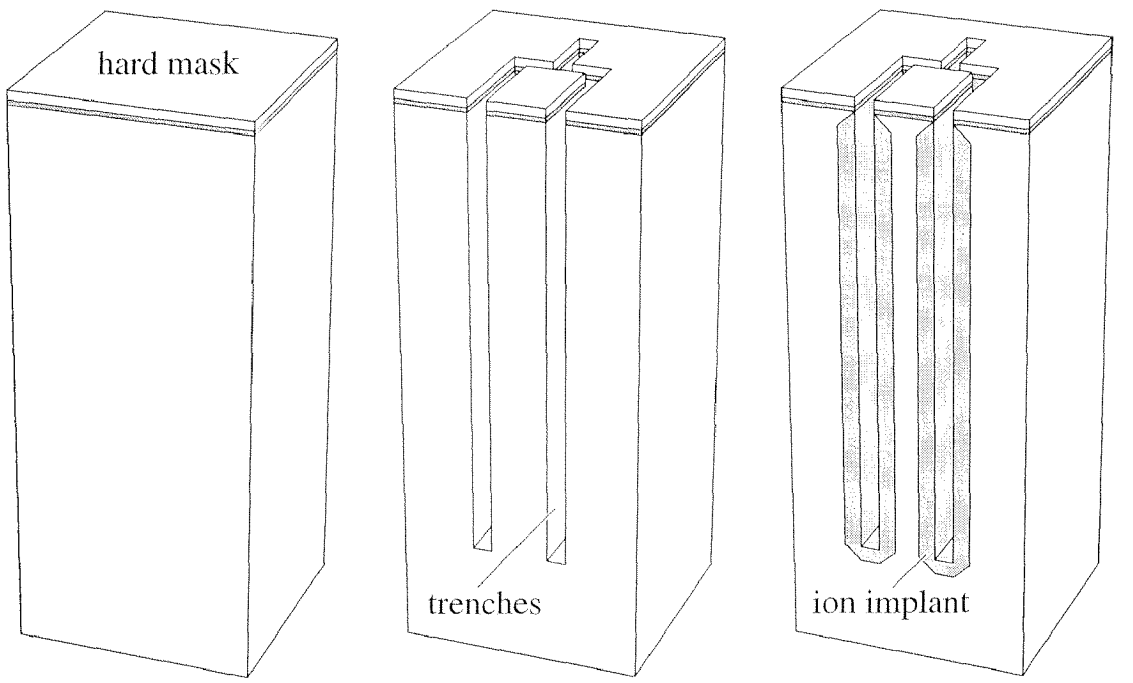


Fig. 4.8: Left) (100)-p-substrate with deposited hard mask. The dielectric layers serve as mask for trench etching and as a protection of the substrate. Middle) Hard mask opened and trenches etched to depths deeper than 20 µm. Right) Etch grooves pre-deposited by ion-implantation. For good side-wall deposition a quad mode implant with a tilt angle of 4° is chosen.

angle of 4° was used. With this unique method of trench etching, followed by ion-implantation, a pre-deposition depth of over 20 µm is achieved without a time consuming drive-in from the chip surface [16]. Additionally, the ion-dose can be arbitrarily chosen to optimize the performance of the trench-Hall devices. Therefore, the parameters of the co-integrated electronics are not affected. The drive-in of the pre-deposited donors occurs simultaneously with the transistor well formation in the process steps that follow [13].

As the next step, the trenches are oxidized for isolation. The side-wall oxide is annealed to reduce initial stress in the crystalline silicon. A highly n-doped poly-silicon layer is deposited, which is mainly intended as planarization of the trench grooves. This turned out as a crucial step in the pre-processing (see Fig. 4.9).

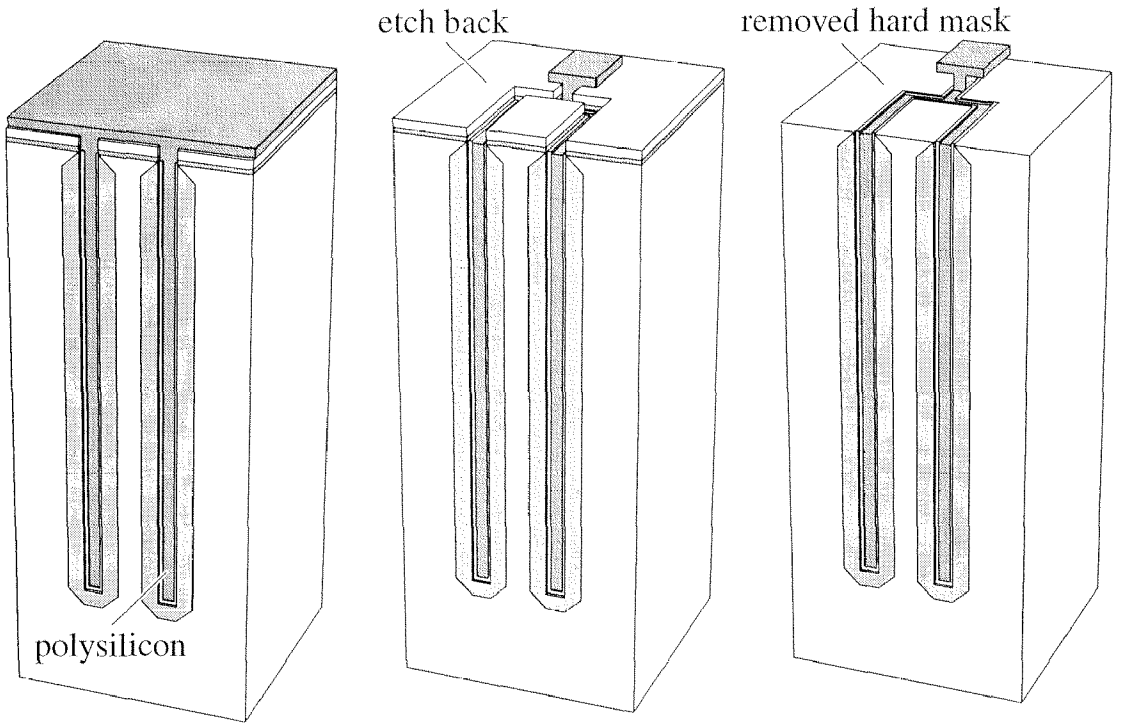


Fig. 4.9: Left) The trenches are oxidized and filled with a polysilicon layer. The polysilicon serves as planarization and as an electrical shield. Middle) The polysilicon is patterned and etched back providing an electrical contact to the polysilicon fill from the chip surface. Right) Finally, the hard mask is removed which finishes the pre-processing.

Improper planarization results in a gap in the metal coverage over the trench. Additionally, the polysilicon serves as an electrical shield to improve the EMC of the trench-Hall device. The polysilicon is patterned and etched back by plasma etching. As a result, a polysilicon paddle is formed which allows to electrically connect the polysilicon in the trench in the later processing steps.

Finally the rest of the hard mask is removed by wet etching to terminate pre-processing. As an alternative, the thick oxide of the hard mask can be removed prior to deposition of the polysilicon. This reduces the topology height of the structure, which caused problems with the resist deposition in the process that follows. The wafers with the finished pre-processed trench-Hall devices serve as a starting substrate for the CMOS process.

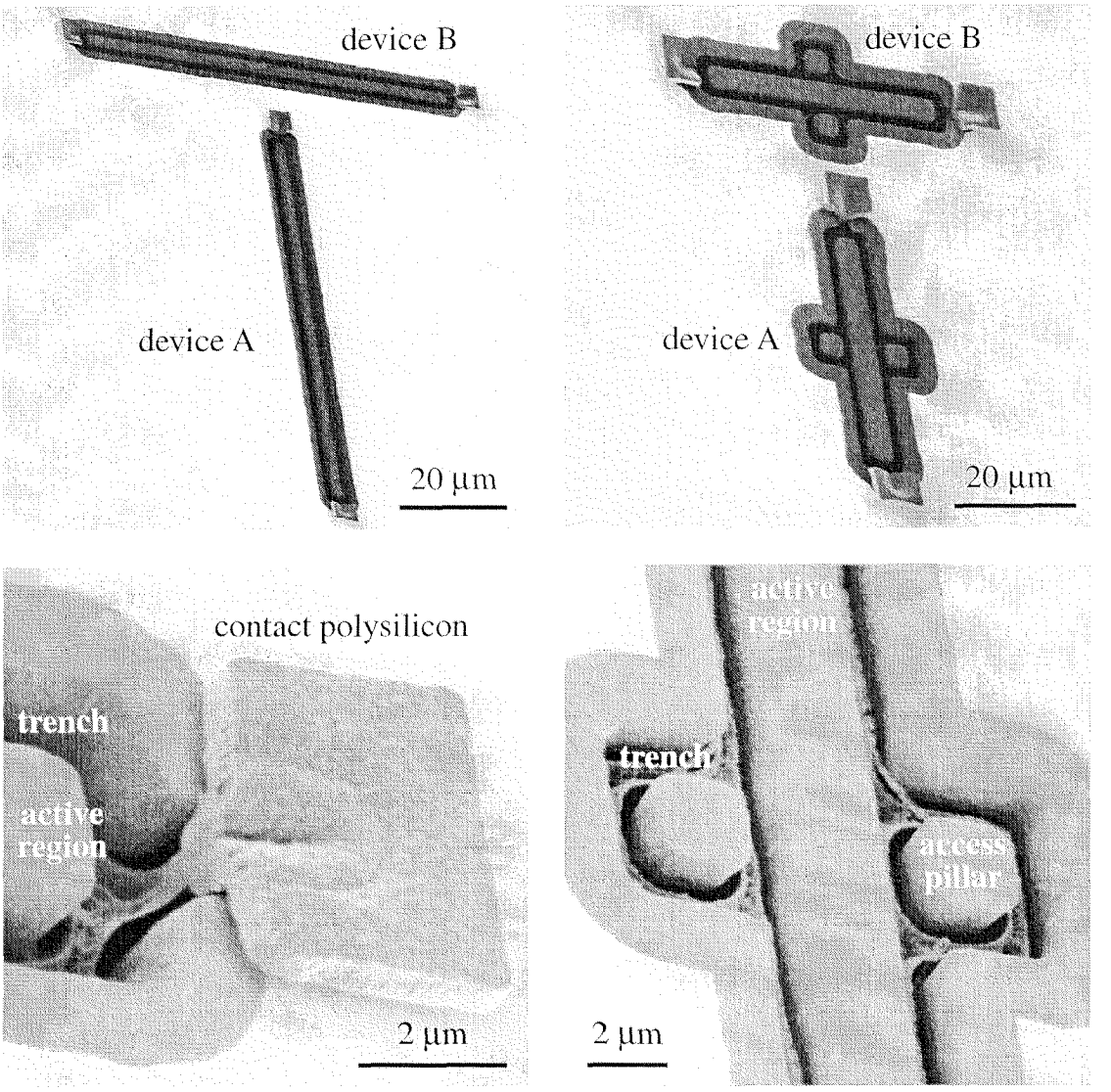


Fig. 4.10: Top left) Top view of the buried active region of a trench-Hall device. Top right) Top view of the active region with access pillars for deep contacts. Bottom left) Contact of the trench polysilicon fill. The polysilicon is used for electrical shielding and planarization. Bottom right) Close-up view of access pillars.

In the pictures in the upper row of Fig. 4.10, top views of the upper edges of buried trench-Hall devices are shown. The devices are in an orthogonal arrangement in order to use them as a magnetic vector probe. In the top right picture, a view of a trench-Hall device with deep contacts is shown. The access pillars of the deep contacts are fabricated simultaneously with the active region. The lower

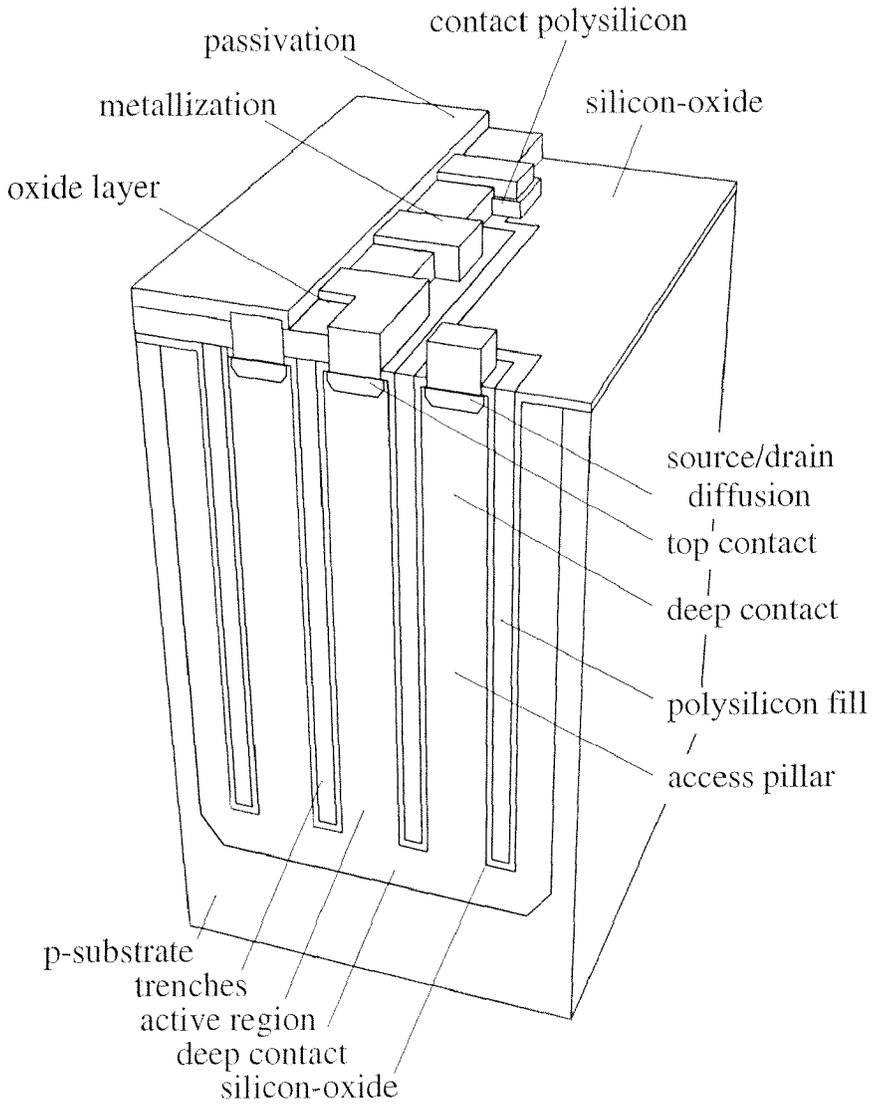


Fig. 4.11: Cross section of a trench-Hall device with top and deep contacts after completing the CMOS process. The drive-in of the pre-deposited donors of the active region and the access pillars occurs simultaneously with the transistor-well formation.

row of pictures of Fig. 4.10 shows close-up views, such as that of the electric contact for the polysilicon fill and of the access pillars of the deep contacts.

In the CMOS processing, the drive-in for the active region and the access pillars occurs simultaneously with the transistor-well formation. As a result, a homogeneously doped active region is achieved with a depth up to 20 µm and

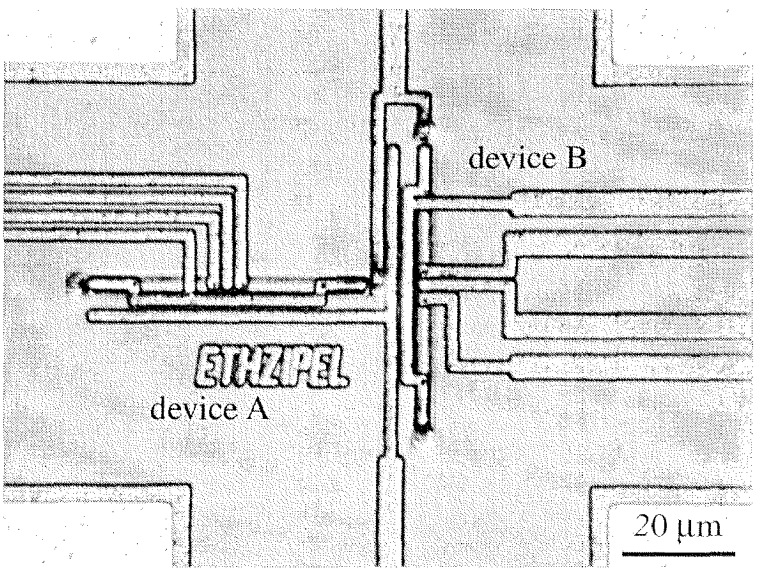


Fig. 4.12: .i: Micrograph of two orthogonally arranged single ended devices with all contacts on the chip surface.

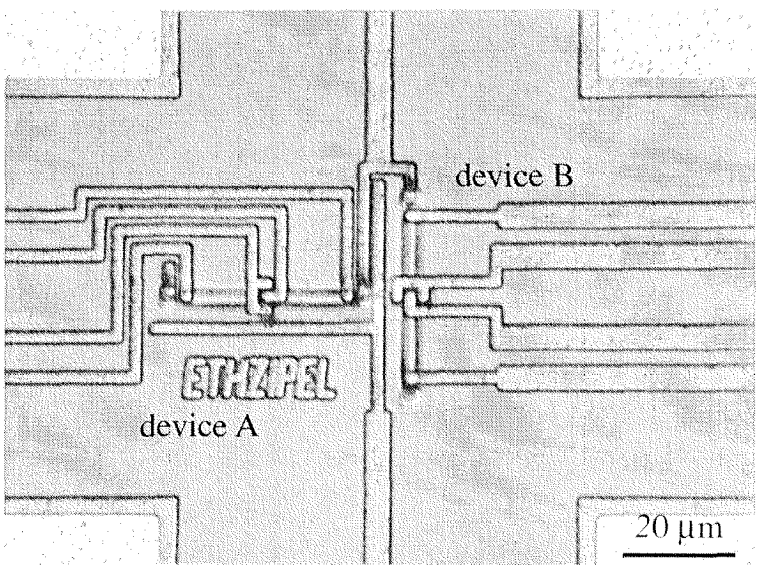


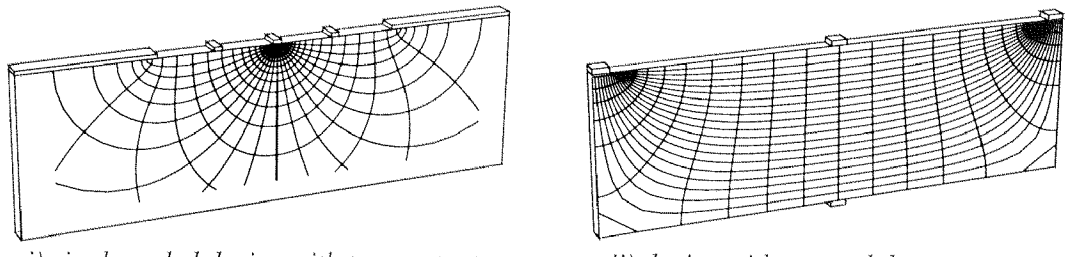
Fig. 4.12.ii: Micrograph of two orthogonally arranged devices with top and deep contacts.

a thickness of approximately 2.4 µm. Furthermore, the electrical contacts of the Hall device are formed by source/drain diffusions as shown in Figs. 4.11, 4.12.i and 4.12.ii. In the current approach, only selected CMOS steps are used consisting of: a drive-in diffusion, BPSG deposition, a planarization step of the trenches with SOG, source/drain implant through contact holes, activation, metallization, and passivation. The realization of Hall devices that are feasible and compatible with a standard CMOS process and co-integration of front-end electronics is straight forward.

4.3 Electrical and Magnetic Performance

In order to prove the feasibility of the fabrication process, two different device geometries were manufactured: i) a single ended device with top contacts, and, ii) a device with top and deep contacts (see Fig. 4.13). Additionally, the single ended device was designed according to the design guidelines of Eqs. (4.1 to 4.3).

The current related sensitivities S_I were determined to be 250 V/AT for device i) and 314 V/AT for device ii) (see Fig. 4.14). These values are in the range of the sensitivities of the lateral Hall devices reported in literature [23]. However, the sensitivity can be arbitrarily adjusted by the ion-dose without changing any electrical parameters of co-integrated electronics. For device i) the input resistance R was measured to be a value of 5.3 kΩ. With a contact opening angle of $\vartheta = 17°$ and a thickness of $t = 2.4$ µm, $n = 8.5 \cdot 10^{15}$ cm^{-3}, $\mu_n = 0.12$ m^2/Vs, $r_H = 1.1$, and $\theta_H/\tan\theta_H \sim 1$, the resistance R calculated with Eq. (4.2) turns out to be 5.0 kΩ, and the sensitivity to be $S_I = 250$ V/AT. The linearity error of device i) is below 0.1%, and below 0.15% for inductions up to 0.3 T of device ii) (Fig. 4.15).



i) single ended device with top contacts *ii) device with top and deep contacts*

Fig. 4.13: Investigated geometries to demonstrate the feasibility of the fabrication process of the trench-Hall devices.

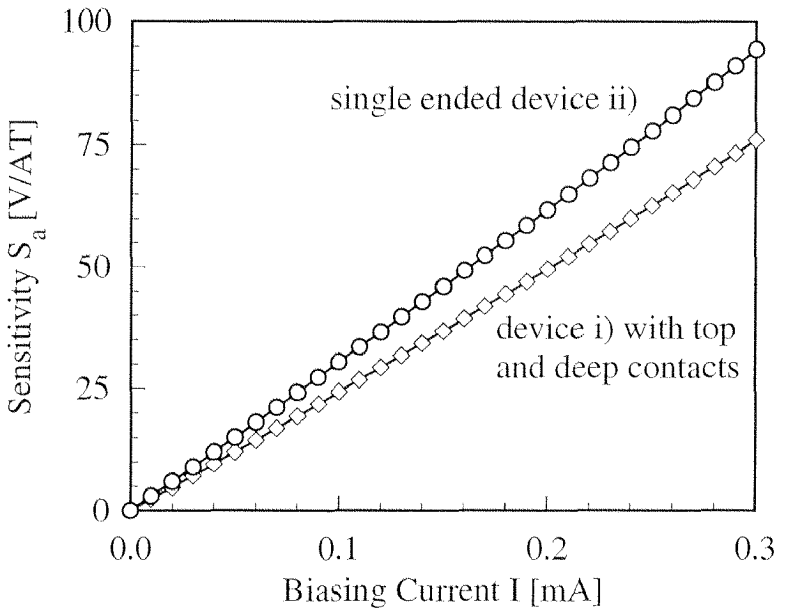


Fig. 4.14: Measured absolute sensitivity $S_a = S_i \cdot I$ of the trench-Hall devices as a function of the biasing current I. A current related sensitivity S_i of 250 V/AT for device i) and 314 V/AT for device ii) can be obtained based on a linear fit.

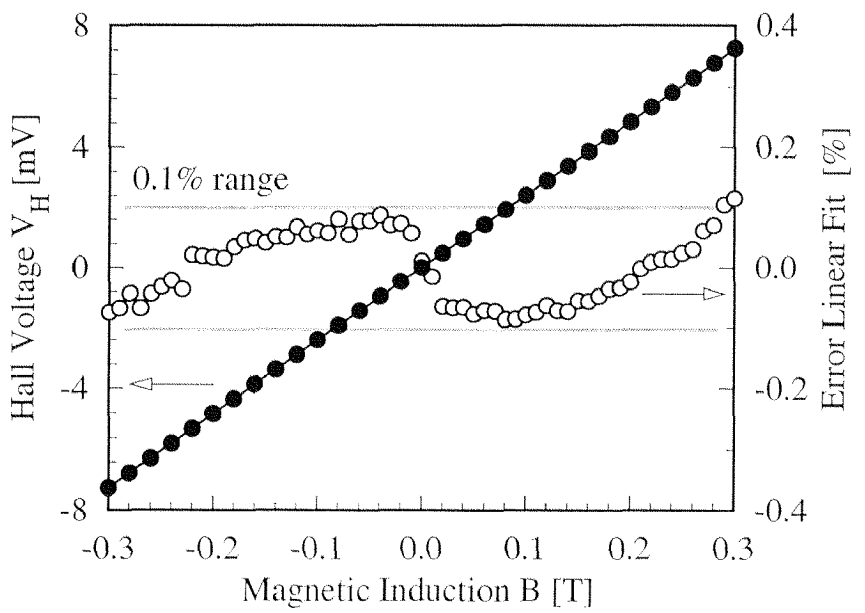


Fig. 4.15: Magnetic response of the single ended trench-Hall device i) at a bias I = 100 µA. The deviation from a linear fit is below 0.1% of the full scale. For the device ii), a deviation of 0.15% was measured for the same conditions.

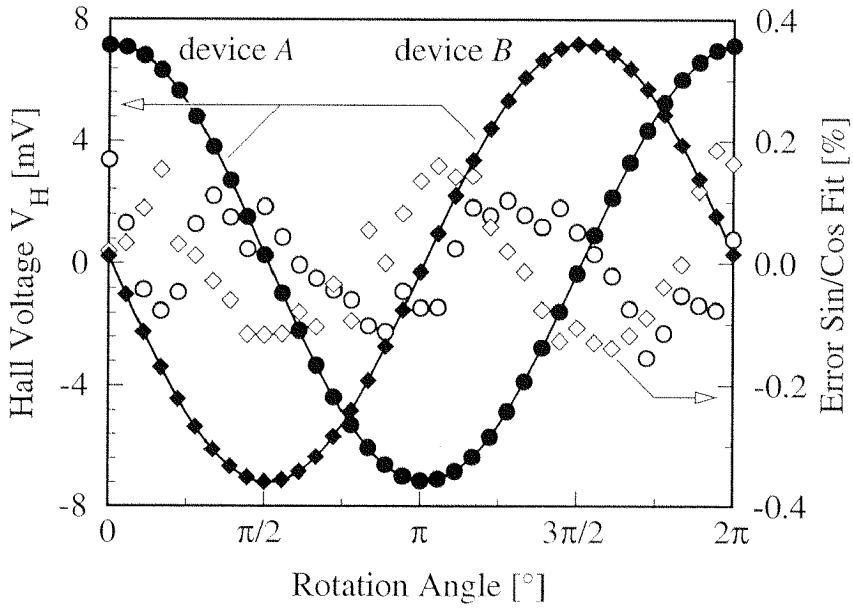


Fig. 4.16: Angular field dependence of two orthogonal trench-Hall devices A and B (according design rules given in i)) in an orthogonal arrangement for an induction of 0.3 T parallel to the chip surface. The signal deviations from sine and cosine fits are smaller than 0.2%. These deviations are due to a combination of non-linearity and cross-sensitivity.

In order to determine the cross-sensitivity, the response of the Hall device *A* and *B* in an orthogonal arrangement (see Fig. 4.10) were measured while rotating the magnetic induction parallel to the chip surface (see Fig. 4.16). Cross-sensitivity and linearity errors for a magnetic induction of 0.3 T result in a signal deviation from a sine-/cosine-function below 0.2%. This is expressed in terms of an equivalent angular error of approximately 0.2°.

The trench-Hall device can be dynamically offset compensated by means of the current spinning. Measurements of ten devices showed residual offsets from 0.1 to 1.0 mT. These residual offsets resulted from a non-linearity introduced by poor biasing of the silicon substrate. This can be improved by placing the substrate contact further away from the trench region.

4.4 References

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5 APPLICATIONS

CMOS magnetic sensors are best suited for applications demanding high system performance at a low price. Two possible applications are presented in this chapter: a current monitor and a wear-free angle measurement system.

Application of intelligent power electronics is a key technology for today's efficient energy management and for modern transportation systems. However, power electronics require small and inexpensive current measurement systems for monitoring and protection [1 to 6]. Additionally, safety requirements demand galvanic isolation between power lines and control circuitry. A fully packaged current monitor system is demonstrated in this chapter [7]. The manufacturing is in line with commercial IC mass fabrication and packaging technology. Utilizing the *LOC* packaging technology, a small, accurate and inexpensive current monitor system is realized which satisfies the safety requirements for galvanically isolated current monitoring [8]. The performance can be further improved by ferromagnetic field concentrators [9, 10] and on-chip compensation techniques [11].

As another application, a wear-free angle detection system is demonstrated [12, 13]. The approach provides a low cost solution well suited for a harsh environment in terms of mechanical load and wide temperature range. Traditional angle position detectors meeting these specifications are mainly based on permanent magnets combined with conventional lateral Hall plates measuring only one magnetic field component perpendicular to the chip plane [14]. Due to this principle, the angle measurement accuracy is limited or the use of expensive multi-pole magnets and extensive signal processing is required [15]. A more accurate angle detection, independent of the field magnitude, becomes possible by detecting the two components of magnetic inductions B_x and B_y parallel to the chip plane by, e.g. two vertical Hall devices [16]. Furthermore, a CMOS single-chip solution can be provided, as well as a low-cost packaging approach for the entire system.

5.1 Current Monitor

A convenient principle for the galvanically isolated measurement of an electrical current flowing through a conductor is the detection of the current-generated magnetic field with an appropriate magnetic sensor [1]. As an example, a current of 10 A through a wire 1 mm in diameter generates a field of 1 mT at a distance of 1 mm. In this field range, the favorable properties of the widely applied integrated Hall sensor can be used for accurate and stable measurements [17].

The magnetic field strength drops quickly with distance from the conductor (see Fig. 5.1). Therefore, the sensor must be as close as possible to the current path in order to achieve a high system response. At the same time a perfect electrical isolation between the conductor and magnetic sensor must be provided. The above requirements must be fulfilled by the system package. For the success of market oriented microsystem development, this needs to be done at minimum cost since packaging is a major contributor to the final system cost, and its importance is often underestimated. Thus, the packaging solution must be as simple as possible, and must be compatible with batch techniques. For inexpensive mass production, the exclusive use of standard IC technologies is required.

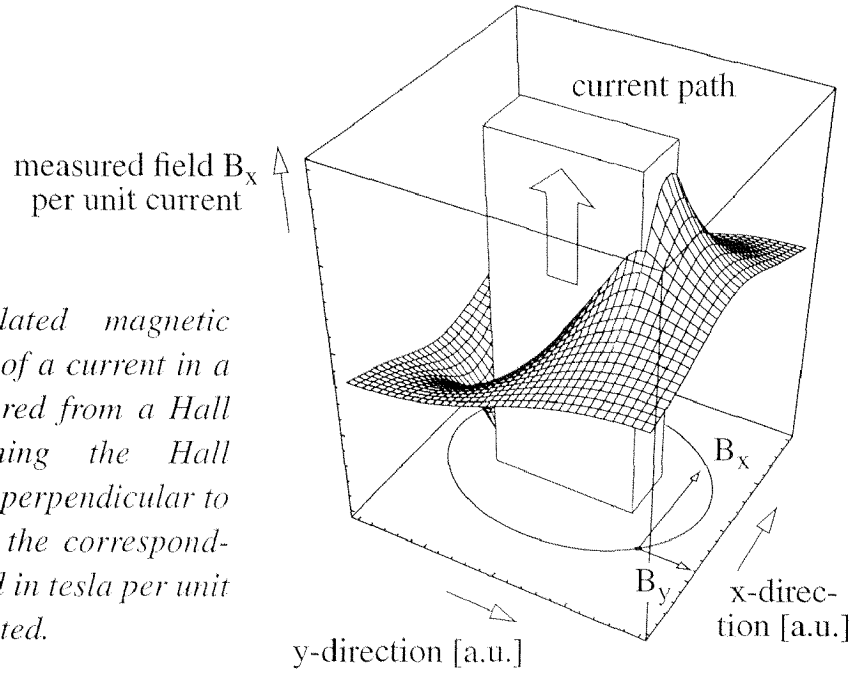


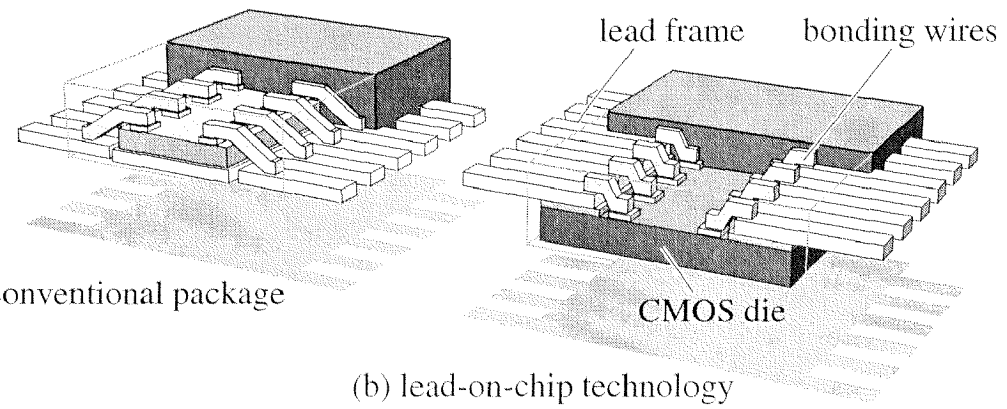
Fig. 5.1: Calculated magnetic field distribution of a current in a conductor measured from a Hall sensor. Positioning the Hall device in a plane perpendicular to the current flow, the corresponding magnetic field in tesla per unit current is calculated.

In this chapter, a highly sensitive current monitor system is demonstrated. It is based on a CMOS die containing two Hall sensors which is packaged using lead-on-chip technology (*LOC*) [8]. This packaging technique is widely applied for assembly of memory cells in order to increase the ratio between chip size and package dimension. Therefore, inexpensive and reliable high volume production is provided.

LOC Packaging technology

Most IC chip packaging techniques use a thin lead frame and bonding wires to ensure electrical connections from the die to outside [18]. In conventional packaging the lead frame connection ends at the periphery of the die and all bonding pads are arranged close to the chip edges as shown in Fig. 5.2a. Thus, the total package covers a substantially larger area than the original die size. For many applications such as CPU's and ASIC's this is only of minor importance.

In the *LOC* packaging technology the tips of the lead frame extend over the die surface (see Fig. 5.2b). The bonding connections are made completely over the die surface and the bonding pads can be placed at almost any location. Therefore, the final package size is only slightly larger than the die and an optimum ratio of die area with respect to package area is achieved. With *LOC* technology the die occupancy is increased to more than 70% of the packaging area compared with the conventional case. For that reason, the *LOC* technology is widely accepted for packaging of space consuming devices such as memory cells [8, 18].



(a) conventional package

(b) lead-on-chip technology

Fig. 5.2: Arrangement of CMOS die relative to lead frame for electrical interconnects (a) in conventional packaging technique and (b) in lead-on-chip (LOC) technology.

LOC technology is well suited for inexpensive mass packaging within an IC manufacturing line. First, the chips are mounted by an automatic die bonder on a lead frame stripe. Then, the stripe is fed into a wire bonder. After plastic molding and cutting of the lead frame stripe into single packaged IC's, the production process is finished. In this work, we exploit the advantages of the *LOC* packaging technology for the realization of a CMOS current monitor system as shown in Fig. 5.3. Here, the lead frame contains signal lines and an additional wide conductor which carries the electrical current to be measured. As a result, low resistance for the current path is achieved which is comparable to a shunt resistor usually used for current measurements. The low power dissipation in our system combined with an excellent thermal conductivity to an external printed circuit board leads to minimized temperature increase of the current path.

For mechanical interconnection the die is glued on the lead frame with a polyimide *LOC* glue tape. Consequently, the current path is close to the Hall sensors

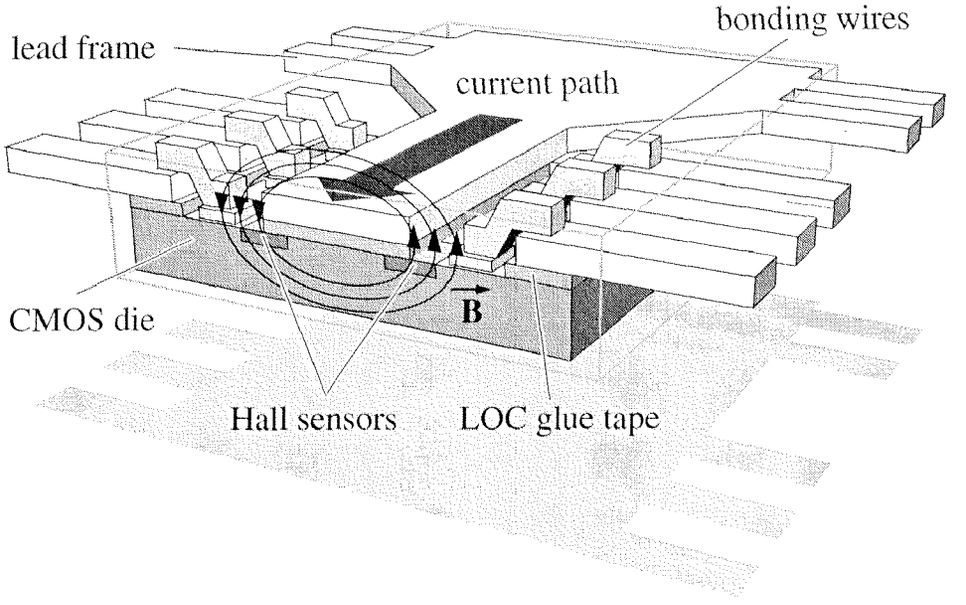


Fig. 5.3: Current monitor system packaged using lead-on-chip technology (LOC). The lead frame contains signal lines and current path. It is attached close to the CMOS die with a LOC glue tape. Thus, high system response and excellent isolation is achieved.

(approximately 90 µm) and electrically isolated by the polyimide tape. The *LOC* glue tape consists of a polyimide carrier coated on both sides with a thin layer of high purity thermoelastic adhesive. The polyimide carrier maintains electrical isolation between the chip and the current path, while the adhesive provides excellent mechanical strength. Additionally, dwell time and the die thermal exposure are minimized which makes the *LOC* glue tape suitable for high volume assembly operation.

System Assembly

The packaging technique applies to any integrated magnetic sensor. For our application two lateral Hall devices were chosen and arranged on either side of the current path (Fig. 5.4). The current monitor system response is defined as the difference of the responses of the Hall sensors on the CMOS die in order to reject common-mode magnetic fields [19]. The geometry was set to a width to length ratio of 22 µm to 66 µm. With a biasing current of 0.25 mA, the current related sensitivity of a single Hall sensor is 510 V/AT with a voltage drop of 3.9 V. The power related sensitivity is then calculated to be 130.8 $A^{-1} T^{-1}$. The major drawback of Hall sensors is their high offset voltage which highly degrades the current monitor system performance. The offset voltages were compensated by continu-

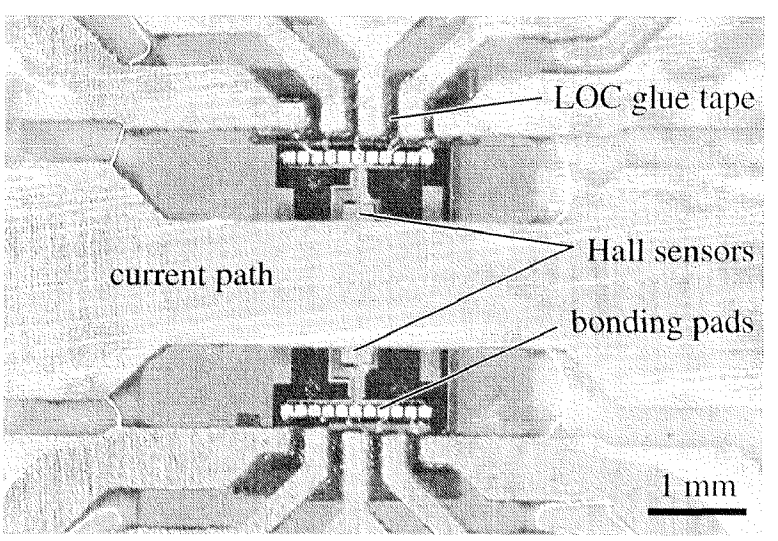


Fig. 5.4: CMOS die mounted on a lead frame. The Hall sensors are sensitive perpendicular to the chip surface. They are located on each side of the current path for rejection of common-mode magnetic fields.

ous spinning current to values lower than 1 μV with a sampling frequency of 2 Hz [20]. Additionally, the spinning current method reduces the temperature drift of the offset voltage [21]. For cancelling the sensitivity variations over time and temperature, on-chip coils were designed [11]. The solenoid is realized with two metal layers available in the CMOS process. The coil occupies an area of 310 x 310 μm^2 for forty turns. In this configuration the biasing current is limited to 14.5 mA to remain within the design rules resulting in a magnetic induction of 6.1 mT. In order to avoid capacitive coupling between the coils and the Hall sensor terminals, an additional polysilicon layer for shielding is necessary. Two possible measurement configurations are now considered. Either the on-chip coil is used for autocalibration of the Hall sensor, or the Hall sensor, current path and on-chip coil are operated in a closed-loop setup. Additionally, the on-chip coil can be used for field tests to improve the reliability of the current monitor system.

The *LOC* technology is optimized for automatic high volume IC packaging. It requires appropriate lead frame stripes and a sufficient amount of chips for machine adjustment. In order to allow flexible system prototyping with a limited number of samples, different steps during the packaging process had to be manually controlled in this work. Nevertheless, the complete system fabrication and assembly process is in line with standard *LOC* packaging technology.

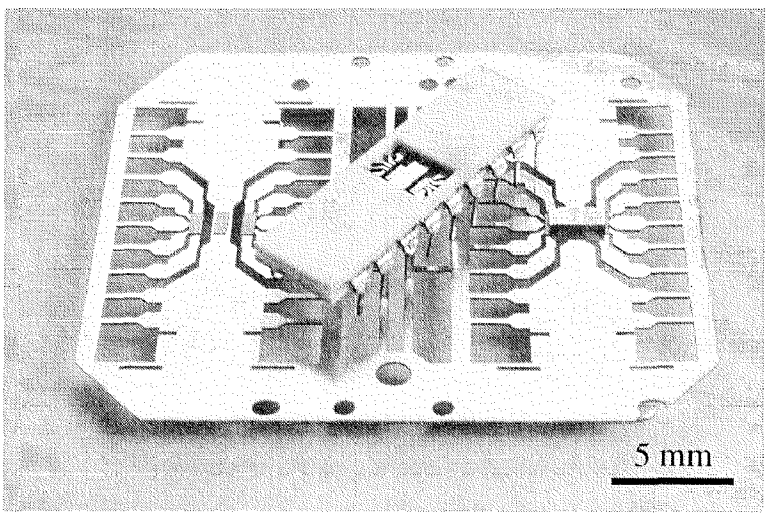


Fig. 5.5: Different phases of system packaging process: section of lead frame stripe patterned with LOC glue tape (left), CMOS die mounted on lead frame (right) and the fully packaged current monitor system (center).

The lead frame for the current monitor system was laid out by CAD and manufactured by laser cutting (see Fig. 5.5 and Fig. 5.6, top). The lead frame material is copper with a thickness of 250 µm. In order to improve the surface properties for subsequent bonding of gold wires, a 10 nm Ti layer followed by a 400 nm Au layer is sputter deposited after laser cutting. The lead frame has the same dimensions as an 18-pin DIL package. It fits into industrial *LOC* die bonders, offered by, e.g., *ESEC SA*, Cham, Switzerland. Eight pins of the lead frame are used for the low resistive current path which has a width of 1.3 mm. The remaining pins are used for electrical interconnections to the Hall sensors.

The lead frame was pre-patterned with a thermoelastic polyimide supported tape adhesive such as, e.g., ABLELOC 5000 from Ablestik, Electronic Materials & Adhesives (see Fig. 5.5, left and 5.6, middle). The *LOC* glue tape offers high dielectric strength combined with excellent mechanical properties. The sandwich structure consists of a polyimide carrier coated with thermoelastic adhesives. With an overall thickness of 90 µm a dielectric strength higher than 14 kV is achieved. The *LOC* glue tape application to the lead frame was made on a hot-plate at 250 to 300°C. To maximize the adhesive properties a pressure of 3 bar must be applied for 50 ms.

The accuracy of the CMOS die placement limits the performance of the current monitor system. Misalignment causes a loss in the magnitude of the magnetic field measured by the Hall sensors. Furthermore, a mismatch of the Hall sensor signals on each side of the current path occurs which makes it necessary to calibrate the system. Commercial *LOC* die bonders offer an excellent placement accuracy in the µm-range which makes the packaging technology well suited for the application. On the other hand, changes of the distance from current path to the Hall sensors over lifetime is mainly governed by the thermal expansion of the *LOC* glue tape. A typical value specified for the ABLELOC 5000 tape is 35 ppm/°C in a temperature range from -50 to 150°C. In this range the change of distance is calculated to be 0.6 µm. Approximating the degradation of the magnetic field caused by the current with a 1/r-dependence, a change of 75 ppm over the above temperature range is calculated. Since a high number of samples are necessary for process optimization for a *LOC* die bonder, the CMOS die was placed with a flip-chip fine placer and misalignment corrected manually (see Fig. 5.5, right and 5.6, bottom). For attaching the CMOS die to the *LOC* glue tape on the lead frame, a temperature of 300°C over 200 ms is recommended.

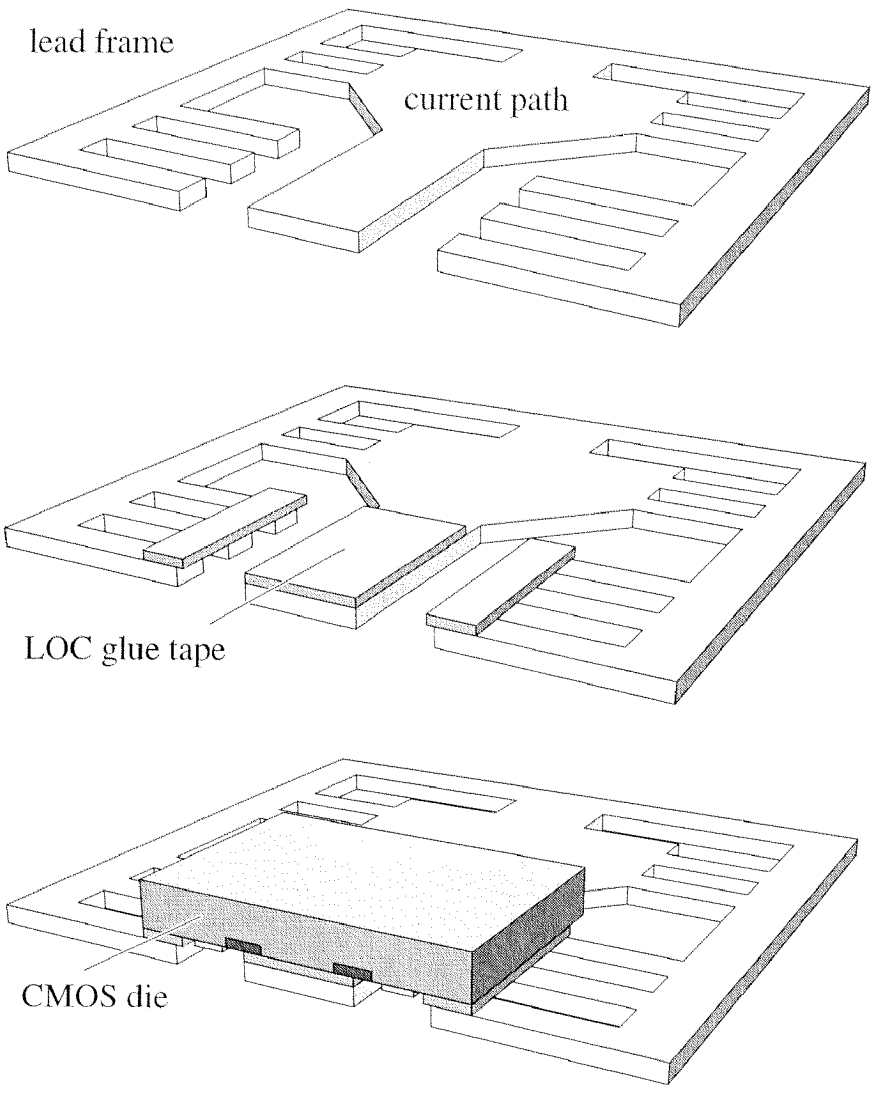


Fig. 5.6: top) The lead frame for the current monitor system laid out by CAD and manufactured by laser cutting. The material is copper with a thickness of 250 µm. Middle) The lead frame pre-patterned with a thermoelastic polyimide supported tape adhesive. The tape offers high dielectric strength combined with excellent mechanical properties. Bottom) Placement of the CMOS die with a commercial LOC die bonders.

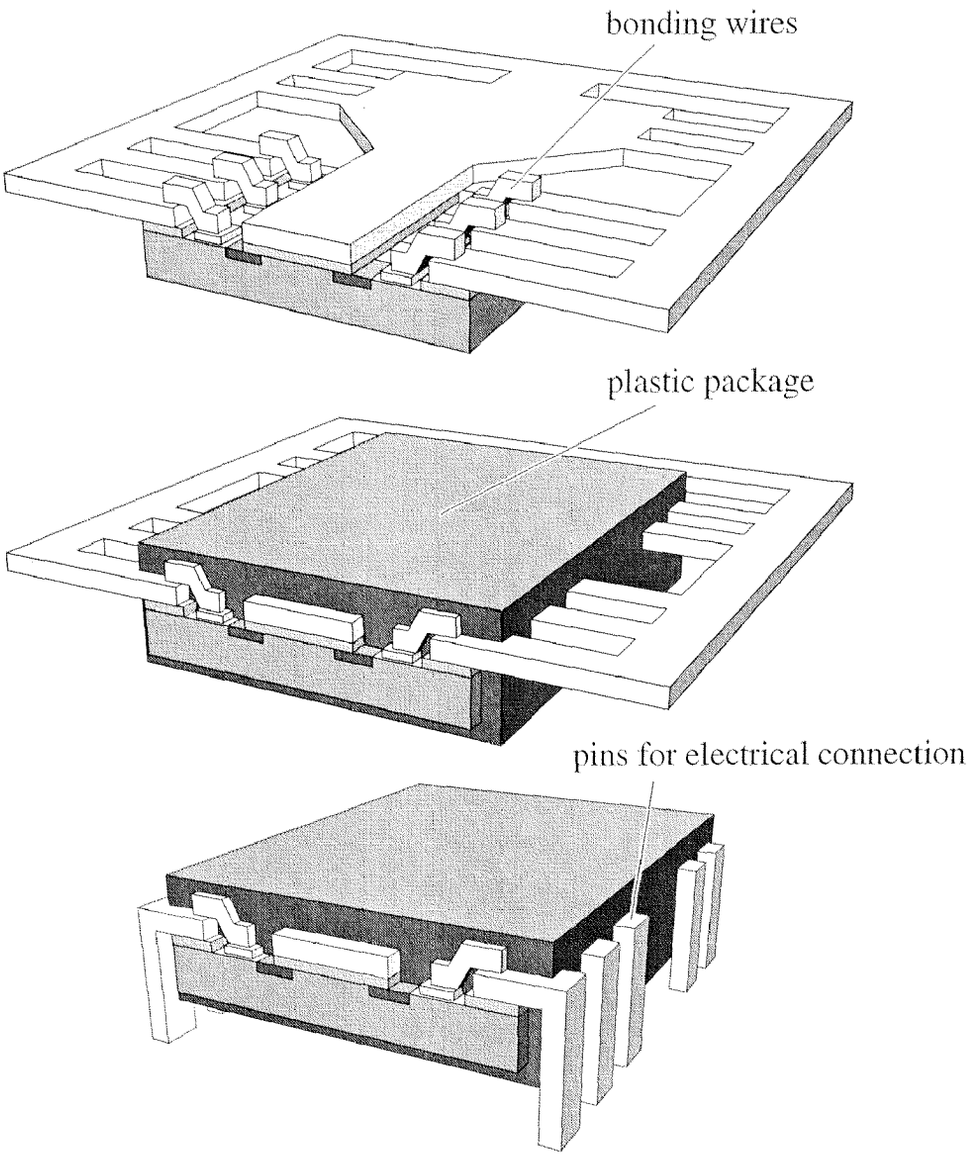


Fig. 5.7: Final packaging steps with commercial packaging tools. Top) Wire bonding on the flipped lead frame. Middle) Plastic molding of the system. Bottom) The formation of pins and the final system test.

In the final step, the current monitor system is bonded with a commercial wire bonder, plastic molded, and tested with standard equipment used in IC mass production.

System Characterization

The response of the current monitor system is defined as the difference of the output signals of the two Hall sensors on each side of the current path (see Fig. 5.4). According to Fig. 5.8 a system sensitivity of 82 µV/A in the range of ±10 A is measured. The non-linearity of the system response is below 0.3%. The quadratic nature indicates that the cause of the non-linearity is mainly due to power dissipation in the current path. Therefore, with temperature compensation of the Hall sensor sensitivity, the system linearity can be easily improved.

The resolution and accuracy of the current monitor system is limited by the following properties:

- offset voltage
- offset drift over temperature
- sensitivity drift over temperature
- noise level of output voltage

For the current monitor system, the continuous spinning current method was used to reduce the offset voltage and its offset drift. A sampling frequency of 2 Hz

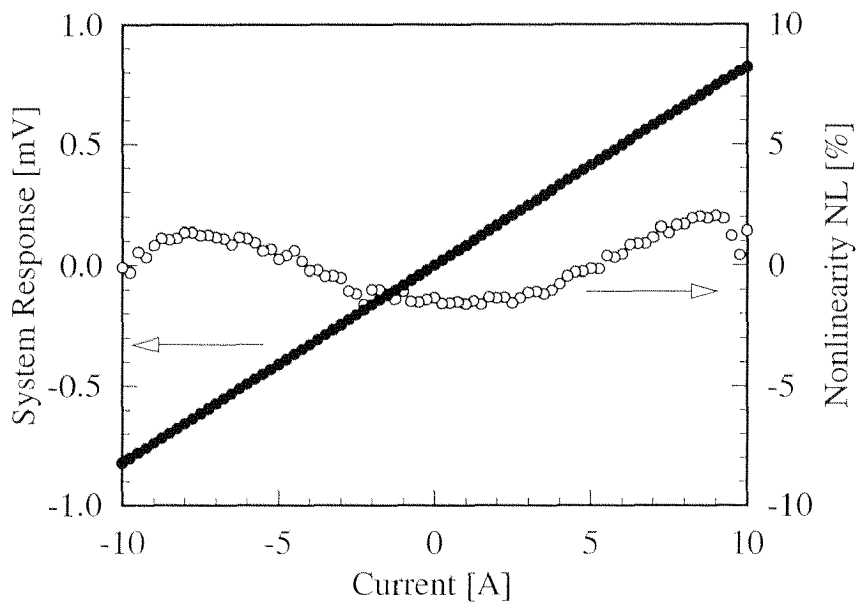


Fig. 5.8: Response of current monitor system. The signal is linear with a sensitivity of 82 µV/A. The non-linearity is smaller than ±0.3% and the signal offset lies below 2 µV. This results in a measurement accuracy better than 50 mA.

results in a residual offset of 1 µV at room temperature which is mainly limited by noise. Offset, noise and non-linearity result in a measurement accuracy better than 50 mA and a resolution of 10 mA.

Offset reduction and temperature compensation can be performed by electronics integrated on the same CMOS die as the Hall sensors. The noise level of the electronics will be the limiting factor for the system resolution. An equivalent rms white-noise level for the current monitor system with integrated electronics is assumed to be in a range from Nl_w = 100 µT/√Hz to 400 µT/√Hz. The value of the system resolution is calculated from the white-noise level Nl_w, the bandwidth Δf and the magnetic field B_I generated at the position of the Hall sensors per unit current. Assuming Gaussian distributed peak-to-peak amplitudes of noise, multiplying the Nl_w value by a factor $A = 6.6$ ensures that the calculated resolution exceeds only 0.1% of the measurement time, its peak value [22]. The equation is given below:

$$I_{Res} = A \frac{NL_w \sqrt{\Delta f}}{B_I} . \tag{5.1}$$

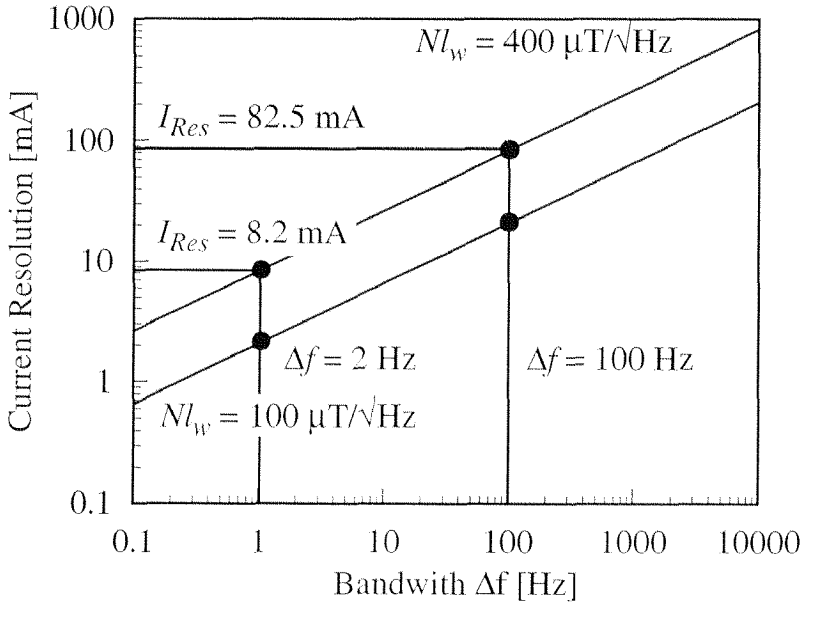


Fig. 5.9: Calculated system resolution with integrated electronics assuming white-noise levels ranging from Nl_w = 100 to 400 µT/√Hz with Gaussian distributed peak-to-peak noise amplitudes.

In Fig. 5.9 the calculated current monitor system resolution is shown as a function of the bandwidth Δf for different white-noise levels Nl_w. As an example, with an rms white-noise level Nl_w = 400 µT/√Hz and a bandwidth Δf = 100 Hz, a resolution of better than I_{Res} = 82.5 mA is achieved (see Fig. 5.9).

System Improvement with Field Concentrators

The system sensitivity can be further enhanced by magnetic field concentrators. Two methods are tested (Fig. 5.10): In *method (a)* a soft ferromagnetic sheet is attached to the backside of the thinned CMOS die. In *method (b)* tip concentrators are fabricated by anisotropic backside-etching and plated with a soft NiFeMo alloy [23, 24].

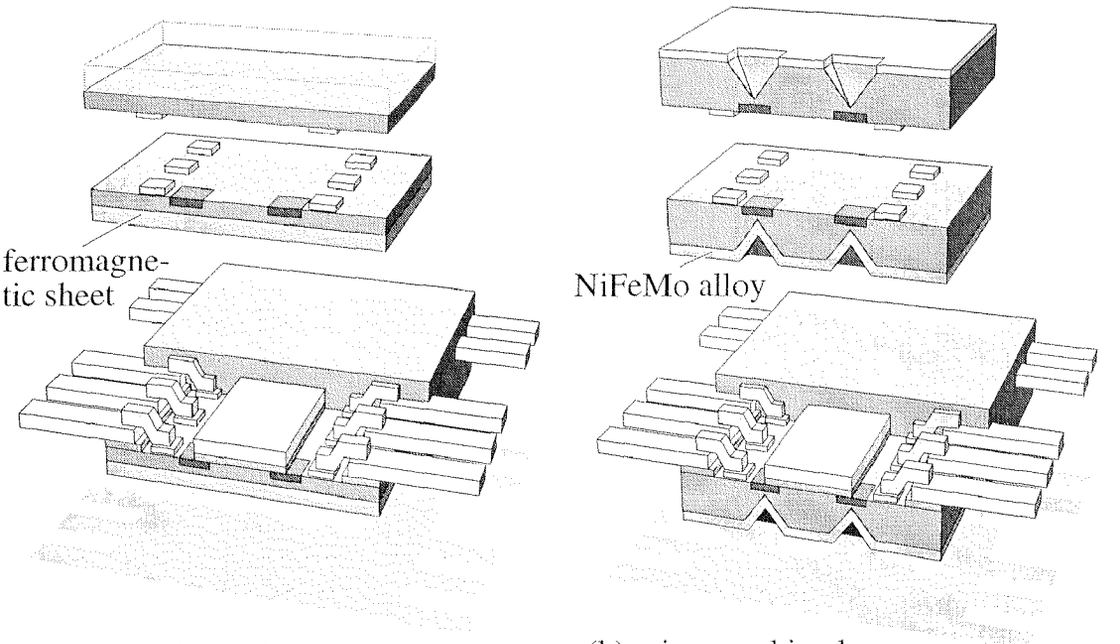


Fig. 5.10: Sensitivity improvement by using field concentrators on the die backside. In method (a) a ferromagnetic sheet is attached to the die which is thinned to 75 µm. In method (b) a tip concentrator fabricated by anisotropic etching is plated with a NiFeMo alloy [23].

The thinning of the CMOS die to a thickness of 75 µm as used for *method (a)* was performed at the chip-level by grinding. Wafer-level etching techniques can also be used, but for reasons of mechanical stability, a minimum thicknesses of only approximately 300 to 400 µm is achieved. A stamped soft magnetic sheet covering the entire die area is attached to the back of the CMOS die with an epoxy glue. In the presence of the soft magnetic sheet the field distribution of the current path is perturbed and the magnetic field lines penetrate the Hall sensor perpendicular to the die surface (see Fig. 5.11). As a consequence, field lines are bent towards the direction of sensitivity of the Hall sensor. Numerical simulations propose an improvement of the performance of the current monitor system by a factor of approximately 1.5. Furthermore, for a high relative permeability of the magnetic sheet ($\mu_r > 2500$), its thickness and placement, as well as the thickness of the CMOS die and epoxy glue, become non-critical properties.

The tip concentrators capture the magnetic field generated by the current to be measured and guide it to the region the Hall sensors are placed. Processing starts with anisotropic KOH backside-etching on wafer-level [25]. The tip of the etch-groove points at the center of the Hall sensor. At the present state, the dis-

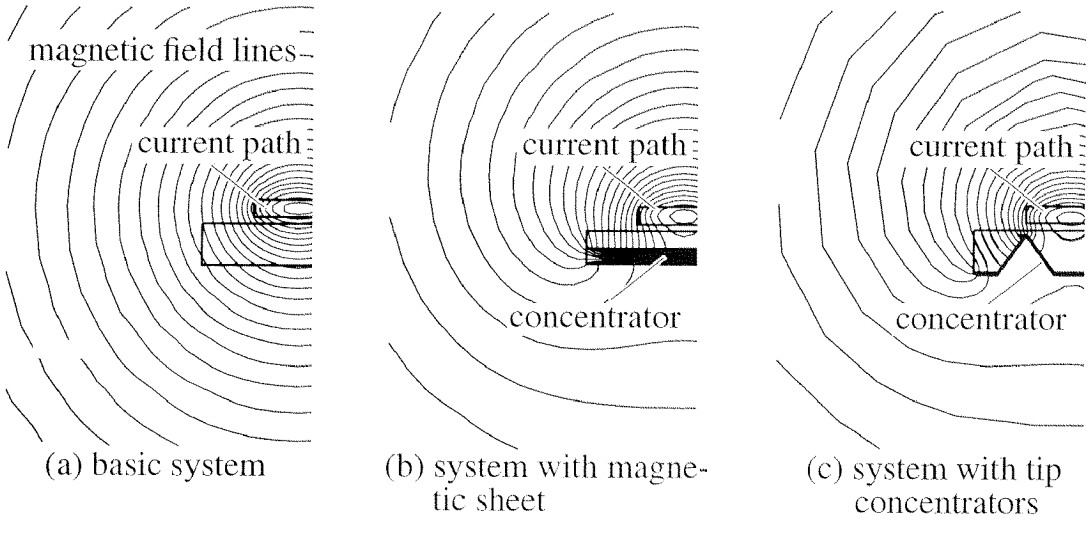


Fig. 5.11: FE simulation of magnetic field distribution for the basic system (a) and system enhanced with ferromagnetic sheet (b). The magnetic field lines are bent towards a perpendicular direction with respect to the CMOS die surface. As a result, higher magnetic response is achieved. In the case of the tip concentrator (c), a higher field density in the area of the sensors is achieved.

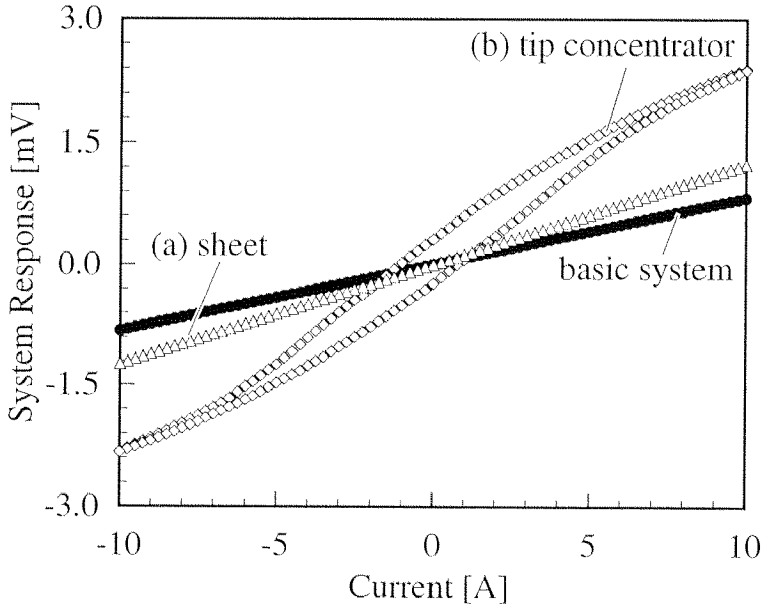


Fig. 5.12: A current monitor with concentrators. With a ferromagnetic sheet (a) the sensitivity is improved to 124 µV/A with ±0.3% non-linearity. The micromachined concentrators (b) improve the sensitivity to 240 µV/A but introduce an additional non-linearity.

tance between sensor and etch groove is defined by lithography and etching properties. For high yield mass-production, an additional electrochemical etch-stop underneath the Hall sensor is recommended [26]. After removing the PECVD nitride used as KOH etch mask, a seed layer sandwich for subsequent electroplating is sputter deposited (10 nm Ti layer followed by a 1.08 µm Cu layer). Electroplating of the NiFeMo alloy follows the procedure according to [23]. The NiFeMo alloy was plated at 30 mA/cm^2 for 3 hours resulting in a film-thickness of approximately 1.5 µm.

The ferromagnetic sheet improves the sensitivity by a factor of 1.5 to 124 µV/A as proposed by numerical simulation (Fig. 5.12). Non-linearity and offset of the system response are not affected by the magnetic sheet. The tip concentrators increase the sensitivity even by a factor of 3 to 237 µV/A. Due to the hysteresis of this particular NiFeMo film an additional non-linearity is introduced.

5.2 Wear-Free Angle Measurement

Cost effective angle detection systems are usually based on a resistive principle, such as a potentiometer, where an electrode touches a resistive layer. However, the approach suffers from severe mechanical wear, and, lifetime and reliability related problems become an issue. In order to overcome these problems, a contactless position detection system is desirable. On the other hand, commercial contactless angle measurement systems are usually based on an optical principle. Nevertheless, such systems never meet the price requirements such as for the automotive market. Another cost effective approach is the use of magnetic sensors in combination with a permanent magnet.

In general, the following requirements apply to a magnetic angle detection system. The magnetic sensors must be small enough to perform a point measurement of the magnetic field. This lowers the requirements for the homogeneity of the permanent magnet, and, consequently its price. Furthermore, the system becomes more robust against mechanical tolerances, e.g., misalignment of sensor and axis of rotation of the permanent magnet. Additionally, if more than one sensor is used to determine the direction of the magnetic field, the sensors have to be placed as close as possible together, preferably on the same chip. This results in best initial sensitivity matching, independent of process tolerances, as well as matching of temperature coefficients. Finally, the sensor setup must allow a simple and low-cost packaging solution.

A concept meeting all of the above requirements is possible by detecting the two components of the magnetic inductions B_x and B_y parallel to the chip plane by, e.g. a magnetotransistor or a vertical Hall device as shown in Fig. 5.13 [12, 16]. However, magnetotransistors suffer from a large offset voltage resulting in poor absolute accuraccy for angle detection [27]. The vertical Hall device shows a strong cross-sensitivity due to an insufficient carrier path confinement [28]. In contrary, the vertical trench-Hall devices presented in *chapter 4* have excellent cross-sensitivity due to the thin active region defined by two parallel trenches. Furthermore, the device bears the potential for dynamic offset compensation by the spinning current technique for high absolute accuracy.

The packaging concept implies a sensor chip mounted on a pc-board by chip-on-board packaging [18]. The sensor die is protected by a globe-top [18].

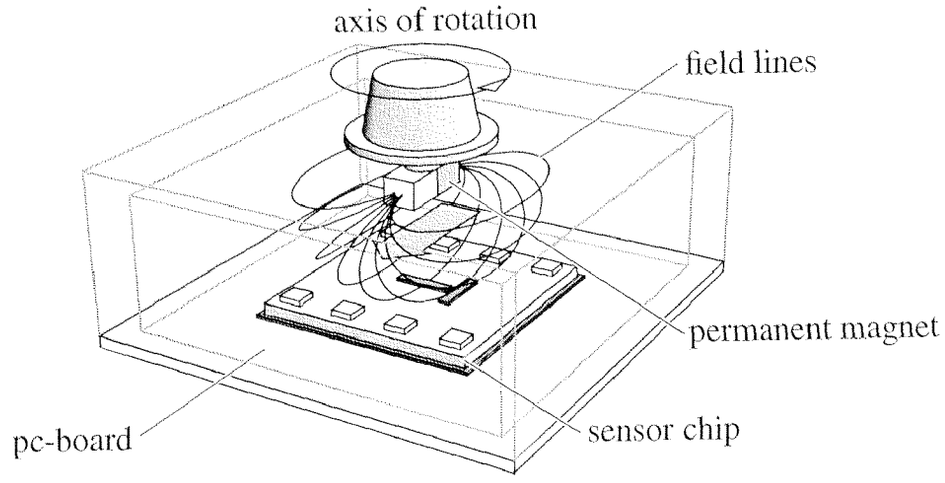


Fig. 5.13: Wear free angular detection system based on two orthogonally arranged vertical trench-Hall devices detecting the angular position of a permanent magnet.

The fixture for the permanent magnet can be realized by plastic molding and is snapped on the pc-board [29]. The approach meets the necessary requirements in terms of geometrical tolerances at a low price (see Figs. 5.13 and 5.14). The distance between permanent magnet and sensor ranges from 0.1 to 5 mm resulting in magnetic induction from 5 to 100 mT depending on the magnet [15].

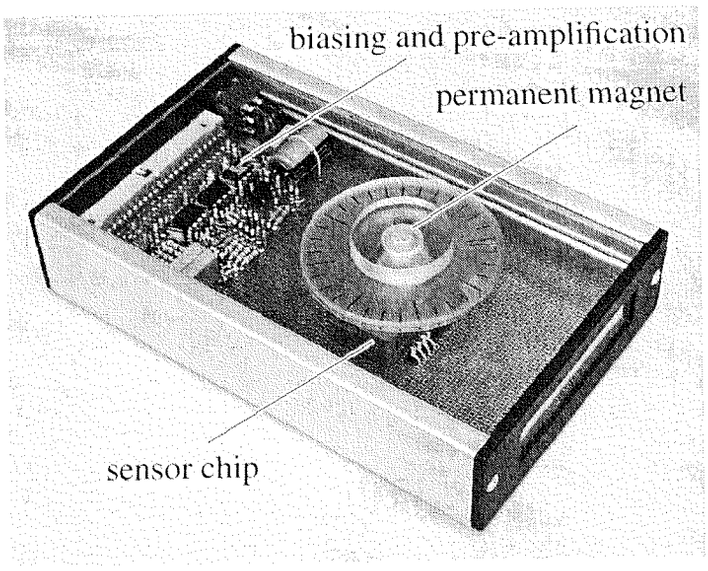


Fig. 5.14: Photograph of a wear free angle measurement system demonstrating its feasibility. The system is attached to a PC for signal read-out.

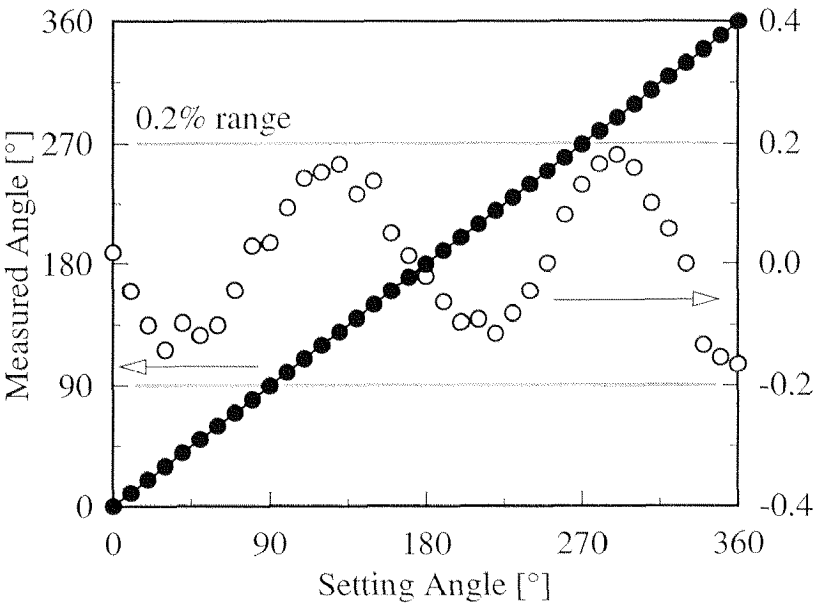


Fig. 5.15: Measured angle of the direction of magnetic induction versus the direction of the applied field. Neglecting offset voltages a resolution below 0.2° is achieved by applying a homogenous field of 0.3 T strength.

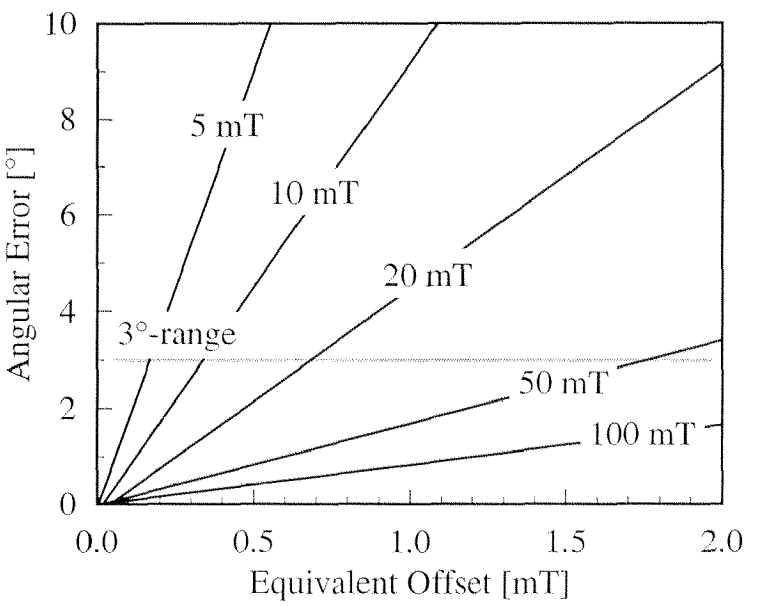


Fig. 5.16: Calculated angle measurement accuracy versus maximum equivalent offset for different magnitudes of applied magnetic induction [30].

An angle measured with two orthogonally arranged trench-Hall devices for the system mentioned above is shown in Fig. 5.15. The angle is calculated by an arc-tangent of the ratio of the two sensor responses. No correction of the sensor sensitivity was needed. Providing a homogenous magnetic field of 0.3 T and neglecting offset voltages a resolution below 0.2° is achieved. The limiting factor for the resolution is the signal to noise ratio of the sensor. Co-integrating the sensor and front-end electronics on the same CMOS chip is favorable for low noise amplification of the sensor signal. However, the electronics contributes noise itself which is, in general, higher than the sensor noise.

The absolute accuracy of the system depends on various properties. In terms of the sensing element the offset voltage causes the main contribution. For the non-optimized trench-Hall devices, an equivalent offset below 1 mT was measured [16]. This value can be further improved by mainly optimizing the fabrication technology. According to Fig. 5.16, considering a magnetic field strength of 100 mT this offset voltage results in an accuracy of approximately 1°. Nevertheless, specifications tend to accuracies below 1° with a 10 mT magnet requiring a maximum offset voltage in the 0.1 mT range.

Another limiting factor for the system accuracy are mechanical tolerances, and, therewith the homogeneity of the applied permanent magnet. In particular for small, low-cost magnets, poor homogeneity can cause a limitation of the accuracy in the range of several degrees.

To conclude, a compact CMOS monitor system for galvanically isolated current measurement is presented. It is packaged with standard lead-on-chip technology and completely in line with commercial IC production. This technology includes inexpensive and high volume batch fabrication of chips followed by automatic mass packaging. Furthermore, an accurate and inexpensive 2D-magnetic-sensor system in CMOS technology is demonstrated. Exploiting vertical trench-Hall devices enables co-integration of sensor and front-end circuitry on the same chip electrically insulated. The sensor bears the potential for being dynamic offset compensated by means of the spinning current, resulting in a high angular system accuracy.

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6 Conclusion and Outlook

6.1 Conclusion

The fabrication of microsystems utilizing standard IC technology exploits unique features such as cost effective batch fabrication, manufacturing with well established reliability, and use of dedicated design software. Moreover, in certain applications, like the cases considered in this thesis, appropriate packaging solutions are also available.

In this work, the theoretical background relevant to design Hall-based magnetic microsystems is presented. Two types of Hall devices are considered: the lateral Hall device sensitive to magnetic induction perpendicular to the chip surface, and the vertical trench-Hall device sensitive to fields parallel to the chip surface. A simple device model is introduced which allows the optimization of integrated Hall devices. The model predicts the input resistance, the common mode voltage at the device sense contacts, and the magnetic response of the sensor. These parameters are essential to the design of dedicated front-end electronics. Furthermore, offset compensation techniques are treated. Although, the double-Hall sensor offers a simple way to reduce the offset voltage, a more powerful method is based on the technique of spinning current. Theoretical and experimental results indicate that four phase spinning is sufficient to cancel the major source of offset induced by mechanical stresses. To avoid offset voltages introduced by non-linearities, a sensor layout with maximum possible symmetry is employed.

The sensors considered in this work are useful for applications involving magnetic induction in the range of 10 μT to 100 mT. For the lateral Hall device, the following general design attributes have been chosen:

- A Greek cross layout to achieve high signal linearity.
- An aspect ratio h/k = 10 μm/20 μm to 20 μm/20 μm, to yield high sensitivity at low input resistance.
- Shielding of the device with a gate-polysilicon layer to improve EMC.

Similarly for the vertical trench-Hall devices, the design attributes considered include:

- Placement of contacts on the chip surface or the use of a deep sense contact.
- A trench depth of 20 µm with thickness of the active region that is 2.4 µm.
- Shielding of the device with a polysilicon-filled trench for EMC.

An overview of performance figures of merit for the devices is given in Tab. 6.1.

Performance figures of merit	*Lateral Hall device*	*Vertical trench-Hall device*
direction of sensitivity	perpendicular	parallel
input resistance	2 to 6 kΩ	5 to 10 kΩ
sensitivity @ 1 mA bias	100 to 150 mV/T	250 to 300 mV/T
linearity	150 ppm @ ±0.3 T	0.1 ... 0.15% @ ±0.3 T
offset behavior	~ 10 µT (with spinning)	<1 mT (with spinning)
area consumption	50 x 50 to 80 x 80 μm^2	10 x 80 μm^2

Tab. 6.1 Performance figures of merit of lateral and vertical Hall devices.

The Hall devices presented here are used for bias field applications. This includes detection of magnetic induction generated by an electrical current or detection of position of an object attached to a permanent magnet. Two specific applications have been considered: a current monitor and a rotary switch. A summary of the key performance figures of merit is shown in Tab. 6.2. Although the current monitor has a limited accuracy, it is perfectly suited for security applications, such as detecting the presence of an electric current. Applications needing higher accuracy require field concentrators, however, this may not prove economically viable. In contrast, the requirements associated with the rotary switch can be met by the use of a vertical trench-Hall device. In particular, the in-plane *xy*-measurement of the magnetic field lowers the requirements of the field strength and of the field distribution of the permanent magnet, including associated mechanical tolerances. This is a critical issue for the overall system cost. The vertical trench-Hall device should be further optimized for low offset (< 100 µT), to make a significant impact on the market.

Performance figures of merit	*Current monitor*	*Rotary switch*
range	up to 20 A	360°
resolution	10 mA @ 2 Hz, 80 mA @ 100 Hz	0.1 to 0.5°
accuracy	50 mA @ 2 Hz, 150 mA @ 100 Hz	0.1 to 1.0° (with spinning current)[a]

a. in case of optimized remaining offset voltages

Tab. 6.2 Performance figures of merit of the considered applications.

Finally, a summary of results and their comparison to the state of the art is given:

- *Lateral Hall devices* of reduced area yield input resistances and sensitivities which are only limited by the CMOS process parameters. The devices exhibit outstanding linearity.
- *Vertical trench-Hall devices* show similar performance to lateral devices. Additionally, the yet unoptimized devices have very low cross-sensitivities and high linearity that only can be compared to magnetotransistors. Furthermore, the sensor can be offset compensated by the spinning current technique, where values in the mT-range have already been achieved.
- The *current monitor* combines low system cost with sufficient accuracy. It represents the first current monitor requiring only standard packaging techniques (lead-on-chip). A minimal distance between the current path and the sensor is achieved for high sensitivity. Therefore, no additional (field focussing) magnetic core, requiring hybrid packaging solutions, is needed.
- The *rotary switch* employs the vertical trench-Hall device. Therefore, the measurement principle does not pose stringent requirements on the permanent magnet and associated mechanical tolerances. Consequently, good resolution is achieved at low overall system cost.
- Finally, both applications are completely in line with CMOS-technology, and, therefore, allow co-integration of dedicated electronics on the same chip.

6.2 Outlook

The lateral Hall device should be introduced in a professional design library. Since dedicated front-end electronics, such as offset reduction by the spinning current technique, requires expert knowledge, only the building blocks for the sensor and electronics should be accessible to a general user. The needed device modeling can be based on the theory presented in this work.

However, future work on device optimization should be focussed on the vertical trench-Hall device. The already demonstrated performance holds sufficient promise, particularly, when combined with the possibility of offset reduction using the spinning current method. First, the associated CMOS technology has to be qualified to meet the reliability requirements of high volume fabrication. Next, a device model similar to the lateral Hall device has to be provided. Again, this offers the necessary building blocks for the sensor and dedicated front-end electronics to a large group of designers.

Further work on an approach using LOC packaging is recommended, for applications of a low-cost current monitor up to 20 A, with moderate accuracy requirements. However, this solution is viable only if a large quantity of systems are manufactured. Efforts should concentrate on issues related to packaging, i.e., long-term reliability and environmental test. The measurement principle should be based on a closed-loop approach utilizing on-chip compensation coils.

Finally, future work for the rotary switch is mainly limited to signal conditioning. The effort needed in extracting the angle of rotation from the sensor signal and subsequent AD-conversion should not be under estimated. As far as packaging is concerned, no serious issues are expected if plastic molded packaging is used.

APPENDICES

A.1 Basic Field Equations and Unit Conversions

The magnetic flux density or magnetic induction B is related to the magnetic field strength H as

$$B = \mu_0 \mu_r H, \tag{A.1}$$

where μ_r is the relative permeability and material dependent, and μ_0 the permeability in vacuum. The magnetic induction B in a material is the superposition of the external magnetic field strength H and the magnetization M

$$B = \mu_0 (H + M). \tag{A.2}$$

The relation between the magnetization M and the magnetic field strength H is given by

$$M = \chi_m H, \tag{A.3}$$

using the magnetic susceptibility χ_m. The corresponding units in the *SI*- and *cgs*-system of above properties are given in Tab. A.1.

property	*SI-unit*	*cgs-unit*	*conversion*
B	T (tesla)	G (gauss)	$1\ T = 1\ Vs/m^2 = 10^4\ G$
H	A/m	Oe (oersted)	$1\ A/m = 4\pi \cdot 10^{-3}$ Oe
M	A/m	Oe	$1\ A/m = 4\pi \cdot 10^{-3}$ Oe
μ_0	T/Am	G/Oe	$4\pi \cdot 10^{-7}$ T/Am = 1 G/Oe[a]
μ_r	-	-	-
χ_m	-	-	-

a. 1 G = 1 Oe in free air ($\mu_r = 1$)

Tab. A.1 Useful conversion units of magnetic properties.

A.2 List of Symbols

β	[-]	Numerical Non-Linearity Coefficient
γ	[-]	Material Non-Linearity Coefficient
ε	[-]	Dielectric Constant
ε_0	[F/cm]	Permittivity in Vacuum
ε_S	[-]	Dielectric Constant of Silicon x ε_0
λ	[-]	Correction Factor Doping Profile
λ_n	[-]	Phase Angle
μ_n	[cm^2/Vs]	Electron Mobility
μ_p	[cm^2/Vs]	Hole Mobility
μ_0	[H/cm]	Permeability in Vacuum
μ_{Hn}	[cm^2/Vs]	Hall Mobility for Electrons
μ_{H0n}	[cm^2/Vs]	Hall Mobility at Zero Induction
$\pi_{\alpha\beta}$	[Pa^{-1}]	Piezoresistive Coefficients
ρ	[Ω/m]	Resistivity
$\bar{\rho}$	[Ω cm]	Mean Hydrostatic Unstressed Resistivity
ρ_α^0	[Ω cm]	Resistivity Stress Free Material
σ_β	[Pa]	Mechanical Stress
σ_{Bn}	[Ω^{-1} cm^{-1}]	Effective Conductivity of Electrons
σ_0	[Ω^{-1} cm^{-1}]	Conductivity of Electrons
τ	[s]	Relaxation Time
τ_p	[s]	Hole Relaxation Time
ϑ	[-]	Contact Opening Angle
ϕ	[V]	Electric Field
φ	[-]	Switching Angle
ω_c	[s^{-1}]	Cyclotron Frequency
Θ_H	[-]	Deflection Angle, Hall Angle
Φ	[cm^{-2}]	Ion Dose
A_i	[V]	Fourier Components of Offset Voltage
B	[T]	Magnetic Induction
B_i	[V]	Fourier Components of Restive Voltage
B_I	[T/A]	Magnetic Induction per Unit Current
D	[cm^2/s]	Diffusion Constant
Δd	[m]	Geometric Deflection

e	[C]	Electron Charge
E	[V/m]	Electric Field
E_a	[V/m]	Applied Electric Field
E_H	[V/m]	Hall Electric Field
Erf(x)	[-]	Error Function
f	[Hz]	Frequency
Δf	[Hz]	Bandwidth
F	[N]	Mechanical Force
F_H	[N]	Hall Force
F_L	[N]	Lorentz Force
G_R	[-]	Resistive Correction Factor
G_S	[-]	Sensitivity Correction Factor
h	[µm]	Length Side Arm Greek Cross Hall Devices
I	[A]	Electric Current
I_{ij}	[V]	Contact Current at Contact i and j
J_n	[A/m^2]	Electron Current Density
J_p	[A/m^2]	Hole Current Density
k	[J/K]	Boltzmann Constant
k	[µm]	Width Side Arm Greek Cross Hall Devices
$K_{1,2,3}$	[-]	Kinetic Coefficient
K(m^2)	[-]	Complete Elliptic Integral
kT	[eV]	Thermal Energy
m_0	[kg]	Rest Mass Electron
m^*	[kg]	Effective Mass
n	[cm^{-3}]	Electron Carrier Density
n_i	[cm^{-3}]	Intrinsic Carrier Concentration
N_A	[cm^{-3}]	Acceptor Carrier Concentration
N_C	[cm^{-3}]	Eff. Density of States (Conduction Band)
N_D	[cm^{-3}]	Donor Carrier Concentration
N_V	[cm^{-3}]	Eff. Density of States (Valence Band)
NL_G	[-]	Geometrical Non-Linearity
NL_M	[-]	Material Non-Linearity
NL_W	[T/√Hz]	Noise Level
p	[cm^{-3}]	Hole Carrier Density
p_0	[cm^{-3}]	Equilibrium Hole Carrier Density
p_0	[cm^{-3}]	Background Doping Concentration

p_p	[cm^{-3}]	Peak Doping Concentration
q	[C]	Electrical Charge
r_m	[-]	Scattering Factor
r_H	[-]	Hall Scattering Factor
R	[Ω]	Resistance
R_H	[cm^3/As]	Hall coefficient
R_{H0}	[cm^3/As]	Hall coefficient at Zero Induction
R_{Hn}	[cm^3/As]	Hall coefficient Including Scattering
R_p	[m]	Projected Range
ΔR_p	[m]	Projected Straggle
RF_{nplus}	[µm]	Reduction value n^+-Layer
RF_{nwell}	[µm]	Reduction value n-well
s, ds	[m]	Integral path
sn(u, v)	[-]	Jacobian Integral Function
S_a	[V/T]	Absolute Sensitivity
S_I	[V/AT]	Current Related Sensitivity
S_P	[1/AT]	Power Sensitivity
S_V	[1/T]	Voltage Related Sensitivity
T	[°C, K]	Temperature
t_p	[m]	Depth Abrupt Junction Profile
v	[m/s]	Charge Velocity
v_n	[m/s]	Drift Velocity of Electrons
V_{bi}	[V]	Built-in Voltage
V_H	[V]	Hall Voltage
$V_{H,O}$	[V]	Superposition of Hall And Offset Voltage
V_{ij}	[V]	Contact Voltage at Contact i and j
V_O	[V]	Offset Voltage
V_R	[V]	Resistive Voltage
$V_{R,O}$	[V]	Superposition of Resistive And Offset Voltage
V_{ref}	[V]	Reference Voltage
V_{sub}	[V]	Substrate Voltage
x_n (V)	[m]	Depletion Layer Thickness n-Region
x_p (V)	[m]	Depletion Layer Thickness p-Region

A.3 Physical Constants

ε_0		[As/Vm]	$8.85418 \cdot 10^{-12}$	Permittivity in Vacuum
ε_{Si}		[-]	11.9	Dielectric Const. Silicon
μ_0		[Vs/Am]	$4\pi \cdot 10^{-7}$	Permeability in Vacuum
μ_n	(Si)	[cm^2/Vs]	1500	Electron Mobility
μ_p	(Si)	[cm^2/Vs]	450	Hole Mobility
eV		[J]	$1.60218 \cdot 10^{-19}$	Electron Volt
E_g	(Si)	[eV]	1.12	Bandgap at 300K
k		[J/K]	$1.3807 \cdot 10^{-23}$	Boltzmann Constant
kT/q		[V]	0.0259	Thermal Voltage at 300K
m_0		[kg]	$9.1094 \cdot 10^{-31}$	Rest Mass Electron
m^*	(Si)	[kg]	$0.98 / 0.19 \cdot m_0$	Effective Mass
n_i	(Si)	[cm^{-3}]	$1.45 \cdot 10^{10}$	Intrinsic Carrier Concentration
N_C	(Si)	[cm^{-3}]	$2.80 \cdot 10^{19}$	Eff. Dens. of Stat. (Cond. Bd.)
N_V	(Si)	[cm^{-3}]	$1.04 \cdot 10^{19}$	Eff. Dens. of Stat. (Val. Bd.)
q		[C]	$1.60218 \cdot 10^{-19}$	Electrical Charge
r_H	(Si)	[-]	1.17	Hall Scattering Factor

A.4 List of Abbreviations

ASIC	Application Specific Integrated Circuit
BPSG	Boro Phospho Silicate Glass
CAD	Computer Aided Design
CYE, CXE	2 µm CMOS processes of Austria Mikro Systeme Int. AG.
CMOS	Complementary Metal Oxide Semiconductor
DRAM	Dynamic Random Access Memory
EDP	Ethylene-Diamine Pyrocatechol
EMC	Electromagnetic Compatibility
ESD	Electrostatic Discharge
FEM	Finite Element Modeling
IC	Integrated Circuit
JFET	Junction Field Effect Transistor
KOH	Potassium Hydroxide
LOC	Lead On Chip
LOCOS	Local Oxidation
LPCVD	Low Pressure Chemical Vapor Deposition
MEMS	Micro Electro Mechanical System
MOS	Metal Oxide Semiconductor
PCB	Printed Circuit Board
PECVD	Plasma Enhanced Chemical Vapor Deposition
PMMA	Polymethyl-Methacrylat
PSG	Phospho Silicate Glass
RIE	Reactive Ion Etching
SIMS	Secondary-Ion Mass Spectrometry
SOI	Silicon On Insulator
SOG	Spin On Glass
SOS	Silicon On Sapphire
TEOS	Tetraethylorthosilicate
ULSI	Ultra Large Scale Integration
VLSI	Very Large Scale Integration

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