C-DIAS Frequency Measuring Card CFC 051

This universal counter card has a counter input and SSI (Serial Synchronous Interface) input.
The counter has a 32-bit range and can be used as a frequency sensor as well as a counter.
With the software, the 5 channels can be configured either as a counter or an SSI connection. The SSI connection is designed for the SSI sensor (i.e.: angle encoder, Length measuring). Non-coded and gray code generators are supported (gray code is converted to binary internally).

Technical Data

Counter Specification

Number of channel	5 counter inputs (or SSI)	
Counter range	32 Bit	
Counter frequency	64 MHz internal 5 MHz external	
Time base precision	Quartz-Frequency stability: ±100 ppm, aging: ±5 ppm p.a.	
Signal level	RS422 Input: 150 Ohm Bus termination, each 1,2 kOhm spreading against +5 Volt and ground	
Prescaler	16 Bit, Software configurable	
Impulse suppression	12 Bit counter with 125 kHz, Software configurable (0 – 32,75 ms in 8 µs-steps)	
Configuration	Up/Down	Per Software
	Enable	Per Software
	Load	Per Software
	Flank	Per Software
	Counter source	Per Software
Inputs	5 Inputs, optional as counter or SSI-Data input.	
Reference counter	Internal counter with programmable prescaler. When the counter of the corresponding channels increments, the reference counter is stored.	

SSI Sensor Specification

Number of channels	5 SSI (or counter)
Signal level SSI	RS422 Input: 150 Ohm Bus termination, each 1,2 kOhm spreading against +5 Volt and ground Outputs: without spreading or Bus termination
Shift register frequency	125 kHz – 1 MHz
Shift register length	Maximum 32 Bit
Signal evaluation	Gray code or binary

Electrical requirements

Supply voltage +24 V DC (input) [1)]	22 – 29,5 V DC (this voltage is monitored for availability)	
Current consumption supply+24 V DC (Input)	Depending on the power consumption of the connected modules	Maximum 1 A
+24 V out	+24 V +20 / -15 % (20,4 V ... 28,8 V)	
Load capacity +24 V-out-supply	Maximum 200 mA per channel	
Supply form C-DIAS-Bus	+5 V	
Current consumption of C-DIAS Bus (+5 V-supply)	Typically 250 mA	Maximal 400 mA

IMPORTANT:

This module exceeds the standard current consumption for C-DIAS modules!
(+5V: 150mA and +24V: 150mA)

In case this C-DIAS module is mounted on an 8x module carrier (CMB 08x), the total current of the modules used must be determined and tested.
The specification for the current consumption is found in the module specific technical document under “Electrical Requirements”
The total current of the +5V supply cannot exceed 1.2A (150mA/slot).
This also applies to the total current of the +24V supply, which cannot exceed 1.2A (150mA/slot).

IMPORTANT:
La consommation de courant de ce module dépasse les valeurs typiques pour les modules C-DIAS! (+5 V: 150 mA et +24 V: 150mA)
Si ce module C-DIAS est monté sur un fond de panier de taille 8 (CMB 08x), le courant total des modules utilisés doit être déterminé et vérifié.
Les données de la consommation de courant sont mentionnées dans la documentation technique du module respectif dans le paragraphe "Spécifications électriques"
Le courant total de l'alimentation +5 V ne peut pas dépasser 1,2A (150mA/module).
Cela vaut également pour le courant total de l'alimentation +24 V, lequel ne peut également pas dépasser 1,2A (150mA/module).

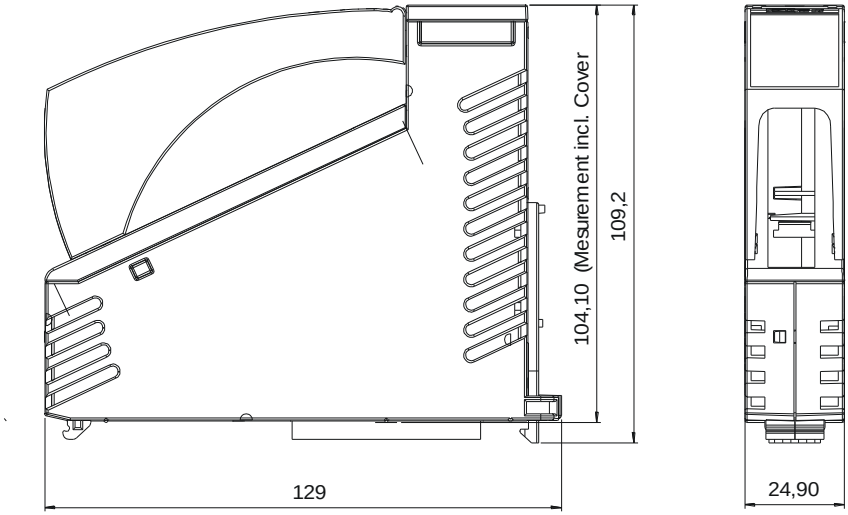
Miscellaneous

Article number	12-074-051		
Module identification of DIAS-Bus	Yes		
Module identification with EEPROM	**Address**	**Data**	**Description**
	$00	$xx	Checksum
	$01	123	Identification
	$02	26	Module group
	$03	2	Variant
	$04	5	Number of channels
	$05	$10	Hardware version $10 = HW-V1.0, …
	$10		Serial number
Software macro	LASAL / Class => CFC051_IM		
Hardware version	1.x - 2.x		
Standardization	UL (E247993)		

Operating conditions

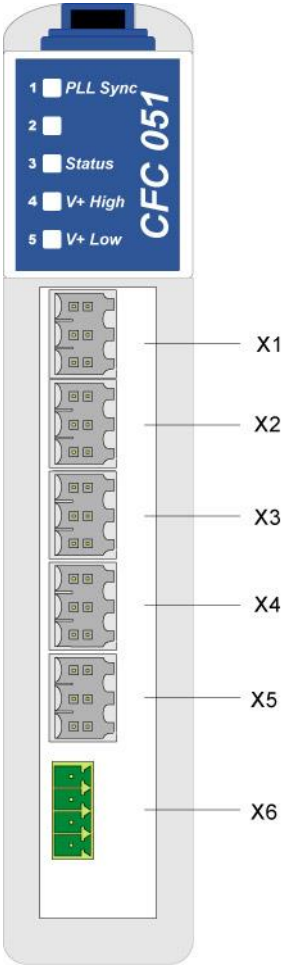
Storage temperature	-20 – +85 °C	
Operating temperature	0 – +60 °C	
Humidity	0 – 95 %, uncondensed	
EMV-stability	Per EN 61000-6-2 (Industrial area)	
Shock resistance	EN 60068-2-27	150 m/s²
Protection type	EN 60529	IP 20

Mechanical Dimensions

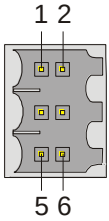


Terminal Assignments

The connection of the SSI sensor or counter is made with the help of five 6-pin connectors (X1 - X5). The supply voltage and supply ground are connected using a 4-pin plug (X6). Each channel has 6 terminal contacts, 4 for the signal lines and 2 for the senor supply.

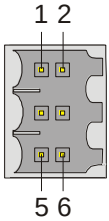


X1:



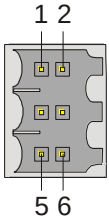
Pin	Assignment: Coun-	Assignment: SSI
1	n.c.	Serial Clock -
2	n.c.	Serial Clock +
3	counter 1 -	Serial Data -
4	counter 1 +	Serial Data +
5	GND	GND
6	+24 V-AUS	+24 V-AUS

X2:



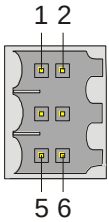
Pin	Assignment: Coun-ter	Assignment: SSI
1	n.c.	Serial Clock -
2	n.c.	Serial Clock +
3	counter 2 -	Serial Data -
4	counter 2 +	Serial Data +
5	GND	GND
6	+24 V-AUS	+24 V-AUS

X3:



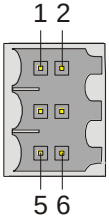
Pin	Assignment: Counter	Assignment: SSI
1	n.c.	Serial Clock -
2	n.c.	Serial Clock +
3	counter 3 -	Serial Data -
4	counter 3 +	Serial Data +
5	GND	GND
6	+24 V-AUS	+24 V-AUS

X4:



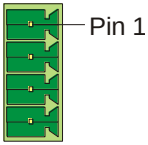
Pin	Assignment: Counter	Assignment: SSI
1	n.c.	Serial Clock -
2	n.c.	Serial Clock +
3	counter 4 -	Serial Data -
4	counter 4 +	Serial Data +
5	GND	GND
6	+24 V-AUS	+24 V-AUS

X5:



Pin	Assignment: Counter	Assignment: SSI
1	n.c.	Serial Clock -
2	n.c.	Serial Clock +
3	counter 5 -	Serial Data -
4	counter 5 +	Serial Data +
5	GND	GND
6	+24 V-AUS	+24 V-AUS

X6:



Pin	Assignment
1	+24 V
2	+24 V
3	GND
4	GND

Applicable connectors

X1-X5: 6-pol. Weidmüller connector B2L/B2CF 3,5/6

X6: **plug connector with spring terminal:**
Phoenix Contact: FK-MCP 1,5/ 4-ST-3,5

Plug connector with Screw terminal:
Phoenix Contact: MC 1,5/ 4-ST-3,5

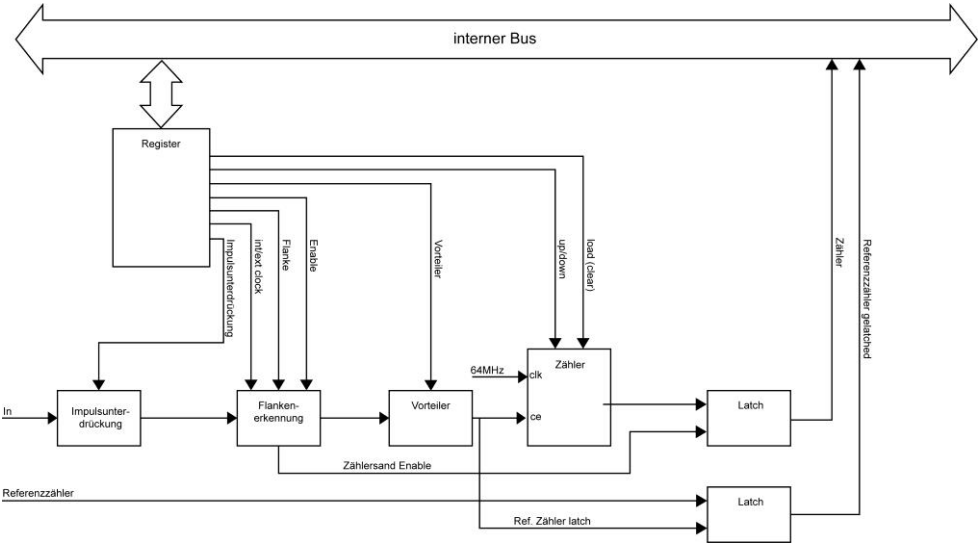
The complete C-DIAS connector set CKL 081 with spring terminals is available at Sigmatek under the article number 12-600-081.

Status Display

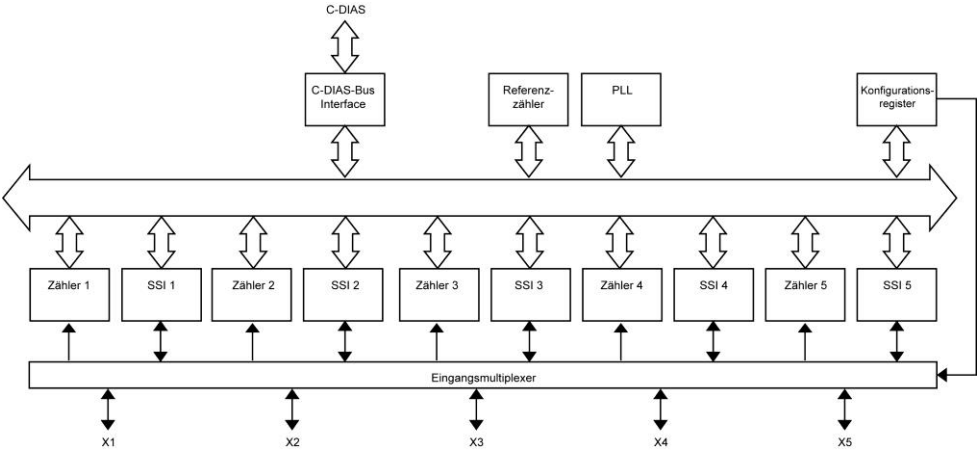
LED Nr.	LED color	meaning
1	green	Sync
2	---	Not used
3	red	Status
4	red	+24 V High Level Error (>+28,8 V)
5	red	+24 V Low Level Error (<+20,4 V)

Function

Block diagram of a counter:



Block diagram FPGA:



Measurement Modes

All 5 channels are user defined and independently configurable in the various modes of measurement. In the counter mode, the common reference counter allows time phase relationships to be established between input signals of several channels.
A fully configurable digital low pass filter (register " configuration impulse suppression") can be use to suppress disruptive signals. The default setting of the filter is 0 (off). With the corresponding configuration it can be set from 0 to 32.75 ms with an 8µs resolution.

- Counter Mode
  - Period duration measurement for slow signals
  - Pulse width measurement
  - Period duration measurement for fast signals
  - Universal counter (Pulse counter)

- SSI-sensor interface Mode
  - Binary mode
  - Gray code Decoder mode

Period Duration Measurement for "Slow" Signals

In the channel configuration register, the counter mode is selected (default setting). In the counter configuration register, the clock and edge recognition are set and the count direction is set to Up. Finally, the period duration measurement with the reference point as positive edge or negative edge is enabled. The difference being the stored reference point of the last recognized edge (rising or falling) at a given time is used, for example, for the phase comparison between several channels. By setting the enable bit in the channel register as well as that of the reference counter, the measurement is started

The result of the measurement is stored in the count value register of the channel as a 32-bit value with resolution of 15.625 ns (time base, 64 MHz). As long as the counter load value is set to 0 (default), it must be kept in mind that in the software, the counter value is incremented by 1 in the calculation for the period and/or signal frequency! The above mentioned quartz time base allows, for example, a 640 kHz signal to be measured with a resolution of ± 1%.
In addition to the phase comparison, each reference counter values stored in a channel (including 32 bit values with a 15.625 ns resolution (64 MHz time base)) gives information on the availability of new measurement values.

Pulse Width Measurement

In the channel configuration register, the counter mode is selected (default setting). In the counter configuration register, the clock and edge recognition are set and the count direction is set to Up. Finally, the measurement for the high time or low time of a given square wave signal is enabled. The stored reference time, which is used for phase comparison between channels for example, is the last rising edge measured on the low-time measurement and/or falling edge of the of the high-time measurement. By setting the enable bit in the channel register as well as that of the reference counter, the measurement is started.

The result of the measurement is stored in the count value register as 32-bit value with a resolution of 15.625 ns (64 MHz time base).
As long as the counter load value is set to 0 (default), it must be kept in mind that in the software, the counter value is incremented by 1 in the calculation for high and/or low time! In addition to the described phase comparison, each reference counter value stored in a channel (including 32 bit values with a 15.625 ns resolution (64 MHz time base)) gives information on the availability of new measurement values.

Period Measurement for "Fast" Signals

The period and/or frequency measurement for fast signals is based on a gate time measurement (the signal impulses divided by the measured time). In the channel configuration register, the counter mode is selected (default setting). In the counter configuration register, the clock and edge analysis are set and the count direction is set to Up. The two flank evaluation doubles the resolution of the measurement.

The stored reference time, which is used for phase comparison between channels for example, is the last measured rising or falling edge at any given time (depending on the configuration of the edge analysis). By setting the enable bit in the channel register as well as that of the reference counter, the measurement is started.

The result of the number of measured pulses is stored as a 32-bit value in the number value register of the channel. The corresponding reference value is stored in the reference number register. The result of the period and/or frequency measurement allows the difference between the actual and previous values as well as the actual and previous reference values to be calculated.
The gate time results from the timed intervals of the selected double values. The reference counter value from the measuring channel is latched during the time it's being read whereby consistent data is actualized. The jitter at the time data is read therefore does not falsify measurement values.

Universal Counter (pulse counter)

In the channel configuration register, the counter mode is selected (default setting). In the counter configuration register, the external clock can be configured to increment or decrement depending on the application. It can be set to any given loading value, starting from the current counter value and then be incremented or decremented directly. Using Enable starting or stopping is possible at any time.

The configurable prescaler enables the counter to increment and/or decrement at every n^{th} pulse (n = 1 to 65535; 0 = 65536). The reference counter is also equipped with a configurable prescaler It should be kept in mind, however, that the prescaler setting affects the reference counter register on all channels.
For exact synchronization of the counter values over several channels, the counter and latches can be set to hold on all channels (see register 16#F7). This hinders the counters for the various channels from changing while the necessary data is being read after which; the latches are re-enabled.

SSI Sensor Interface

In the configuration register, SSI mode is selected. In the register “SSI shift register length”, the total length of the specified bit stream through the SSI sensor (SSI data, including add bits such as overflow, power failure, etc..) is entered. For the SSI shift register frequency, and gray code decoding, the desired clock rate (to select the clock rate, see the SSI sensor data sheet) is set).
The cyclic reading of the SSI sensor is started through the bit, SSI start, in the channel configuration register. It should be kept in mind that the clock rate is multiplied with the shift register length and added in order that the sensor time t_m is as short as possible. The interface logic hinders the new SSI cycle from being started before the previous cycle is completed (the SSI status bit indicates whether a cycle is currently active or not). In addition, the maximum rate of measurement must be accounted for and depending on the effect (false or old values are read, sensor is synchronized..), the measurement rate should not be exceeded.

To start a new SSI frame, SSI start must be set to 1. Then the SSI frame is started with the next cycle (the cycle time is set through the sub millisecond counter), as long as the previous frame is finished. The SSI start is reset automatically, which means the start process must take place explicitly for each desired cycle.
For a flexible adaptation to the measurement reader, the SSI read cycles can be started individually using the PLL configuration register and PLL counter configuration register.

Binary Mode

For the binary mode, the gray code decoding (default on) must be deactivated. This mode is also recommended if the sensor supplies data in Gray code but contains additional un-coded bits, which when automatically decoded leads to the falsification of the total result. The decoding must be done in the software. The de-serialized data stream is stored as a 32-bit value in the SSI data register.

Gray code Decoder Mode

For sensors, which supply gray coded data, the result is automatically decoded (Gray code decoding on) and stored as a 32-bit value in the SSI data register. In this mode, the add bits must be allowed for in the sensor data stream. Un-coded add bits transferred in the serial data stream before or after coded measurement data falsify the decoding of the collected data.

Addressing

REFERENCE COUNTER

Address	Access		Function
16#00..16#03	READ	DOUBLE	**Reference counter – count value** Bit 0...31 actual count value
16#00..16#03	WRITE	DOUBLE	**Reference counter – Load value** Bit 0...31 Preset counter value (Default = 0, transferred with Load)
16#04..16#07			**Reserved**
16#08..16#09	READ/ WRITE	WORD	**Reference counter – Configuration prescaler** Bit 0...15 prescaler value
16#0A..16#0B			**Reserved**
16#0C	READ/ WRITE	BYTE	**Reference counter – Configuration** Bit 0 Direction: Up =1 / Down = 0 Bit 1 Enable: counter Start = 1 / counter Stop = 0 Bit 2 Load: new load value = 1 Bit 3..7 reserved
16#0D..16#0F			**Reserved**

CHANNEL 1

Address	Access		Function
16#10..16#13	READ	DOUBLE	**Channel 1 – Counter value (counter mode) / SSI-Data (SSI-Mode)** Bit 0...31 actual counter value and/or. SSI serial data
16#10..16#13	WRITE	DOUBLE	**Channel 1 – Counter - load value** Bit 0...31 new count value transferred with load (Default = 0, equals Clear Function)
16#14..16#17	READ	DOUBLE	**Channel 1 – Reference counter** Bit 0...31 stored Reference counter value
16#18..16#19	READ/ WRITE	WORD	**Channel 1 – Configuration Prescaler** Bit 0...15 Prescaler value (Default: 1; 0 not allowed!)
16#1A..16#1B	READ/ WRITE	WORD	**Channel 1 – Configuration Impulse suppression** Bit 0...11 Impulse suppression time (Impulses, which are smaller than the adjusted time, are filtered) (Set value * 8 µs corresponds to the filter time) (Default = 0; valid value range 0 … 4094, 4095 not allowed!)
16#1C	READ/ WRITE	BYTE	**Channel 1 – counter - Configuration** Bit 0 Direction: Up = 1 / Down = 0 Bit 1 Enable (Reference counter must also be enabled) counter Start = 1 / counter Stop = 0 Bit 2 Load: new load value = 1 Bit 3 clock: internal = 0 / external = 1 Bit 4...5 Flanks Internal clock 00: rising to falling Flank – low 01: falling to falling Flank – Period duration 10: rising to rising Flank – Period duration 11: rising to falling Flank– high External clock 00, 11: two flank analysis 01: single flank analysis (falling Flank) 10: single flank analysis (rising Flank) Bit 6...7 reserved
16#1D	READ/ WRITE	BYTE	**Channel 1 – SSI-shift register length** Bit 0...5 shift register length

16#1E	READ/ WRITE	BYTE	**Channel 1 – SSI-Shift register frequency and Gray code Decoding** Bit 0...1 shift register frequency 00: 125 kHz 01: 250 kHz 10: 500 kHz 11: 1 MHz Bit 2 Gray code Decoding 0: off 1: on
16#1F	READ	BYTE	**Channel 1 – Channel Configuration and SSI-Status** Bit 0: channel mode 0 .. counter 1 .. SSI Bit 1: SSI-Status 0 .. SSI ready (Data valid) 1 .. SSI busy
16#1F	WRITE	BYTE	**Channel 1 – Channel configuration and SSI-Status** Bit 0: channel mode 0 .. Counter 1 .. SSI Bit 1: SSI Start 1 .. SSI start (Frame started with next sync)

CHANNEL 2

Address	Access		Function
16#20..16#23	READ	DOUBLE	**Channel 2 – Counter value (Counter mode) / SSI-Data (SSI-Mode)** Bit 0...31 actual counter value and/or SSI serial data
16#20..16#23	WRITE	DOUBLE	**Channel 2 –** counter **– load value** Bit 0...31 new count value transferred with load (Default = 0, equals Clear Function)
16#24..16#27	READ	DOUBLE	**Channel 2 – Reference counter** Bit 0...31 stored Reference counter value
16#28..16#29	READ/ WRITE	WORD	**Channel 2 – Configuration Prescaler** Bit 0...15 Prescaler value (Default: 1; 0 not allowed!)
16#2A..16#2B	READ/ WRITE	WORD	**Channel 2 – Configuration Impulse suppression** Bit 0...11 Impulse suppression time (Impulses, which are smaller than the adjusted time, are filtered) (Set value * 8 µs corresponds to the filter time) (Default = 0; valid value range 0 … 4094, 4095 not allowed!)
16#2C	READ/ WRITE	BYTE	**Channel 2 – counter - Configuration** Bit 0 Direction: Up = 1 / Down = 0 Bit 1 Enable (Reference counter must also be enabled) counter Start = 1 / counter Stop = 0 Bit 2 Load: new load value = 1 Bit 3 clock: internal = 0 / external = 1 Bit 4...5 Flanks Internal clock 00: rising to falling Flank – low 01: falling to falling Flank – Period duration 10: rising to rising Flank – Period duration 11: rising to falling Flank– high External clock 00, 11: two flank analysis 01: single flank analysis (falling Flank) 10: single flank analysis (rising Flank) Bit 6...7 reserved
16#2D	READ/ WRITE	BYTE	**Channel 2 – SSI-shift register length** Bit 0...5 shift register length

16#2E	READ/ WRITE	BYTE	**Channel 2 – SSI-Shift register frequency and Gray code Decoding** Bit 0...1 shift register frequency 00: 125 kHz 01: 250 kHz 10: 500 kHz 11: 1 MHz Bit 2 Graycode Decoding 0: off 1: on
16#2F	READ	BYTE	**Channel 2– Channel Configuration and SSI-Status** Bit 0: channel mode 0 .. counter 1 .. SSI Bit 1: SSI-Status 0 .. SSI ready (Data valid) 1 .. SSI busy
16#2F	WRITE	BYTE	**Channel 2 – Channel configuration and SSI-Status** Bit 0: channel mode 0 .. counter 1 .. SSI Bit 1: SSI Start 1 .. SSI start (Frame started with next sync)

CHANNEL 3

Address	Access		Function
16#30..16#33	READ	DOUBLE	**Channel 3 – Counter value (Counter mode) / SSI-Data (SSI-Mode)** Bit 0...31 actual counter value and/or SSI serial data
16#30..16#33	WRITE	DOUBLE	**Channel 3 –** counter **– load value** Bit 0...31 new count value transferred with load (Default = 0, equals Clear Function)
16#34..16#37	READ	DOUBLE	**Channel 3 – Reference counter** Bit 0...31 stored Reference counter value
16#38..16#39	READ/ WRITE	WORD	**Channel 3 – Configuration Prescaler** Bit 0...15 Prescaler value (Default: 1; 0 not allowed!)
16#3A..16#3B	READ/ WRITE	WORD	**Channel 3 – Configuration Impulse suppression** Bit 0...11 Impulse suppression time (Impulses, which are smaller than the adjusted time, are filtered) (Set value * 8 µs corresponds to the filter time) (Default = 0; valid value range 0 … 4094, 4095 not allowed!)
16#3C	READ/ WRITE	BYTE	**Channel 3 – counter - Configuration** Bit 0 Direction: Up = 1 / Down = 0 Bit 1 Enable (Reference counter must also be enabled) counter Start = 1 / counter Stop = 0 Bit 2 Load: new load value = 1 Bit 3 clock: internal = 0 / external = 1 Bit 4...5 Flanks Internal clock 00: rising to falling Flank – low 01: falling to falling Flank – Period duration 10: rising to rising Flank – Period duration 11: rising to falling Flank– high External clock 00, 11: two flank analysis 01: single flank analysis (falling Flank) 10: single flank analysis (rising Flank) Bit 6...7 reserved
16#3D	READ/ WRITE	BYTE	**Channel 3 – SSI-shift register length** Bit 0...5 shift register length

16#3E	READ/ WRITE	BYTE	**Channel 3 – SSI-Shift register frequency and Gray code Decoding** Bit 0...1 shift register frequency 00: 125 kHz 01: 250 kHz 10: 500 kHz 11: 1 MHz Bit 2 Gray code Decoding 0: off 1: on
16#3F	READ	BYTE	**Channel 3 – Channel Configuration and SSI-Status** Bit 0: channel mode 0 .. counter 1 .. SSI Bit 1: SSI-Status 0 .. SSI ready (Data valid) 1 .. SSI busy
16#3F	WRITE	BYTE	**Channel 3 – Channel configuration and SSI-Status** Bit 0: channel mode 0 .. counter 1 .. SSI Bit 1: SSI Start 1 .. SSI start (Frame started with next sync)

CHANNEL 4

Address	Access		Function
16#40..16#43	READ	DOUBLE	**Channel 4 – Counter value (Counter mode) / SSI-Data (SSI-Mode)** Bit 0...31 actual counter value and/or SSI serial data
16#40..16#43	WRITE	DOUBLE	**Channel 4 –** counter **– load value** Bit 0...31 new count value transferred with load (Default = 0, equals Clear Function)
16#44..16#47	READ	DOUBLE	**Channel 4 – Reference counter** Bit 0...31 stored Reference counter value
16#48..16#49	READ/ WRITE	WORD	**Channel 4 – Configuration Prescaler** Bit 0...15 Prescaler value (Default: 1; 0 not allowed!)
16#4A..16#4B	READ/ WRITE	WORD	**Channel 4 – Configuration Impulse suppression** Bit 0...11 Impulse suppression time (Impulses, which are smaller than the adjusted time, are filtered) (Set value * 8 µs corresponds to the filter time) (Default = 0; valid value range 0 … 4094, 4095 not allowed!)
16#4C	READ/ WRITE	BYTE	**Channel 4 – counter - Configuration** Bit 0 Direction: Up = 1 / Down = 0 Bit 1 Enable (Reference counter must also be enabled) counter Start = 1 / counter Stop = 0 Bit 2 Load: new load value = 1 Bit 3 clock: internal = 0 / external = 1 Bit 4...5 Flanks Internal clock 00: rising to falling Flank – low 01: falling to falling Flank – Period duration 10: rising to rising Flank – Period duration 11: rising to falling Flank– high External clock 00, 11: two flank analysis 01: single flank analysis (falling Flank) 10: single flank analysis (rising Flank) Bit 6...7 reserved
16#4D	READ/ WRITE	BYTE	**Channel 4 – SSI-shift register length** Bit 0...5 shift register length

16#4E	READ/ WRITE	BYTE	**Channel 4 – SSI-Shift register frequency and Gray code Decoding** Bit 0...1 shift register frequency 00: 125 kHz 01: 250 kHz 10: 500 kHz 11: 1 MHz Bit 2 Gray code Decoding 0: off 1: on
16#4F	READ	BYTE	**Channel 4 – Channel Configuration and SSI-Status** Bit 0: channel mode 0 .. counter 1 .. SSI Bit 1: SSI-Status 0 .. SSI ready (Data valid) 1 .. SSI busy
16#4F	WRITE	BYTE	**Channel 4 – Channel configuration and SSI-Status** Bit 0: channel mode 0 .. counter 1 .. SSI Bit 1: SSI Start 1 .. SSI start (Frame started with next sync)

CHANNEL 5

Address	Access		Function
16#50..16#53	READ	DOUBLE	**Channel 5– Counter value (Counter mode) / SSI-Data (SSI-Mode)** Bit 0...31 actual counter value and/or SSI serial data
16#50..16#53	WRITE	DOUBLE	**Channel 5–** counter **– load value** Bit 0...31 new count value transferred with load (Default = 0, equals Clear Function)
16#54..16#57	READ	DOUBLE	**Channel 5– Reference counter** Bit 0...31 stored Reference counter value
16#58..16#59	READ/ WRITE	WORD	**Channel 5– Configuration Prescaler** Bit 0...15 Prescaler value (Default: 1; 0 not allowed!)
16#5A..16#5B	READ/ WRITE	WORD	**Channel 5– Configuration Impulse suppression** Bit 0...11 Impulse suppression time (Impulses, which are smaller than the adjusted time, are filtered) (Set value * 8 µs corresponds to the filter time) (Default = 0; valid value range 0 … 4094, 4095 not allowed!)
16#5C	READ/ WRITE	BYTE	**Channel 5– counter - Configuration** Bit 0 Direction: Up = 1 / Down = 0 Bit 1 Enable (Reference counter must also be enabled) counter Start = 1 / counter Stop = 0 Bit 2 Load: new load value = 1 Bit 3 clock: internal = 0 / external = 1 Bit 4...5 Flanks Internal clock 00: rising to falling Flank – low 01: falling to falling Flank – Period duration 10: rising to rising Flank – Period duration 11: rising to falling Flank– high External clock 00, 11: two flank analysis 01: single flank analysis (falling Flank) 10: single flank analysis (rising Flank) Bit 6...7 reserved

16#5D	READ/ WRITE	BYTE	**Channel 5 – SSI-Shift register frequency and Gray code Decoding** Bit 0...1 shift register frequency 00: 125 kHz 01: 250 kHz 10: 500 kHz 11: 1 MHz Bit 2 Gray code Decoding 0: off 1: on
16#5E	READ/ WRITE	BYTE	**Channel 5 – Channel Configuration and SSI-Status** Bit 0: channel mode 0 .. counter 1 .. SSI Bit 1: SSI-Status 0 .. SSI ready (Data valid) 1 .. SSI busy
16#5F	READ	BYTE	**Channel 5 – Channel configuration and SSI-Status** Bit 0: channel mode 0 .. counter 1 .. SSI Bit 1: SSI Start 1 .. SSI start (Frame started with next sync)

GENERAL

16#F7	READ/ WRITE	BYTE	**Status** Bit 0 = Status LED Bit 1 = Latch enable 0 enable 1 hold
16#F8	READ	BYTE	**PLL Status register** Bit 1 = PLL online Bit 0 = PLL lock (PLL engaged)
16#F8	WRITE	BYTE	**PLL Counter Configuration register** Bit 0 ... 7 : Register Select 0 : Offset Counter 250 (resolution 0,5 µs) Register Select 1 : Offset State Counter (resolution125 µs) Register Select 2/3 : Sub Millisecond Counter (resolution 0,5 µs)
16#F9	READ/ WRITE	BYTE	**PLL Configuration register** Bit 3…0: Period of the PLL time base in ms (Default value: 1 ms) Bit 6.. 4: Register Select for PLL Counter Configuration register 0 Offset Counter 250 (0 … 249) 1 Offset State Counter (0 … 7) 2 Sub Millisecond Counter (low byte: Bit 0 .. 7) 3 Sub Millisecond Counter (high byte: Bit 8 .. 10)
16#FA	READ	BYTE	**Reserved**
16#FB	READ	BYTE	**Xilinx Version**
16#FC ... FF			**Reserved for interface module (CIC)**