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The appearance of ENG (electronic news gathering) a little over 15 years ago profoundly affected our concepts of TV news presentation. Before then, TV news was merely an animated extension of the newspaper, reporting events in an essentially historical context with little viewer involvement. ENG changed all that by providing up-to-the-minute reports from flash points around the world. Wars, accidents and natural disasters now appear in our homes within hours of their occurrence and compel us, perhaps for the first time in history, to identify with the human distress that such events can engender. The cameras used for ENG, like the men who operate them, are a special breed – equipped to handle the roughest, most hazardous situations. Formerly based on camera tubes, ENG cameras have now gone over almost exclusively to solid-state imagers like Philips' own frame-transfer sensors, not only for their durability, but also for their lightness and excellent performance under adverse lighting conditions. ENG has finally come of age. And if this can help us realize that we all share a common world, maybe it will be an age well worth living in.

Contents

Engine management with the PCB83C552 single-chip 8-bit microcontroller

DION METZERMAEKERS and EVERT VAN VELDHUIZEN

The PCB83C552 is an 8-bit single-chip high-performance CMOS microcontroller for use in real-time applications such as instrumentation, industrial control and automotive control – specifically engine management systems. It is a derivative of the 8051 and includes dedicated on-chip hardware for these applications. It uses the powerful instruction set of the 8051 and additional special function registers are incorporated to control the on-chip peripherals. There are three versions of the microcontroller but the generic term 'PCB83C552' is used to refer to all:

- PCB83C552: 8 Kbyte mask-programmable ROM, 256 byte RAM
- PCB87C552: 8 Kbyte EPROM, 256 byte RAM
- PCB80C552: ROM-less version of the PCB83C552

FEATURES OF THE PCB83C552

- 8051 central processing unit
- 8 K × 8 ROM, expandable externally to 64 Kbytes
- 256 × 8 RAM, expandable externally to 64 Kbytes
- Two 16-bit timer/event counters: T0, T1 (identical to those of the 8051)
- An additional 16-bit timer/counter (T2) coupled to four 16-bit capture registers and three 16-bit compare registers
- Fifteen vectored interrupts; two priority levels
- 10-bit ADC with 8 multiplexed analog inputs
- Dual 8-bit DAC with pulse width modulated outputs
- Five 8-bit I/O ports plus one 8-bit input port
- I^2C-bus serial I/O port with byte oriented master and slave functions
- Full-duplex UART compatible with the standard 8051
- Watchdog timer
- On-chip oscillator and timing circuits

The combination of an additional timer (T2) and the capture and compare logic is very powerful in applications involving rotating machinery, automotive injection systems etc.

The PCB83C552 has two software-selectable modes of reduced activity for further power reduction: Idle and Power-down. The Idle mode halts the CPU and resets timer T2, the ADC and PWM circuitry but allows the other timers, RAM, serial ports and interrupt system to continue functioning. The Power-down mode saves the RAM contents but inhibits the oscillator, causing all other chip functions to become inoperative.

The PCB83C552 also functions as an arithmetic processor and has binary/BCD arithmetic and bit-handling facilities. The instruction set consists of over 100 instructions: 49 one-byte, 45 two-byte and 17 three-byte. With a 12 MHz crystal, 58% of the instructions are executed in 1 μs and 40% in 2 μs. Multiply and divide instructions require 4 μs.

For detailed information on the PCB83C552, consult the 'PCB83C552 User Manual' (order number: 9398 637 90011).

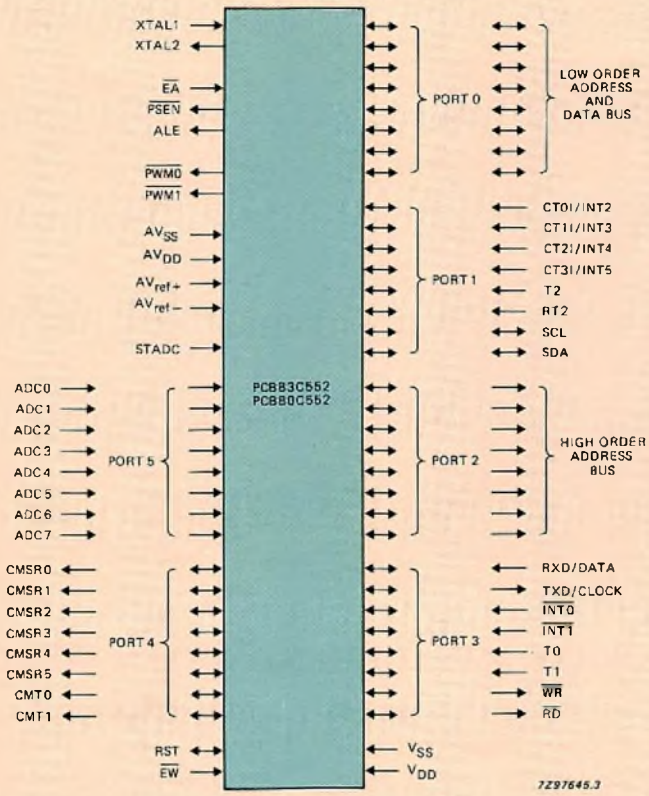


Fig.1 Functional diagram of the PCB83C552

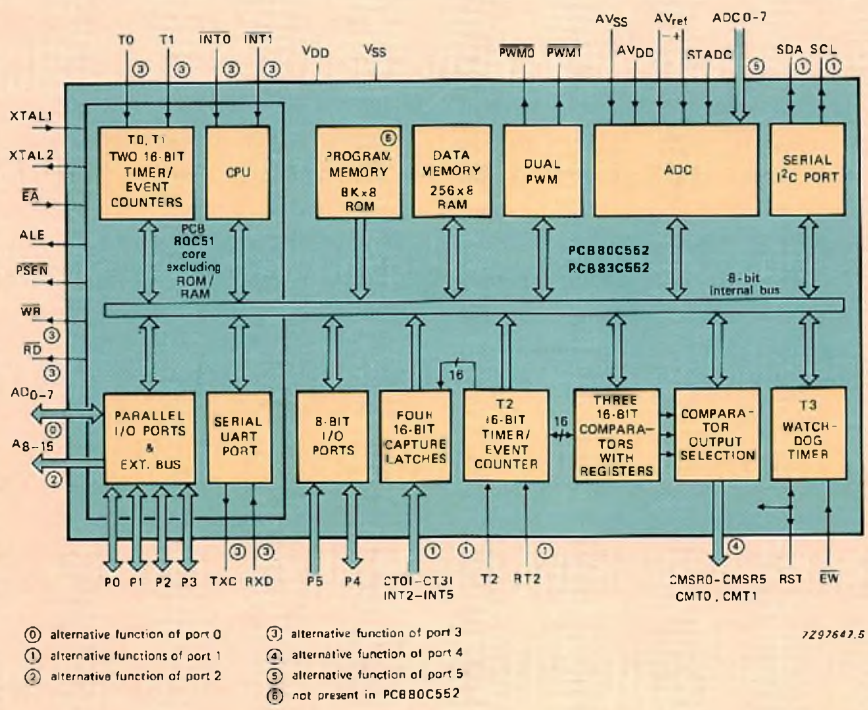


Fig.2 Block diagram of the PCB83C552

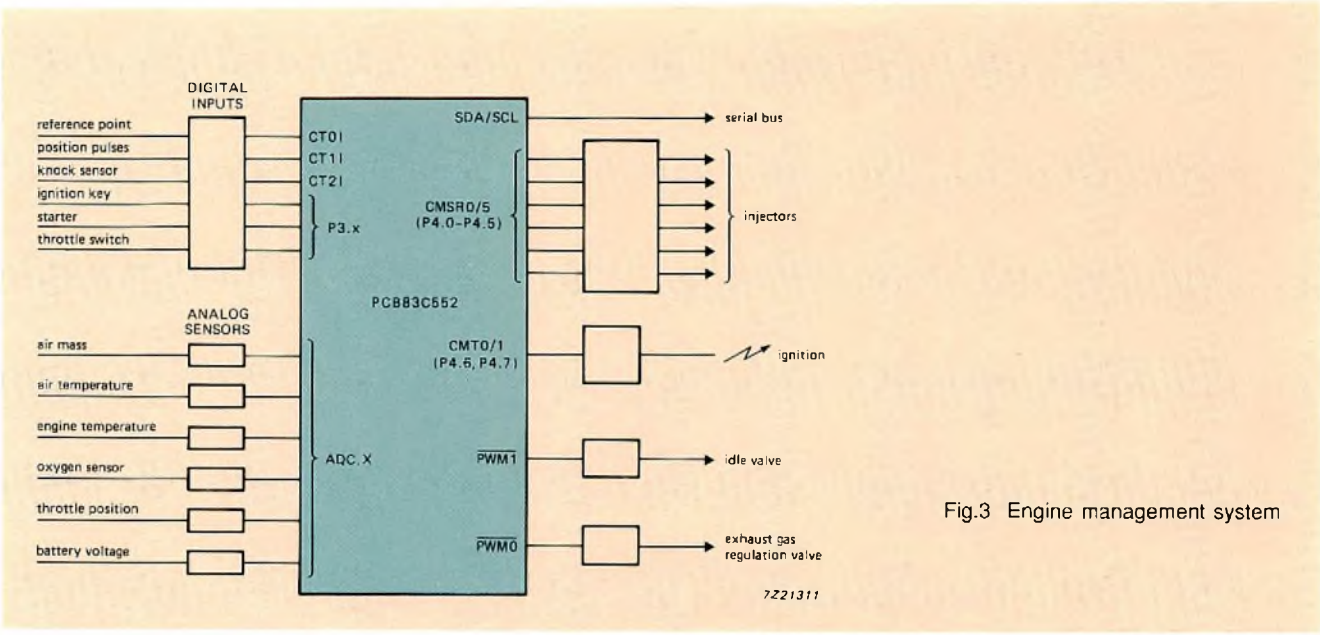


Fig.3 Engine management system

AN ELECTRONIC ENGINE MANAGEMENT SYSTEM WITH THE PCB83C552

Engine control has evolved from simple electronic ignition to modern closed-loop systems that operate in extreme conditions and compensate for engine wear, maladjustment and variations in fuel quality. Concern for the environment has led to government limits on permitted emissions from new vehicles, conditions which must be met throughout the life of the vehicle. Catalytic converters have been used to control emissions, but they reduce engine efficiency and can only be used with unleaded fuel. The real solution lies in better ignition and fuel injection control. Modern engine management systems (see Fig.3) require components which perform accurate analog to digital conversion, precise timing of ignition and provide exact control of start and duration of injection.

The PCB83C552 dedicated single-chip micro-controller performs complete engine management for multi-point injection, ignition control, idle control and exhaust gas recirculation (EGR).

The ADC

Since the PCB83C552's ADC has a resolution of 10 bits, an open loop system may be used for fuel control. An ADC conversion may be initiated by hardware or by software. Eight analog channels are available and these should be sufficient for most engine management systems.

I/O timing

Timer T2 is a 16-bit timer coupled to four 16-bit capture registers and three 16-bit compare registers. A capture register may be used to capture the contents of timer T2 when a transition occurs on its corresponding input pin. A compare register may be used to set, reset or toggle port 4 output pins at programmed time intervals. Timer T2 and the capture and compare logic are shown in Fig.4. Timer T2 may be used to:

- determine engine speed
- time up to 6 injector (start and duration)
- time ignition spark and dwell for up to two coils

Timer T2 is clocked via a prescaler from one of two sources: $f_{osc}/12$ or an external signal. The prescaler has a programmable division factor of 1, 2, 4 or 8. When configured as a timer, T2 may record absolute time and the capture registers may be used to store the time at which certain events occur (e.g. the time at which a crankshaft or camshaft reference mark passes). Thus, the capture registers may be used to determine engine speed, cylinder recognition etc. The comparators may be used to set, reset and toggle port 4 bits P4.0 to P4.7. Port 4 bits P4.0 to P4.5 may be set when a match occurs between the contents of T2 and comparator 1, and reset when a match occurs between T2 and comparator 2. Bits P4.6 and P4.7 may be toggled when a match occurs between T2 and comparator 3. The contents of the Set Enable Register (STE) and Reset/Toggle Enable Register (RTE) determine which bits are affected. Up to six injectors may be driven by bits P4.0 to P4.5 and bits P4.6 and P4.7 can switch ignition coils on and off to obtain accurate spark timing and control of coil energy (charge time).

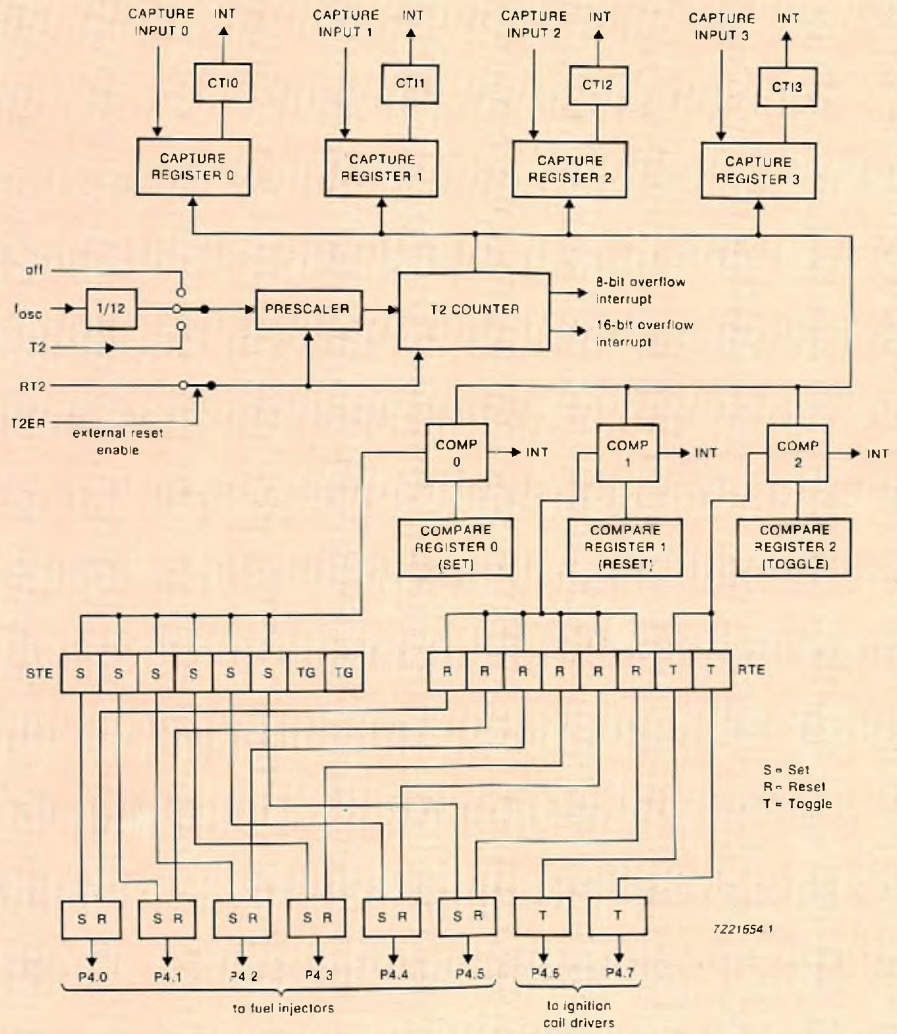


Fig.4 Timer T2, capture and compare logic

Analog outputs

The PCB83C552 also provides two 8-bit pulse width modulated outputs, PWM0 and PWM1. The PWM channels may output either a DC level (logic 0 or logic 1) or a square wave. The output frequency is programmable between 92 Hz and 23.5 kHz and the mark/space ratio varies between 0/255 and 255/255 in increments of 1/255. These output signals may be used to drive valves for idle speed control (throttle by-pass) or exhaust gas re-circulation (EGR). Two analog output signals may be obtained by integrating PWM0 and PWM1 using standard operational amplifier circuitry.

Watchdog

The PCB83C552 is also equipped with a watchdog timer, Timer T3, which resets the microcontroller in the event of a malfunction. It's analogous to the 'dead man's handle' in railway locomotives. When enabled, the watchdog circuitry will generate a system reset if the user program fails to reload the watchdog timer within a specified length of time known as the watchdog interval. The watchdog interval is programmable between 2 ms and 510 ms. In order to reload the watchdog timer, two actions must be performed. First, the watchdog load enable bit must be set; then the watchdog timer must be reloaded.

Timed sequential fuel injection

Optimum combustion gives improved torque, better fuel efficiency and fewer emissions. Combustion depends on the air/fuel mix and this is improved by atomizing the injected fuel. The atomization process depends on the speed of the air. With multi-valve engines, the air speed is significantly reduced at low engine speeds and, in modern engines, injection timing becomes very important (see Ref.).

Fuel injection is timed with respect to the opening of the inlet valve(s). This means that the start of injection has to be determined for each cylinder individually, relative to a crankshaft reference point.

The following describes how sequential timed fuel injection with possible overlap may be achieved in a 4-cylinder engine. Figure 5 shows a complete cycle for each cylinder (two crankshaft revolutions). Injection start and injection stop are shown relative to a reference point on the crankshaft. The cylinders are numbered in order of injection sequence.

Injection start is usually given in crank-angle degrees with respect to TDC. This angle has to be converted to time with respect to the reference time. Stop times are calculated by adding the calculated injection duration.

The injector drivers are connected to pins of output port 4. These pins are controlled by timer T2 and the compare logic (see Fig.4). The reference signal is connected to the capture 0 input, CTI0. When a rising edge occurs on this input, capture register 0 (CT0) is loaded with the contents of timer T2 and an interrupt is generated. Thus the absolute time of the reference point for a specific cylinder is known in software.

To initiate injection, compare register 0 (CM0) is loaded with a value relative to the reference time for the cylinder, and the corresponding bit in the STE register is set to logic 1. When comparator 0 detects that timer T2 has reached the value held in CM0, the corresponding port 4 output pin is set and an interrupt is generated. At this stage, CM0 must be loaded with the start time for the next injector relative to the new reference time. The STE bit corresponding to the next injector must also be set, and the bit corresponding to the previous injector must be reset.

To terminate injection, compare register 1 (CM1) is loaded with a value relative to the reference time for the cylinder, and the corresponding bit in the RTE register is set to logic 1. When comparator 1 detects that timer T2 has reached the value held in CM1, the corresponding port 4 output pin is reset and an interrupt is generated. At this stage, CM1 must be loaded with the stop time for the next injector relative to the new reference time. The RTE bit corresponding to the next injector must also be set, and the bit corresponding to the previous injector must be reset.

A block diagram of the various software sections is shown in Fig.6. In the main program, the injection duration and the start of injection relative to the reference time are calculated using algorithms. Parameters for these algorithms are derived from various inputs (engine speed, amount of air, temperature etc.) which are used with look-up tables.

Time-critical actions such as the loading of CM0 etc. should be performed immediately after the associated interrupt. However, because interrupt routines can't be interrupted, they must be as short as possible. This is realized by using 'flag routines' which can be interrupted.

In the interrupt routine a CALL is made to a subroutine which only contains an RETI instruction.

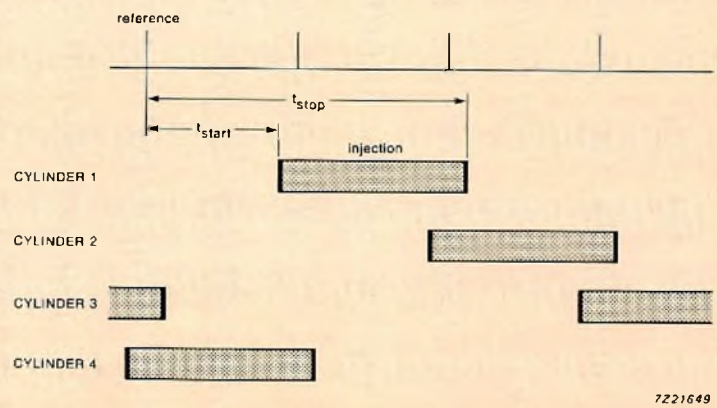


Fig.5 Four cylinder injection timing

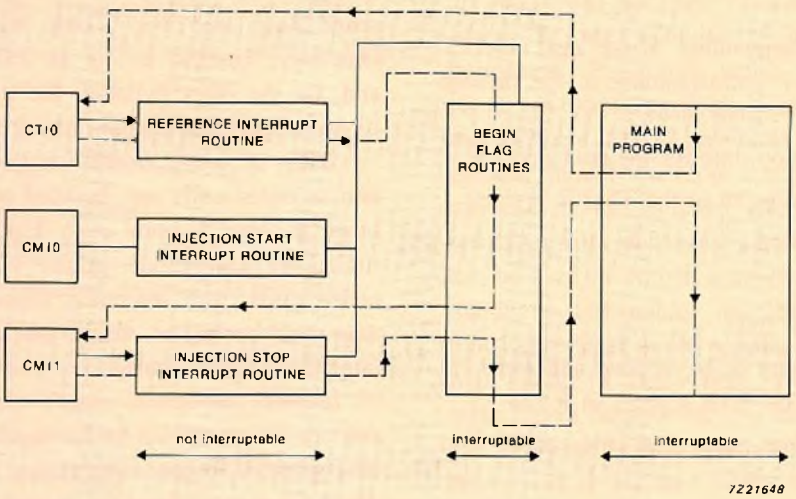


Fig.6 Software structure

This causes a return to the interrupt routine, but the interrupts may now be enabled again and the main program return address is still on the stack. A jump is then made to the flag routines. At the end of a flag routine, an RET instruction is executed to return to the correct location in the main program. An example is given below:

```
                interrupt routine
                ;
                SETFLAGx        ; set the flag corresponding to this
                                  interrupt
                CALL INTRET     ; push address of LJMP on stack, branch
                                  to RETI
;
                LJMP FLGROUT    ; jump to flag routine while return
                                  address of main program is still on the
                                  stack
;
INTRET          RETI            ; return from interrupt to enable any
                                  other pending interrupts, pop address of
                                  LJMP
-------------------------------------------------------------------------
                flag routine
                ;
                RET             ; return to main program
```

For each interrupt routine there is also a flag routine. After an interrupt or flag routine, all flags are tested in sequence. When a flag is set, the associated flag routine is executed. A flag routine may be interrupted, and will continue after the interrupt routine (and possibly another flag routine) have been executed.

The actions that are performed in the interrupt and flag routines are listed below:

Reference Interrupt (CT0I)

Interrupt routine actions

- Set the reference flag. This is the only interrupt routine action. The CT0I interrupt bit in the TM2IR register is cleared in the flag routine after this information is used.

Flag routine actions

- Reset the reference flag
- Calculate the cycle time. $T_{cycle} = T_{CT0} - T_{abs}$ (previous reference)
- Store the absolute reference time (T_{abs}) in RAM
- Clear the CTI0 interrupt flag in the TM2IR register
- Determine the cylinder number.

Injection Start Interrupt (CM0I)

Interrupt routine actions

- Set the STE bit corresponding to the next injector and clear the STE bit corresponding to the present injector
- Load CM0 with the start time for the next injector
- Clear the CMI0 interrupt bit in the TM2IR register
- Set the start injector flag.

Flag routine actions

- Reset the start injector flag
- Identify the next injector to be started and store the appropriate mask for the STE register in RAM
- Determine the absolute start time and store it in RAM.

Injection Stop Interrupt (CM11)

Interrupt routine actions

- Set the RTE bit corresponding to the next injector and clear the RTE bit corresponding to the present injector
- Load CM1 with the stop time for the next injector
- Clear the CMI1 interrupt bit in the TM2IR register
- Set the stop injector flag.

Flag routine actions

- Reset the stop injector flag
- Identify the next injector to be stopped and store the appropriate mask for the RTE register in RAM
- Determine the absolute stop time and store it in RAM.

Distributorless ignition

In a conventional engine with mechanical contact-breakers and a single coil, a distributor is used to connect the spark plugs in sequence to the high voltage end of the coil, producing a spark in each cylinder.

The contact-breakers may be replaced by electronics. However, with the exception of a two-cylinder engine, a distributor is still needed with a single coil. With a two-cylinder engine, each end of the coil is connected to a spark plug (see Fig.7) and both plugs fire simultaneously. Ignition timing is correct for one cylinder and, for the other cylinder, the spark occurs at the end of the exhaust stroke and has no effect.

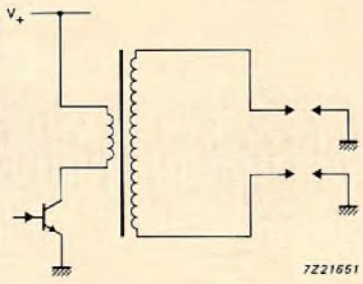


Fig.7 Double ended coil

With a four-cylinder distributorless engine, two double ended coils may be used or each spark plug may have its own ignition coil. Figure 8 shows the coil timing for a 4-cylinder engine which uses two double-ended coils. The reference should occur before TDC (top dead centre) to ensure that ignition always occurs after the reference point.

Ignition advance is usually expressed in crank-angle degrees before TDC. As for injection, this angle has to be converted to time with respect to the reference time. The time elapsed from the moment the coil is turned on to the moment it is turned off is called the dwell or load time. At the end of this period, there should be sufficient current flowing through the coil to cause an adequate spark when the coil is switched off. The time at which the coil is turned on is calculated by subtracting the load time from the ignition time (T_{ign}).

The coil drivers are connected to bits 5 and 6 of port 4 (see Fig.4). These two bits are toggled and the CM2 interrupt flag is set when a match occurs between timer T2 and the CM2 compare register provided that the corresponding bits in RTE are set.

In the main program, the switch on and switch off times have to be calculated for both coils with respect to specific reference points. After each CM2 interrupt, register CM2 must be reloaded and bits 6 and 7 of RTE must be inverted. The two coils can be controlled independently. However, when one coil has to be switched on and the other has to be switched off within the interrupt latency plus coil handling time, both actions should be carried out simultaneously. In this case, the coil which should be switched off (ignition) has priority. The software structure is similar to that for fuel injection shown in Fig.6.

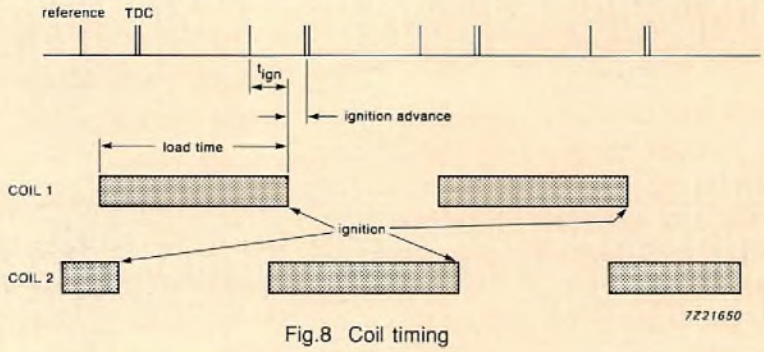


Fig.8 Coil timing

In the ignition interrupt routine:

- RTE bits 6 and 7 are set to switch the next coil
- register CM2 is reloaded with a value corresponding to the next switch on or switch off time
- the CMI2 interrupt flag in register TM2IR is reset
- the ignition flag is set.

The flag routines are then executed.

In the ignition flag routine:

- the next coil to be switched on or off is selected
- the contents of RTE bits 6 and 7 and a value corresponding to the next switch on or switch off time are calculated. These values are used in the ignition interrupt routine and they are derived from coil load time and ignition time which are calculated in the main program.

Air-flow measurement by means of timed A/D conversion

For optimum performance of a spark-ignited combustion engine, it's essential that the optimum mixture (air/fuel ratio) is maintained. To achieve the optimum mixture, the amount of air that enters the inlet manifold must be measured very accurately.

Air flow may be measured by a vane-type air flow meter, a hot-wire mass air flow sensor or an inlet manifold air pressure sensor. The output from these sensors is usually an analog voltage that must be converted to a digital value before it can be processed by the microcontroller. Several factors affect the accuracy of the value including the accuracy of the sensor itself (which is influenced by temperature, age etc.), noise, and the accuracy of the ADC (the PCB83C552 on-chip, 8-channel ADC has a resolution of 10 bits). The accuracy of the value also depends on when, in the cylinder cycle, the measurement is performed. Pulsations which significantly affect the result can occur, particularly at low engine speeds. The measurement (A/D conversion of the processed sensor output) should therefore be performed at a specific moment in the cylinder cycle e.g. at TDC. If this coincides with the reference point, the reference signal can be used to initiate a hardware ADC start. When the 'hardware-start-enable' bit of the ADCON special function register is set, a rising edge on the STADC pin will initiate a conversion (see Fig.9). Conversion of other sensor outputs may be initiated by software. When the relevant analog channel has been selected, a conversion is initiated when the 'software-start-enable' bit of the ADCON special function register is set.

When the conversion is complete, the ADC interrupt flag (ADCI) is set. The ADC interrupt routine sets the analog flag and the flag routines are then executed.

In the analog flag routine:

- the converted result is read and stored in RAM
- the ADC interrupt flag is reset
- a new analog input channel is selected via the analog multiplexer
- if the next input to be converted is not the air flow measurement, the hardware start is disabled and a conversion is started by software
- if the next input is the air flow measurement, the hardware start is enabled and a conversion will commence when a rising edge occurs on pin STADC
- the analog flag is reset.

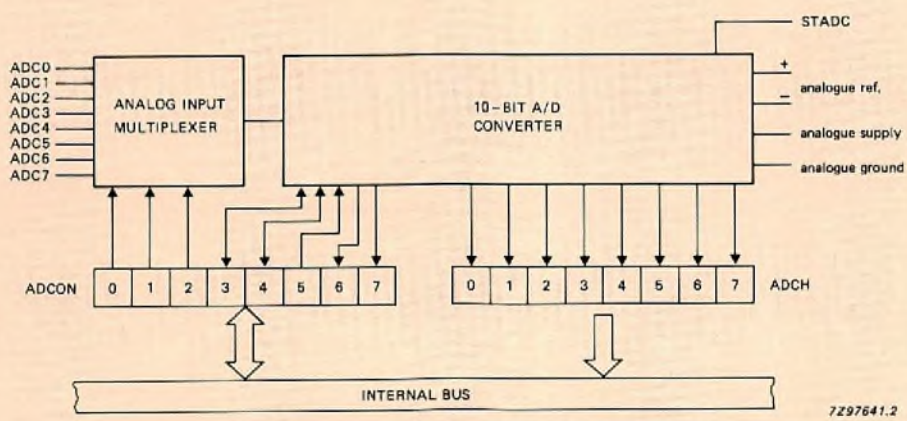


Fig.9 Block diagram of the PCB83C552's ADC

Valve control

The PCB83C552 may also be used to control idle stabilization and exhaust gas recirculation (EGR). Idle speed is regulated by a throttle by-pass valve which controls the amount of air entering the inlet manifold when the throttle is closed. The amount of air is measured and the quantity of fuel to be injected into each cylinder can then be calculated. Idle speed can be corrected by controlling the position of the throttle by-pass valve.

Exhaust gas recirculation increases engine efficiency at partial load and reduces the amount of nitrogen oxide emitted. The amount of exhaust gas fed back to the inlet manifold depends on a number of input parameters including engine load, and is controlled by a valve.

The position of the throttle by-pass or EGR valve depends on the voltage applied to the valve. These two voltages must be controlled by the microcontroller. The PCB83C552 contains two pulse width modulated output channels (see Fig.10). These channels generate pulses of programmable length and interval. These pulses can be integrated using conventional operational amplifier circuitry and buffered to drive the valves. The pulses may also be integrated using the mechanical inertia of the valves.

The repetition frequency is defined by an 8-bit prescaler PWMP which supplies the clock for an 8-bit counter. The prescaler and counter are common to both PWM channels. The repetition frequency, f_{PWM}, at the PWMn outputs is given by:

$$f_{PWM} = \frac{f_{OSC}}{2 \times (1 + PWMP) \times 255}$$

This gives a repetition frequency range of 92 Hz to 23.5 kHz (f_{OSC} = 12 MHz).

The 8-bit counter counts modulo 255 i.e. from 0 to 254 inclusive. The value in the 8-bit counter is compared with the contents of two registers: PWM0 and PWM1. When the contents of either of these registers is greater than the counter value, the corresponding PWM0 or PWM1 output is logic 0 (see Fig.11). If the contents of these registers are equal to, or less than the counter value, the output will be logic 1. The pulse-width-ratio is therefore defined by the contents of the registers PWM0 and PWM1. The pulse-width-ratio is programmable between 0 and 255/255 in increments of 1/255.

Loading the PWM registers with either 00H or FFH will cause the PWM channels to output a constant logic 1 or logic 0 respectively. Since the 8-bit counter counts modulo 255, it can never actually reach the value in the PWM registers when they are loaded with FFH.

When register PWM0 or PWM1 is loaded with a new value, the associated output is updated immediately, not at end of the current counter period.

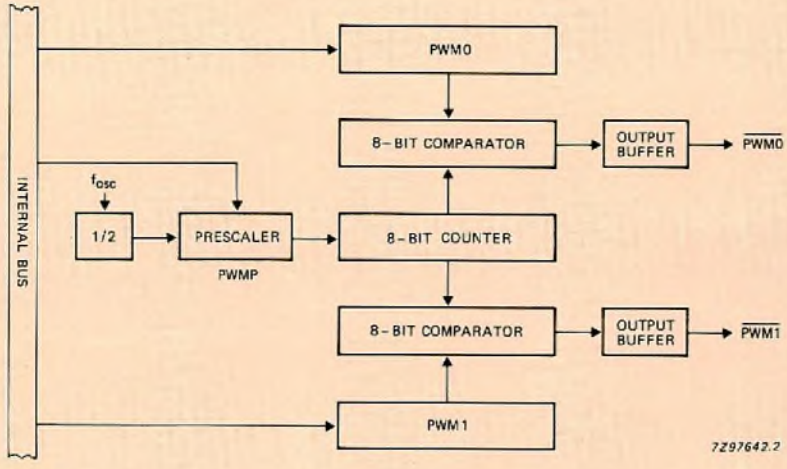


Fig.10 Block diagram of the pulse width modulated outputs

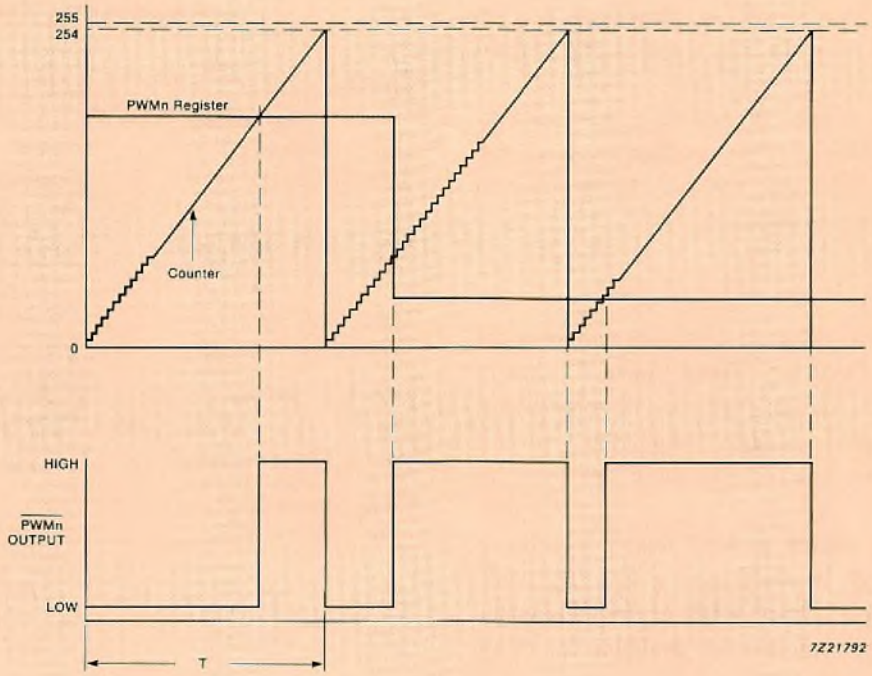


Fig.11 Quasi analog output

Checking program flow

Microcontrollers may enter erroneous processor states induced by electrical noise, RFI or a momentary drop in supply voltage. The normal program flow may also be disturbed by software which has not been fully debugged: an unforeseen combination of input conditions may cause the program flow to be disrupted. The purpose of the PCB83C552's on-chip watchdog timer (T3) is to reset the microcontroller within a reasonable period of time in the event of such a disruption.

When enabled, the watchdog circuitry will generate a system reset if the user program fails to reload the watchdog timer within a specified time (the watchdog interval). The watchdog interval is programmable between 2 ms and 510 ms. The watchdog timer consists of an 8-bit timer with an 11-bit prescaler as shown in Fig.12. The prescaler is clocked by a signal whose frequency is $f_{OSC}/12$ (1 MHz with a 12 MHz oscillator). The 8-bit timer is incremented every 't' seconds where:

$$t = 12 \times 2048 \times 1/f_{OSC}$$
$$= 2 \text{ ms (when } f_{OSC} = 12 \text{ MHz)}$$

If the 8-bit timer overflows, a short internal reset pulse is generated which will reset the PCB83C552. A short output reset pulse (3 machine cycles) is also generated on the RST pin. This pulse may be destroyed if the RST pin is connected to a capacitor. This would not, however, affect the internal reset operation. Watchdog operation is enabled when external pin EW is tied low. It is impossible to disable watchdog operation by software when EW is tied low.

The watchdog timer has to be reloaded within periods shorter than the programmed watchdog interval (see Fig.13), otherwise the timer will overflow and a system reset will be generated. The user program must always reload the watchdog timer within the watchdog interval. When using a 12 MHz oscillator, the watchdog interval is programmable between 2 ms and 2 × 255 ms.

To prevent erroneous software from reloading the watchdog timer, it is reloaded in two stages. First, the watchdog load enable bit must be set. Then T3 may be loaded. When T3 is loaded, the watchdog load enable bit is automatically reset. T3 can't be loaded if this bit is reset.

Since timer T3 is an up-counter, a reload value of 000H gives the maximum watchdog interval (512 ms with a 12 MHz oscillator) and a reload value of FFH gives the minimum watchdog interval (2 ms with a 12 MHz oscillator).

In the Idle mode, the watchdog circuitry remains active. When watchdog operation is implemented, the Power-down mode can't be used since both states are contradictory. Thus, when watchdog operation is

enabled by tying external pin EW low, it is impossible to enter the Power-down mode; an attempt to set the Power-down bit will have no effect and it will remain at logic 0.

During the early stages of software development/ debugging, the watchdog may be disabled by tying the EW pin high. At a later stage, EW may be tied low to complete the debugging process.

System development

A number of steps are involved in the development of an engine control system. These include system specification, hardware design, software design, system debugging, and system-to-engine adaptation. Several development tools are required and these are listed in Table 1.

Software may be written in 8051 assembly code or in PL/M51 high-level language on a PC (IBM-AT, IBM-XT or compatible), Intel MDS or host computer system. Assemblers or compilers are available for all of these systems.

TABLE 1
System development tools

Equipment	Function
Personal Computer	Software design, System debugging, System-to-Engine adaptation
8051 assembler or PL/M-51 compiler	Software design
Engine simulator	System debugging
SDS-80C552	System debugging
EPROM programmer	System debugging, System-to-Engine adaptation
Dual port RAM controller	System-to-Engine adaptation
PC program for loading and modification of tables	System-to-Engine adaptation

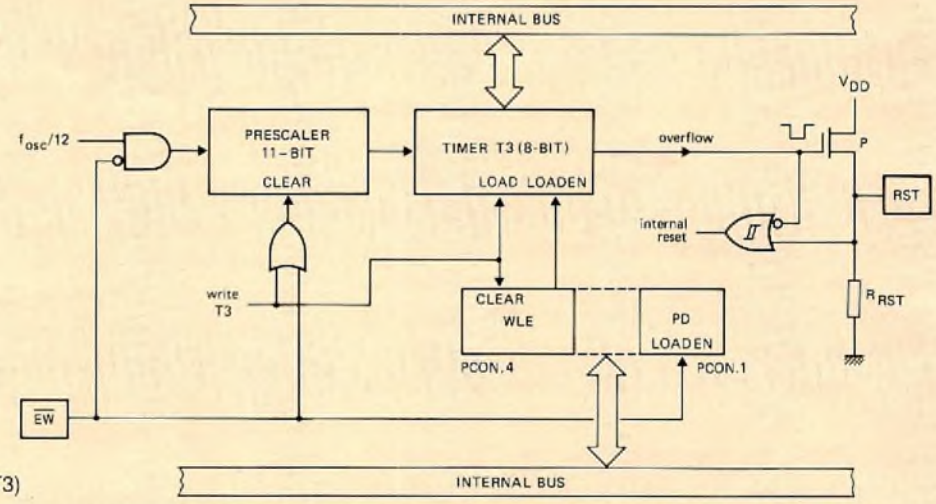


Fig.12 Watchdog timer (T3)

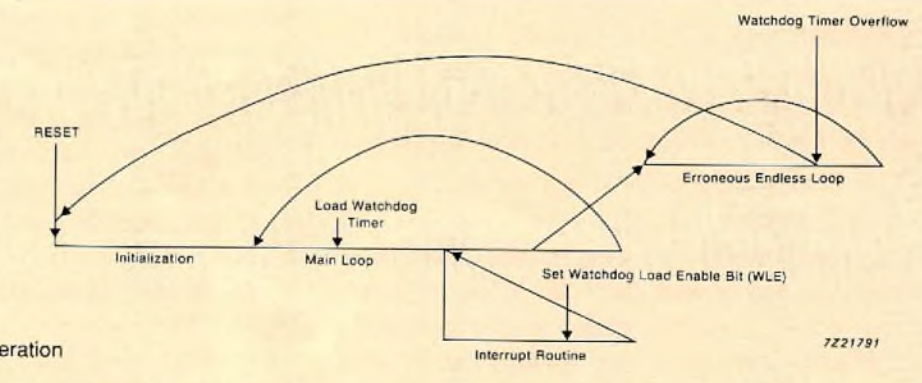


Fig.13 Watchdog timer operation

For system debugging, a Philips SDS (Stand-alone Debugging System) may be used (see Fig.14). The system's emulation probe is plugged into the 83C552 socket. The SDS has several debug facilities including single-step, break-point, and program trace. A PC (or a VDU terminal and host computer) may be connected to the SDS to enable the programmer to transfer the program object file, type commands etc.

For prototype development, an EPROM programmer can be connected to the PC or host computer via an RS232 interface and used to program the EPROM version of the PCB83C552 (the PCB87C552) or an EPROM to be used by the ROM-less version (the PCB80C552).

In order to check the control software, an engine simulator may be used to provide input signals for the engine control system. The simulator may be a simple device consisting of a pulse generator to produce reference pulses, switches to simulate digital inputs, and potentiometers to simulate analog input signals.

When the control program is running correctly with an engine simulator, the engine control system may be connected to the actual engine that has to be controlled. Engine performance can then be optimized by modifying the tables and constants used by various software algorithms. A quasi-dual-port RAM may be used to store these tables and constants (see Fig.15). The contents of the RAM may be modified by the PC. The engine control system uses this RAM instead of the internal ROM or external EPROM. Ideally, it should thus be possible to modify the tables and constants while the engine is running.

REFERENCE

1. Improving Lower Speed Engine Response, Automotive Engineering, February 1987, pp 137 – 146).

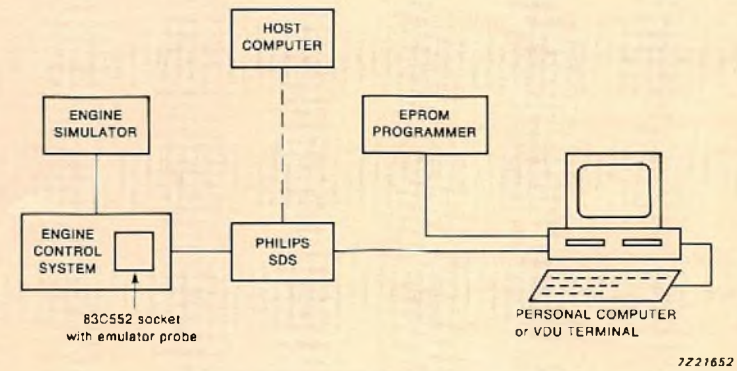


Fig.14 System development

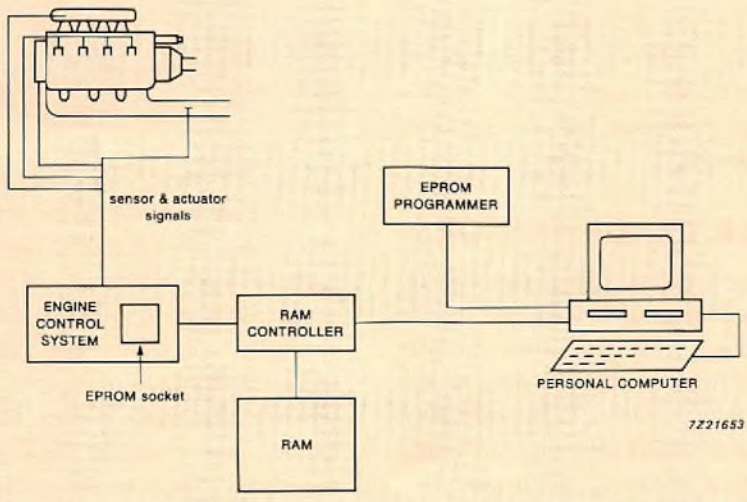


Fig.15 System-to-engine adaptation

Inexpensive monochrome TV camera design – brings CCD imaging into everyday applications

THOMAS WESTENDORFF

For applications such as home-surveillance cameras, video phones, door security systems, automotive rear-view systems, etc., many of today's CCD TV cameras are over complicated and thus needlessly expensive. Many potential camera applications have never been exploited because TV cameras, of any sort, are simply too expensive. For these reasons, we've designed a monochrome CCD camera that brings all the advantages of solid-state imaging within the price range of many consumers.

The most expensive component in a CCD TV camera is the image sensor. After manufacture, all image sensors are checked for picture element (pixel) defects, graded and then priced accordingly. The secret of our design is a simple but effective signal-processing technique specifically for low-cost image-sensors with pixel defects.

By processing only the low frequency components of the image-sensor output signal, the influence of pixel defects on picture quality can be reduced to an acceptable level. The horizontal resolution of such a camera is, however, lower than usual but it is perfectly adequate for many applications.

FRAME-TRANSFER IMAGE SENSORS

The camera uses a frame-transfer CCD image sensor, originally designed for high-resolution cameras. As the name suggests, it operates on the frame-transfer principle: each of the two fields of the complete picture frame is separately integrated within a photosensitive imaging region, transferred by CCD shift registers into a storage region during vertical blanking, and then clocked out serially to form the video signal during the subsequent integration period.

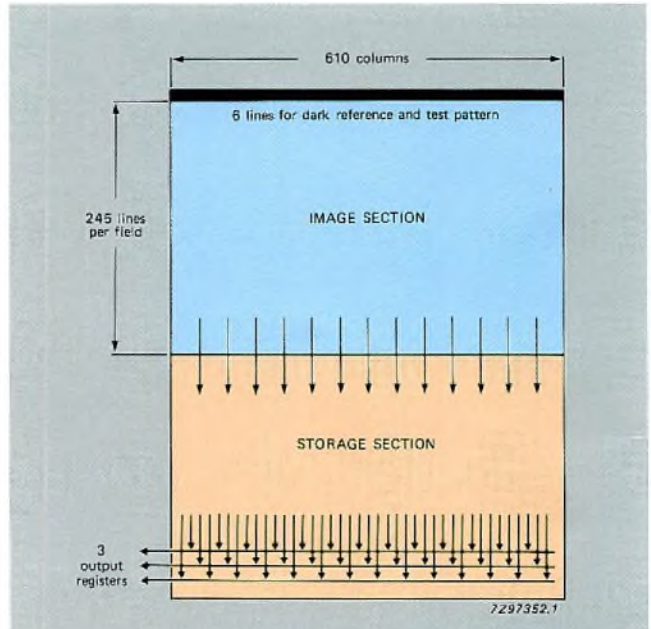


Fig.1 Structure of our frame-transfer sensor (EIA version)

Our FT sensors have 610 (EIA version, see Fig.1) or 604 (CCIR version) pixels per line and this, of course, determines the horizontal resolution of the sensor. The photosensitive image region and the storage region are connected by 610 (or 604) CCD shift registers running vertically through both regions. These registers, separated by stop diffusions, define the pixel width, separate the lines in both the image and the storage regions, and transport the light-generated charge from the image region to the storage region. The number of lines in the sensor is dictated by the TV-standard: a sensor for the 525-line (EIA) standard has 245 active

lines (6 more for black-level reference), and for the 625-line (CCIR) standard, 288 lines. Since two fields are used to form an image frame, each frame comprises 490 × 610 pixels for EIA or 576 × 604 pixels for CCIR.

When the image section of the sensor is illuminated, light generates electron/hole pairs and the electrons collect under the positive electrodes of the CCD-registers. In the vertical direction, pixels are separated by the negative electrodes of the registers to form the lines of a field. The electron charge is integrated in the imaging region during a field period of 16 ms for an EIA sensor (18.36 ms for CCIR). During the vertical blanking period (about 1.6 ms), the charge is rapidly transferred (within 0.5 ms) to the storage section using the shift-registers. In the next field period, a new image is collected in the imaging region while charge from the storage region is read out line by line (during the horizontal blanking period).

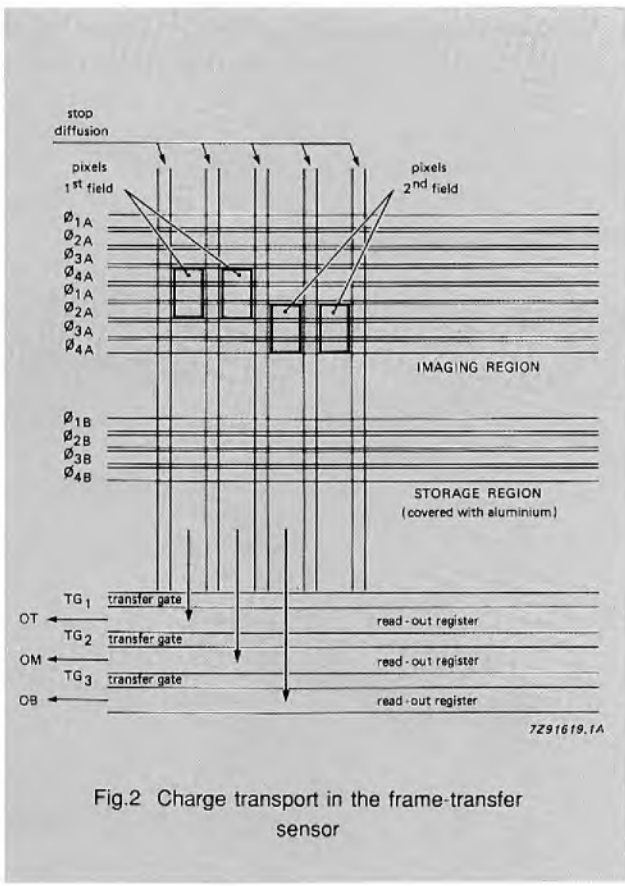


Fig.2 Charge transport in the frame-transfer sensor

During each horizontal blanking period, the charge content of the storage section is moved downward by one line, and the bottom line is transferred into three read-out registers and then read out (Fig.2). Each read-out register is connected to every third vertical shift register, so each reads out about 200 pixels of any line.

This arrangement has two advantages:

- it allows a much higher horizontal pixel density than would a single read-out register, in which the finite width of the gate electrodes limits the minimum horizontal spacing between charge packets. With three shift registers, the spacing is effectively reduced threefold
- it allows selective separation of charge packets within each line and thus, with stripe filters over the imaging region, it allows the device to be used as a colour image sensor.

The read-out registers have separate outputs (output top (OT), middle (OM), and bottom (OB)) and the charge, read out sequentially from the three channels, represents the signal of one TV line; lines are read out in the normal scanning sequence of the TV standard. The output signals (Fig.3) have a phase difference of 120° and each consists of clock-generated crosstalk plus the pixel content. The duty factor of the signals is about 50% so there is a short time in which two outputs are active simultaneously.

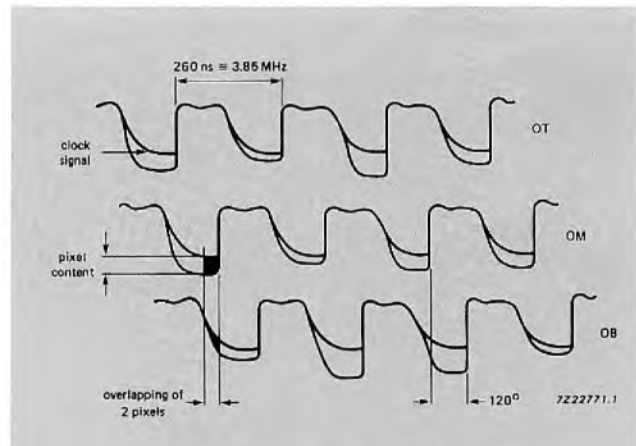


Fig.3 Sensor output signals

STANDARD SIGNAL PROCESSING

For EIA and CCIR sensors, with about 200 picture elements per read-out register, a clock frequency of 3.8 MHz is needed to read out the charge in the standard TV-line period (52 µs). This means the maximum signal bandwidth per channel is 1.9 MHz (Nyquist's theorem). To obtain the maximum possible resolution from this sensor, the signals of the three channels have to be sampled sequentially for multiplexing, at a clock frequency of 11.4 MHz (3 × 3.8 MHz). The maximum bandwidth of the multiplexed signal is then 5.7 MHz (corresponding to 610 or 604 pixels per line).

In this kind of signal processing, the three channels have to be well matched to avoid 3.8 MHz clock components in the video signal: there should be no differences between the sensor output stages or between the three channels of the signal processing circuit.

LOW-COST SIGNAL PROCESSING

With standard signal processing, defective pixels in the sensor result in black or white spots on the TV picture. A defective column is far worse, producing a black or white vertical stripe. To be able to use sub-standard sensors and still obtain an acceptable TV picture, a different method of signal processing is necessary.

In applications where high-resolution is not required, an easy solution is to use the signal from only one channel, excluding the channels that contain signals from defective columns (Fig.4). Then, the only signal processing required is a low-pass filter to limit the bandwidth to the Nyquist frequency of one channel (e.g. 1.9 MHz, corresponding to about 200 pixels per line). Since sub-standard sensors usually have only one or two defective columns, this technique is easy to employ and quite satisfactory.

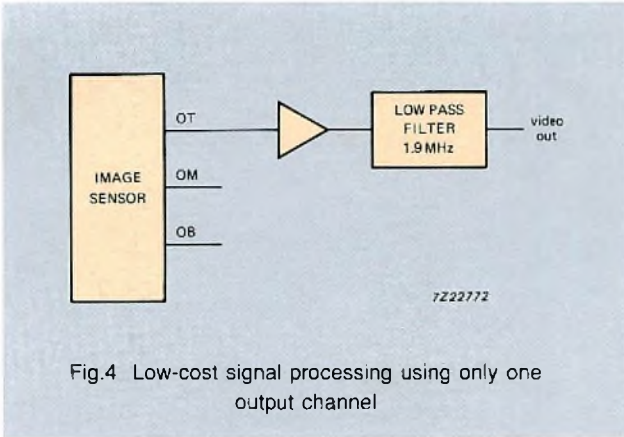


Fig.4 Low-cost signal processing using only one output channel

A more effective solution is possible using the signals from all three channels without a special sampling and multiplex circuit: the signals are combined in a common load circuit (see Fig.5). The bases of the PNP transistors are connected to the sensor output signals, the emitters are connected together, and the collectors are connected to ground. When a transistor's base potential falls below that of the emitter, the transistor is switched on. Figure 3 shows that a sensor output signal has its lowest voltage when a pixel is being read out. For most of this period, the other two outputs have a higher potential so this circuit automatically combines the pixels from the three channels sequentially.

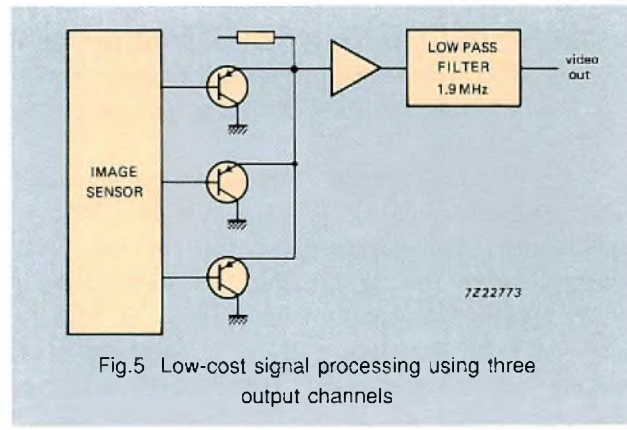
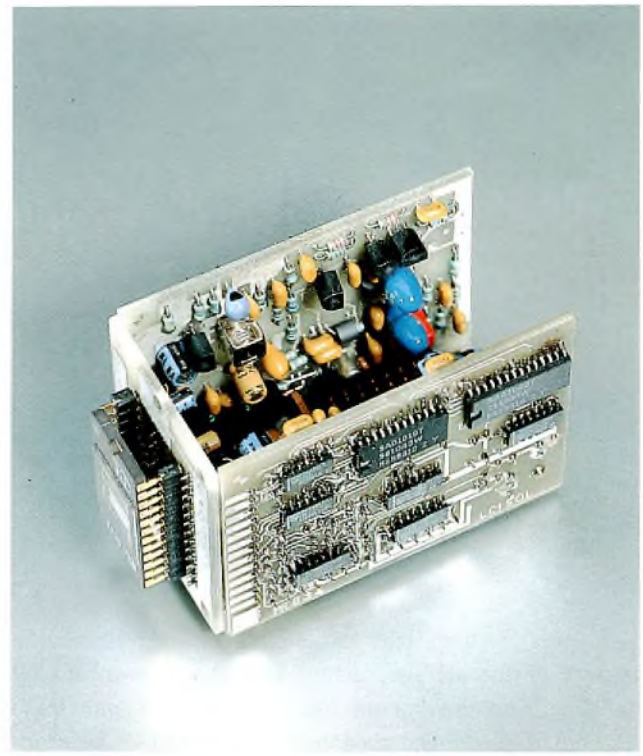


Fig.5 Low-cost signal processing using three output channels

When two channels are active simultaneously, the contents of two adjacent pixels are simply averaged so the resolution isn't as good as using a sampling technique (the bandwidth falls below 5.7 MHz). However, the effect of a defective pixel is thus reduced by its charge being averaged with that of a normal pixel.

If a sensor has a defective column, the error signal is mainly in the upper range of the output signal's frequency spectrum (3.8 MHz). By low-pass filtering the output signal to about 2.7 MHz, a value sufficiently below the disturbing vertical stripe frequency, the influence of defective pixels can be further reduced to obtain an acceptable TV picture.



Low-cost camera with simplified signal-processing circuitry and imperfect image sensor

CAMERA DESIGN AND CIRCUIT DETAILS

The basic construction we recommend to build a low-cost camera uses all three output channels of the image sensor, as described above. Refer to Fig.6 for the circuit description.

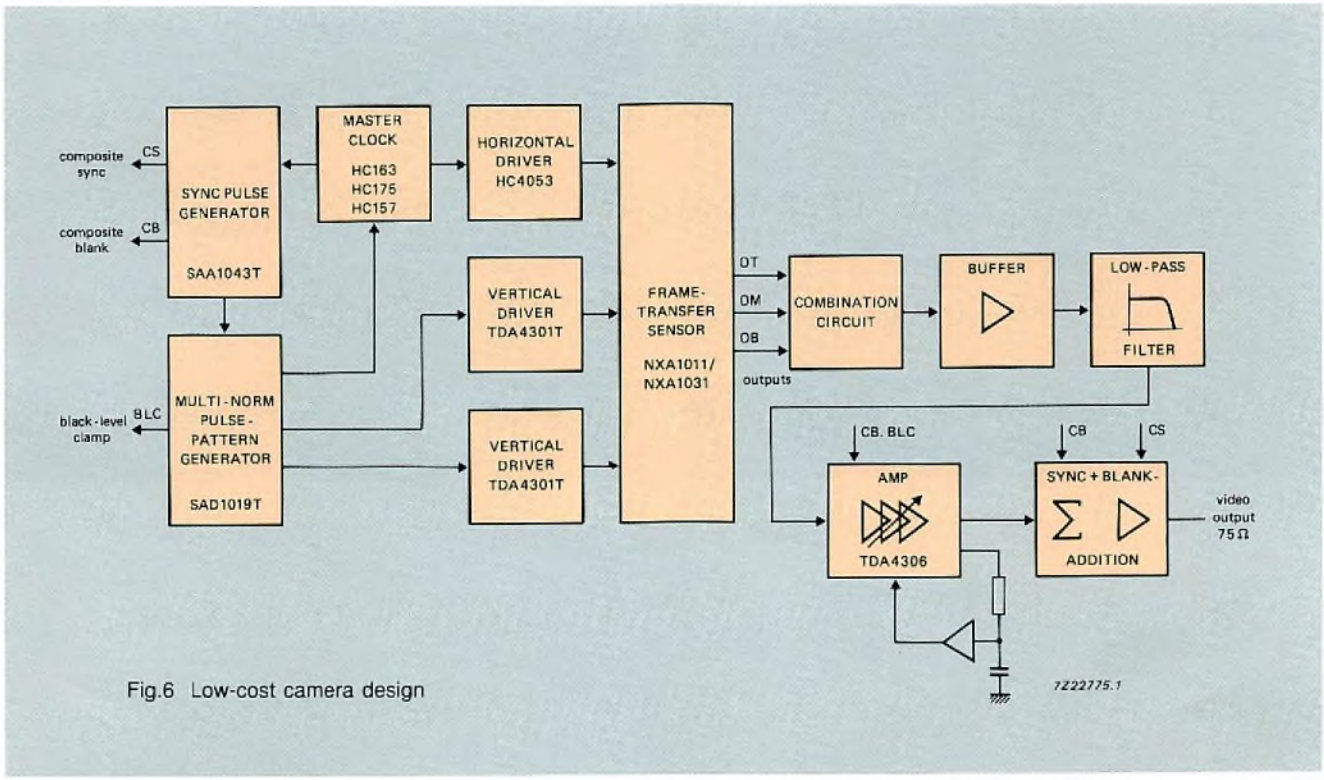


Fig.6 Low-cost camera design

Circuit description

The Master Clock, a crystal oscillator, generates the frequency reference for all timing circuitry: 22.5 MHz for CCIR, and 22.657339 MHz for EIA. This frequency is divided by nine (74HC163) to provide the clock drive for the Sync Pulse Generator (SAA1043T), which in turn provides the EIA or CCIR standard sync signals for the sensor (including vertical and horizontal blanking, vertical and horizontal drive, and composite sync).

The sync pulse generator controls the multi-norm pulse pattern generator (MNPPG). The MNPPG (an SAD1019T IC, developed specifically for our FT sensors) generates all the clock pulses for the sensor, except those for read-out. The output levels from the MNPPG are too low to drive the sensor's vertical shift registers directly, so vertical drivers (type TDA4301) are needed to boost the clock signals.

The fast horizontal drive pulses for the read-out registers are derived from the master clock directly: the master frequency reference is divided by six (74HC175) and used to provide three 3.8 MHz (3.75 MHz in practice) clock signals with 120° phase difference, during read-out. The pulses are fed to the sensor via a multiplexer (74HC157) and a horizontal driver (74HC4053). The MNPPG is also connected to the multiplexer so that normal transport pulses can be fed to the sensor during blanking, and read-out pulses during the active visible line period.

The three sensor output signals (OB, OM and OT) are combined using discrete transistors (see circuit in Fig.5). The result is an inverted image-signal, which is then amplified and low-pass filtered to reduce the influence of defective pixels/pixel columns, as described in the previous section. The low-pass filter has a cut-off frequency of 2.7 MHz, but the slope of the cut-off is not steep enough to completely remove all 3.75 MHz signal components, so an additional 3.75 MHz notch filter is used. Figure 7 shows the frequency characteristic of the notch and low-pass filter combination.

After filtering, the signal is fed through a multi-stage master-gain (MG) amplifier (type TDA4306) which also provides black-level clamping and AGC over a range of 1:125. The AGC voltage is derived from the video output signal.

A final stage, with 75 Ω output impedance, adds sync and blanking pulses to provide a standard video signal at the output.

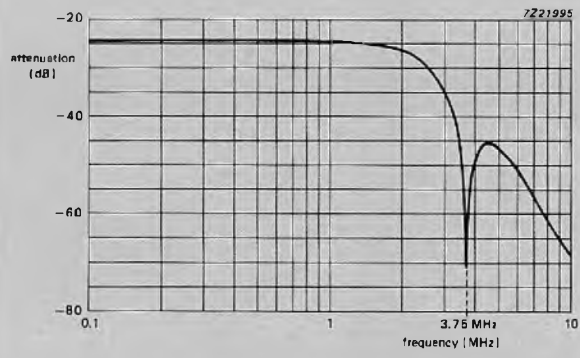


Fig.7 Frequency characteristic of notch filter and low-pass filter combination

Camera specification

Image sensor:	NXA1011/04 (CCIR) or NXA1031/04 (EIA)
Bandwidth:	2.7 MHz (at −6 dB)
Resolution:	
horizontal	250 TV lines
vertical	350 TV lines
Minimum sensor illumination:	0.4 lux (for −6 dB output voltage)
Signal to noise ratio:	42 dB (at 5 lux sensor illumination)
Gamma correction:	0.6
Automatic gain control (AGC) range:	1:125
Output signal:	1 V_{p-p} video (+700 mV white, +300 mV sync), 75 Ω
Temperature range:	−20 to +60 °C
Power supply	
current:	142 mA
voltage:	12 V

HCMOS analog switches and multiplexers/demultiplexers

ROB VOLGERS

Compared with integrated analog switches in other technologies, CMOS switches:

- have lower dissipation
- can handle a wider range of input voltages
- generate less switching interference
- have lower leakage currents.

Compared with analog switches in Philips' own HEF4000B CMOS series, the high-speed CMOS (HCMOS) versions have lower on-resistance, switch faster and have a wider frequency response, owing to their shorter channel lengths and lower parasitic capacitances.

More than a match for bipolar products, HCMOS switches and multiplexers are ideal for use in analog-to-digital conversion systems, signal source selectors in audio and video equipment, modulators, programmable amplifiers, filters and 'electronic' potentiometers to name but a few applications.

PRODUCT RANGE

Table 1 lists the analog switches and multiplexers/demultiplexers in the HCMOS product range (Ref.1). All circuits are available in plastic DIL and in

TABLE 1
HCMOS analog switches and multiplexers/demultiplexers

type	description	DC analog voltage range[1])	$R_{ONtyp.}$ (Ω)
74HC/HCT4016	quad bilateral switch	GND to V_{CC}	65
74HC/HCT4051	8-channel multiplexer/demultiplexer	V_{EE} to V_{CC}	60
74HC/HCT4052	dual 4-channel multiplexer/demultiplexer	V_{EE} to V_{CC}	60
74HC/HCT4053	triple 2-channel multiplexer/demultiplexer	V_{EE} to V_{CC}	60
74HC/HCT4066	quad bilateral switch	GND to V_{CC}	35
74HC/HCT4067	16-channel multiplexer/demultiplexer	GND to V_{CC}	60
74HC/HCT4316[2])	quad bilateral switch	V_{EE} to V_{CC}	65
74HC/HCT4351[2])	8-channel multiplexer/demultiplexer with select latch	V_{EE} to V_{CC}	60
74HC/HCT4352[2])	dual 4-channel multiplexer/demultiplexer with select latch	V_{EE} to V_{CC}	60
74HC/HCT4353[2])	triple 2-channel multiplexer/demultiplexer with select latch	V_{EE} to V_{CC}	60

All types except the 74HC/HCT4016, 4066 and 4067 have logic-level converters. R_{ON}: on-resistance of one switch.

[1]) V_{CC}: positive supply voltage; V_{EE}: negative supply voltage; GND: ground (0 V);
the voltage swing (V_{CC} to V_{EE}, or V_{CC} to GND) of the analog inputs/outputs may not exceed 10 V

[2]) not available in the HE4000B series

plastic SO packages. The 4351[1]), 4352 and 4353 multiplexers/demultiplexers (not available in the HE4000B series) have an on-chip address latch for improved microprocessor control; the 4316 switch, another new circuit, has a level-shifting facility and a chip select pin. All other types are pin-compatible with the HE4000B versions. When replacing HE4000B circuits with HCMOS versions, take account of the lower maximum-permitted supply voltage of HCMOS circuits (10 V for 74HC types; 5.5 V for 74HCT types) compared with 15 V for HE4000B circuits.

ANALOG SWITCH DESIGN

There are two designs of analog switch:

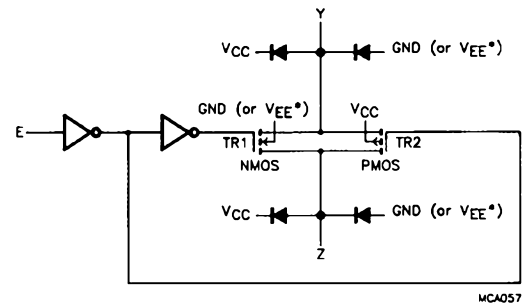
- that used in the 74HC/HCT4016 and in the 74HC/HCT4316
- that used in the 74HC/HCT4066 and in all HCMOS analog multiplexers/demultiplexers.

As a rule of thumb, for the lowest on-resistance, or the widest frequency response, use a circuit having the 4066 switch design. For the lowest crosstalk between the control input(s) and the analog inputs/outputs (for example, as required in sample-and-hold circuits), use the 4016 or 4316 circuits.

74HC/HCT4016 and 74HC/HCT4316 switch

The analog switch used in the 4016 and 4316 is formed by an NMOS transistor, TR1, and a PMOS transistor, TR2, connected in parallel, see Fig.1. To enable (close) the switch (also termed a transmission gate, or a pass-through gate), a HIGH level (up to V_{CC}) is applied to the gate of the NMOS transistor and an inverted version of this signal (LOW level: down to V_{EE}, or for the 4016, GND) to the gate of the PMOS transistor. Now, provided the gate-to-source voltage, V_{GS}, for each transistor is higher than the transistor threshold voltage, both transistors will conduct, forming a low-resistance path between the input/output pins Y and Z. Permissible voltages at the analog pins are from GND (or for the 4316, from V_{EE}) to V_{CC}.

When both the Z and Y terminals are near GND potential, the gate-to-source drive of TR1 is at its highest and there is a low-resistance path between Z and Y solely via TR1 (TR2 is off because its gate-to-source voltage is near to zero). Conversely, when the Z and Y pins are near V_{CC}, there is a low-resistance path solely via TR2, and TR1 is off. For voltages between GND and V_{CC}, although both TR1 and TR2 conduct, the total on-resistance of the transmission gate, R_{ON}, is higher than when TR1 or TR2 conducts alone, owing to the lower gate-to-source voltage of each transistor which has a large effect on the conductance. The on-resistance of the transmission gate also depends on the voltage between the source and substrate of each transistor (i.e. on the voltage between the analog pins, Y and Z, and V_{EE} or V_{CC}). Increasing this voltage increases the transistor's threshold voltage (about 0.7 V for HCMOS) which in turn increases R_{ON}. This 'substrate effect' as it is known is greater for an NMOS transistor than for a PMOS transistor, and is largest at low supply voltages. At high supply voltages (9 V), R_{ON} is relatively constant over the whole input voltage range.



* 74HC/HCT4316

Fig.1 Analog switch design used in the 74HC/HCT4016 and 74HC/HCT4316

Multiplexer/demultiplexer switch

Figure 2 shows the switch used in the 74HC/HCT4066 and in all HCMOS analog multiplexers and demultiplexers. The design of this switch eliminates the substrate effect in the case of the NMOS transistor, providing a flatter R_{ON} characteristic and a lower R_{ON} over the whole input voltage range, see Fig.3.

Compared with the design shown in Fig.1, the substrate of the NMOS transistor TR1 is not at a fixed potential but is connected (in the on state) to the analog pin Y via a second, low-resistance switch formed by transistors TR3 and TR4. As a result, the source-to-substrate voltage of TR1, and hence the threshold

[1]) The full type number of the HCMOS products mentioned in this publication is 74HC/HCTxxxx. Both the HC and HCT versions are specified for a temperature range of -40 °C to +125 °C. For brevity, where it isn't required to distinguish between HC and HCT versions, the prefixes 74HC and 74HCT are omitted.

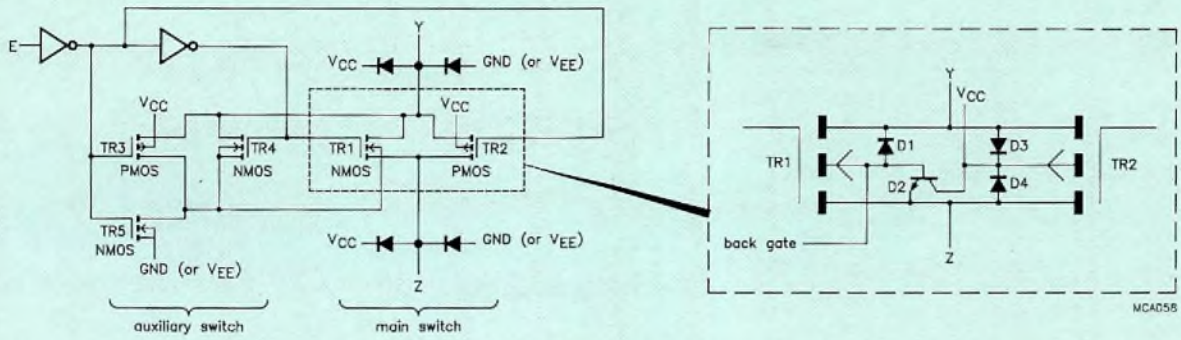


Fig.2 Analog switch design used in the 74HC/HCT4066 and in all HCMOS analog multiplexers/demultiplexers; (right) parasitic diodes of the main switch; switch turned on

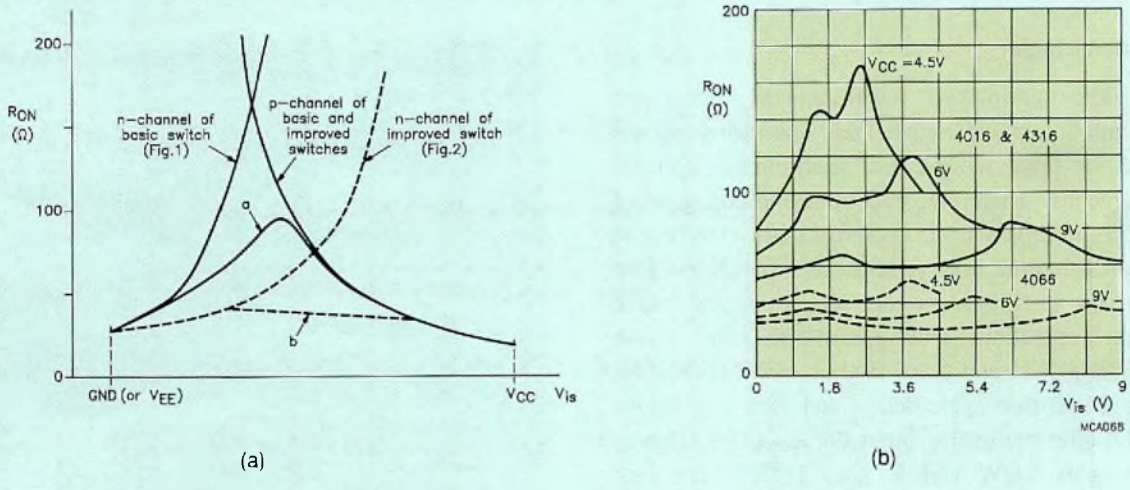


Fig.3(a) On-resistance, R_{ON}, of basic and improved switches as a function of the analog input voltage at a Y or Z pin, V_{is}, showing the individual contributions of each transistor. The on-resistance of a complete switch (n-channel plus p-channel) is also indicated – curve a for a basic switch and curve b for the improved switch.
(b) Typical on-resistance for the two types of analog switch for input voltages from 0 V to V_{CC}. I_S = 1 mA; T_{amb} = 25 °C

voltage of TR1, cannot increase with the voltage on the analog pins, reducing the on-state resistance of TR1 and consequently that of the whole transmission gate. In addition, because the source-substrate bias of TR1 is removed, this type of transmission gate has a wider frequency response than the simple gate shown in Fig.1.

Note that the substrate effect associated with the PMOS transistor TR2 cannot be removed in a similar way because the substrate of TR2 is the substrate of the transistor die itself. However, this is not a major drawback because, as already mentioned, the substrate effect is much smaller for a PMOS transistor.

For circuits having the auxiliary switch, there is a small restriction of the allowable voltage across the main switch in one direction (from Y to Z) owing to a parasitic NPN transistor, see Fig.2. When the voltage at Y is more than one diode drop (0.7 V) above the voltage at Z, the parasitic diode, D2, (the base-emitter junction of the NPN transistor) starts to conduct. Because the transistor's collector is connected to V_{CC}, current can flow from V_{CC} to the Z pin. To prevent this, ensure that $V_Y < V_Z + 0.4$ V. In the opposite direction (from Z to Y), there are no restrictions on the voltage across the switch other than V_{EE} (or GND) and V_{CC}.

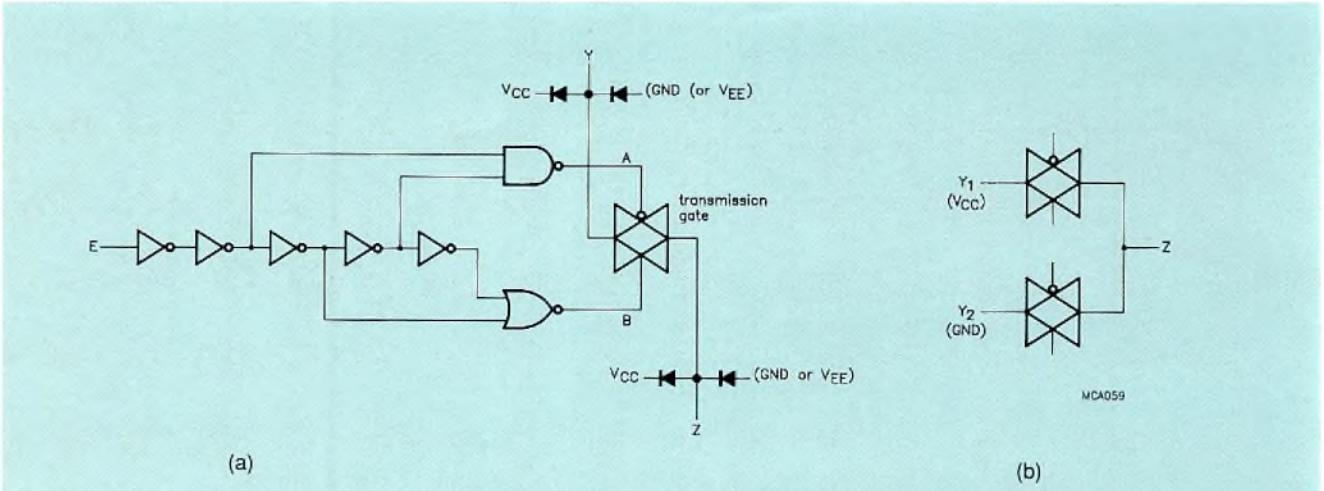


Fig.4 Control logic for each transmission gate (a) ensures 'break-before-make' switch operation, preventing two switches conducting simultaneously as could occur in (b) from short-circuiting the GND and V_{CC} supplies

Switch control logic

In an analog multiplexer, when several inputs are switched onto a common output, only one switch should conduct at a time to prevent short-circuit currents through switches. Therefore, each transmission gate of an HCMOS multiplexer has control logic (see Fig.4) which ensures that the time to turn the transmission gate off is less that to turn it on (i.e. which ensures 'break before make' operation). During turn-off, point A (see Fig.4(a)) goes HIGH and point B goes LOW (indicating the switch is off) three gate delays and four gate delays respectively, after the enable input E goes LOW. During turn-on, A goes LOW and B goes HIGH, five gate delays and six gate delays respectively, after the enable input goes HIGH.

The 'break' (disable) time of a switch is specified in the HCMOS data sheets for a 1 kΩ/50 pF load, and is measured to a 10% change in the output voltage at a Y or Z pin, V_{os}, see Fig.5. This load contributes 5 ns (t_2–t_1) to the specified switch turn-off time. When checking a circuit for break-before-make operation, subtract 5 ns from all the 'OFF' times specified in the data sheet. If the result is less than the turn-on time, break-before-make operation is assured.

Supply operating voltage

A major attribute of HCMOS switches is their wide supply voltage range. For 74HC circuits, the V_{CC} to GND range which can be considered as the supply voltage for the digital circuitry is 2 V to 10 V – a benefit found only in HCMOS technology. And the supply voltage for the analog circuitry is the same.

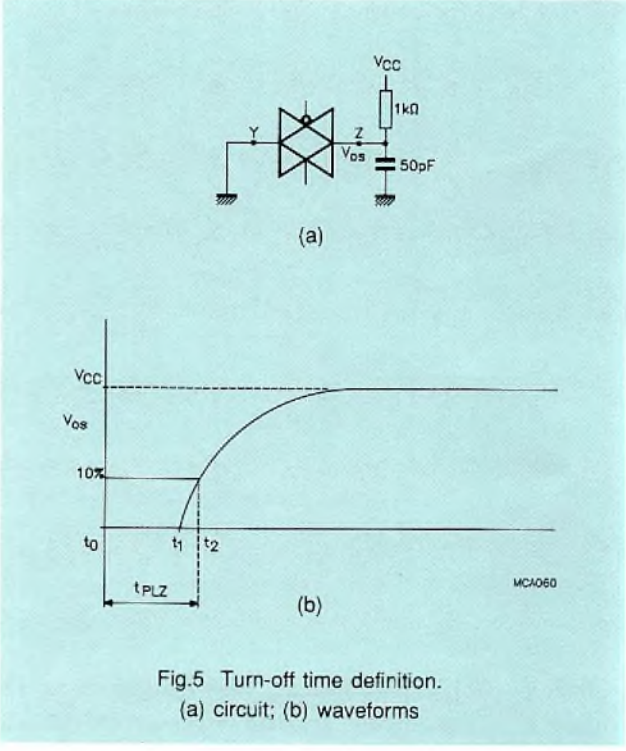


Fig.5 Turn-off time definition.
(a) circuit; (b) waveforms

The availability of virtually a square operating area from 2 V to 10 V, see Fig.6, allows many possibilities for digital level conversion for circuits with a V_{EE} pin (see 'Application examples'). As level converters, HCMOS analog switches can operate as digital gates. For example, in a 74HC4053 2-channel analog multiplexer, Y_1 may go to V_{CC} and Y_0 to V_{EE}, causing Z to switch between V_{CC} and V_{EE} but controlled by the digital signal on the select inputs (the exact voltage swing on Z can be adjusted to suit individual

requirements anywhere within the operating area shown in Fig.6.). For example, 2 V digital signals can be converted to 8 V signals in the analog circuitry. Another useful feature is the ability to interface between industry-standard TTL digital levels and +5 V to −5 V analog circuitry.

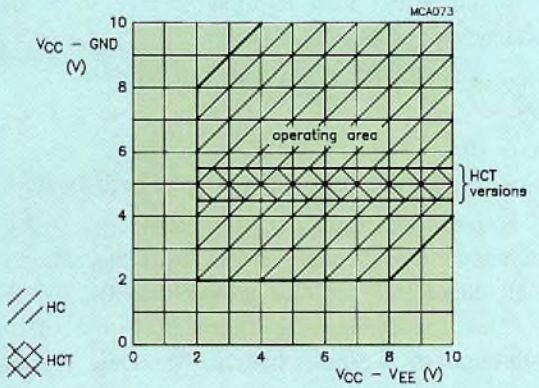


Fig.6 Operating supply voltage range for a 74HC switch or multiplexer. For completeness, the operating range for 74HCT circuits is also shown

Overvoltage protection

All HCMOS multiplexers/demultiplexers and analog switches have input-protection diodes at their analog input/output pins, see Figs 1 and 2, which protect the devices when:

- the analog input/output voltage exceeds either the positive or the negative supply voltage rating
- an electrostatic discharge (ESD) appears on the analog pins. Protection is superior to that of the digital inputs, and is similar to the standard output protection.

Unlike the standard protection circuitry for the digital inputs of HCMOS circuits, these analog-input protection circuits don't have a current-limiting forward resistance, so the maximum permissible diode current of 20 mA can be attained. Protection is limited to short-term, for example, voltage transients on the supply rails. For long-term protection, a resistor should be connected to the analog input to limit the diode current to its maximum permissible value. However, such protection does increase the on-resistance.

COMPLETE ANALOG MULTIPLEXER/ DEMULTIPLEXER

Figure 7 is a schematic of a typical HCMOS multiplexer/demultiplexer – the 74HC/HCT4051. A logic level converter converts LOW (0 V) levels at any of the three select address inputs, S_0, S_1 and S_2, to V_{EE}. HIGH levels are unaltered at V_{CC}. Level conversion is necessary to match the control signals to the V_{CC} to V_{EE} range of the analog signals. Following the level converter, a 1-of-8 decoder generates the switch control signals corresponding to the 3-bit select address. One side of each switch is connected to a common pin (Z). Since the switches are bidirectional, the circuit can operate as a multiplexer or a demultiplexer.

The Fig.7 arrangement is also used in the 4052/4053, and in the 4351/4352/4353 which have an address latch. The 4067 doesn't have a level converter, consequently its analog voltage range is GND to V_{CC}, instead of V_{EE} to V_{CC}.

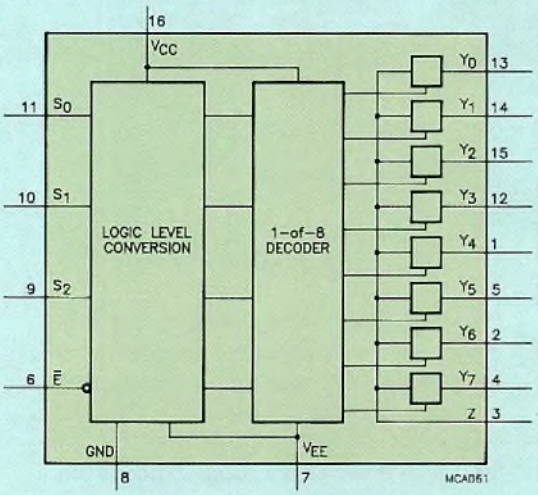


Fig.7 4051 analog multiplexer/demultiplexer

SWITCH OFF-STATE SIGNAL FEED-THROUGH

Figure 8(a) is an equivalent circuit which illustrates the small feed-through across an open switch. Although both transistors of the switch are off, their combined drain-to-source capacitance (C_{DS}) provides an AC signal

path between the Y and Z pins. From Fig.8(a), this feed-through is:

$$-10\log\{1 + (1 + C_L/C_{YIZ})^2\}/(2\pi f R_{EQ} C_{YIZ})^2 \text{ dB}$$

where R_{EQ} is the equivalent output resistance, in this case, R_L, with the other Y pins floating.

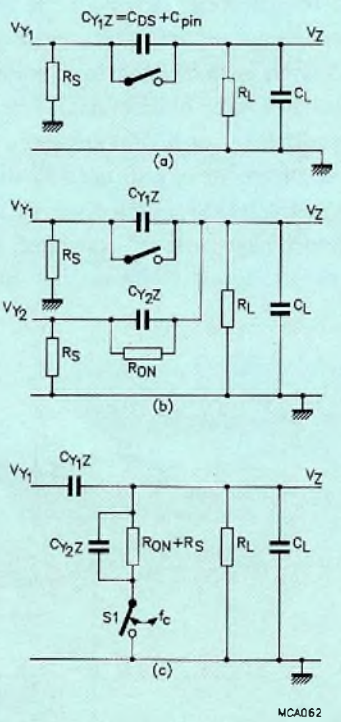


Fig.8 Equivalent circuits illustrating (a) the feed-through via the drain-source capacitance of a switch in the OFF state; (b) the feed-through for a multiplexer (static condition); (c) the feed-through for a multiplexer switching at f_c. Only two switches are shown. C_{Y2Z} is insignificant in comparison with C_L and R_{ON}

The advanced design and manufacture of an HCMOS switch restricts the leakage to −50 dB (DIL package) at f = 1 MHz, R_L = 600 Ω and C_L = 50 pF, corresponding to a C_{YZ} of 0.85 pF, most of which is due to the pin-to-pin capacitance of the package and the layout of the bonding wires. The dynamic characteristics are therefore determined to a large extent by the pin-to-pin capacitances, and therefore by pin positions. For the lowest feed-through, the use of SO packages with their low pin capacitance is recommended. In addition, pay attention to the layout of tracks on a PCB.

In a multiplexer, feed-through across the switches causes a small component from switched-off inputs to appear at the output. The static feed-through (the feed-through when the multiplexer is not switching) is less than that of a single switch, due to the on-resistance of the selected switch and the internal resistance, R_S, of the signal source connected across the load resistance, see Fig.8(b).

When the multiplexer is switching at a frequency of f_C, the situation is as shown in Fig.8(c). Provided R_{ON} is very much less than R_L, the average value of the equivalent output resistance is:

$$R_{EQ\ AV} = [R_{ON}(T - T_{open}) + R_L T_{open}]/T$$

where:

T is $1/f_C$;

T_{open} is the time the switch is open each cycle.

If f_C is zero, and $T_{open} = 0$, R_{EQ} equals $R_{ON} + R_S$ and the dynamic feed-through is less than the static feed-through. Since R_{EQ} can't be greater than R_L, the worst-case value for dynamic feed-through is the off-signal feed-through of a single switch. The Data Handbook, IC06N, gives this worst-case value as a function of the analog frequency for each switch and multiplexer/demultiplexer (for R_L = 600 Ω, C_L = 50 pF). Typically, the feed-through is −50 dB.

CROSSTALK (SELECT INPUT TO ANALOG INPUT/OUTPUT)

The crosstalk between a select input and the analog pins is caused by the gate-source and gate-drain capacitances of the MOS transistors of a transmission gate, see Fig.9. Although the anti-phase switching of the NMOS and PMOS transistors suppresses some of the interference, a part of the select pulse reaches the analog pins because the two transistors don't switch on and off exactly together.

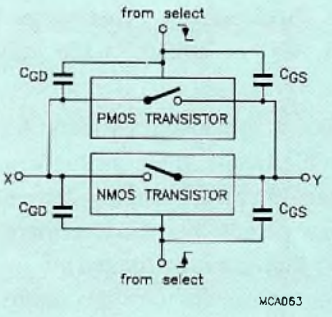


Fig.9 Equivalent circuit for crosstalk between the select input and analog output of an HCMOS switch

With the improved transmission gate of the multiplexer, the switching noise increases at the analog pins slightly, owing to the switching pulses at the back gate (parasitic gate) of TR1 which can produce crosstalk at the Y and Z pins while the main switch turns on, especially when Y and Z are biased via high impedance sources, or are at voltages above GND, see Fig.10. This crosstalk is caused by the charging of the back gate of TR1 from GND to the voltage at the Y (or Z) pin via the auxiliary switch while the main switch turns on. The simple switch of the 4016 and 4316 produces less crosstalk than the switch used in the multiplexers, because the back gate of TR1 won't be switched.

To minimize crosstalk, the use of SO packages with their low pin capacitances is recommended for HCMOS analog designs.

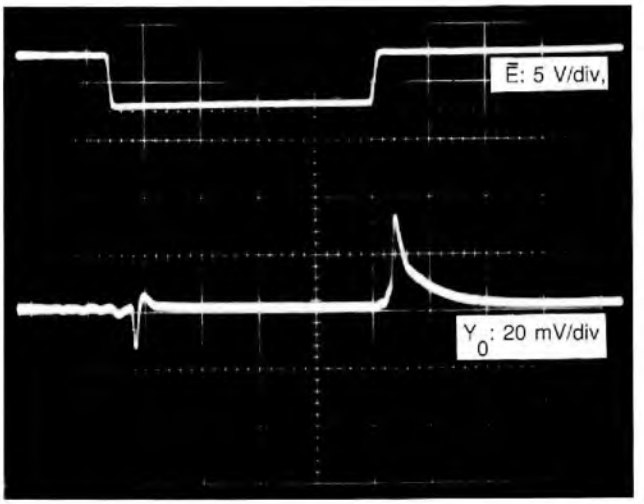


Fig.10 Crosstalk caused by switching a transmission gate with an auxiliary switch. In audio applications, for example, when switching between channels, this crosstalk should be suppressed by a simple muting circuit. Circuit: 74HC4051. Horizontal scale 50 ns/div

APPLICATION EXAMPLES

(Figures 11 to 16 appear overleaf)

Analog multiplexer in a data acquisition system

Figure 11 shows a typical data acquisition system using a 4351 analog multiplexer to select the input channel and a 4016 switch in the sample-and-hold circuit. The 4351 results in a low input offset voltage, while the 4016 is chosen owing to the extremely low crosstalk between its control input and analog pins. A full description of this circuit is given in Ref.2.

Fast 4-bit DAC

Figure 12 is the circuit of a 4-bit DAC using two 74HC/HCT4016 circuits. When a digital input is HIGH, a reference voltage, V_{ref}, is applied to the corresponding binary-weighted resistor (R1, R2, R3 or R4); when the input is LOW, the resistor is grounded.

The values of the resistors were selected assuming an on-resistance of 90 Ω for the 74HC/HCT4016 switch. The settling time to ±0.5 LSB for a full-scale change is 180 ns for a 1 MΩ load in parallel with 20 pF (oscilloscope input). The maximum deviation from the expected output of the converter is about 2.5%.

Level converters

A wide operating supply voltage area, see Fig.6, distinguishes HCMOS analog switches from other commercially-available products, allowing level conversion over a wide range of voltages. For example, the circuit shown in Fig.13 in which the select lines are used as inputs can be used to convert '2 V' digital levels to +8 V levels. Figure 14 shows a circuit using a 74HC/HCT4316 quad-switch to convert 0/5 V levels to −5/+5 V levels.

Audio source selector

Figure 15 shows a circuit which can select one of four stereo inputs as used in a signal-source selector for an audio amplifier. The opamp is a NE5532 chosen for its low noise. Crosstalk between an unselected input and the associated multiplexer output is −68 dB, and the stereo channel separation is 71 dB. The signal-to-noise ratio is 98.5 dB(A), or 85.1 dB(A) according to CCIR-468. (Noise measurement with Sennheiser UPM550, generator internal resistance 60 Ω). For input signals up to 2 V, the distortion is <0.001% over the whole audio band.

Video source selector

Figure 16 shows a video source selector with the switches arranged for minimum leakage and switching noise. The two pairs of switches in each signal path are driven in anti-phase and have a grounding switch between them. When closed, the grounding switch short-circuits the leakage signals of the unselected channel.

A 4066 switch is chosen, owing to its wide bandwidth. The opamp has a differential output but is used single-ended. The overall gain of the circuit is unity. The −3 dB upper frequency limit is about 22 MHz. Channel separation at a frequency of 10 MHz is 45 dB.

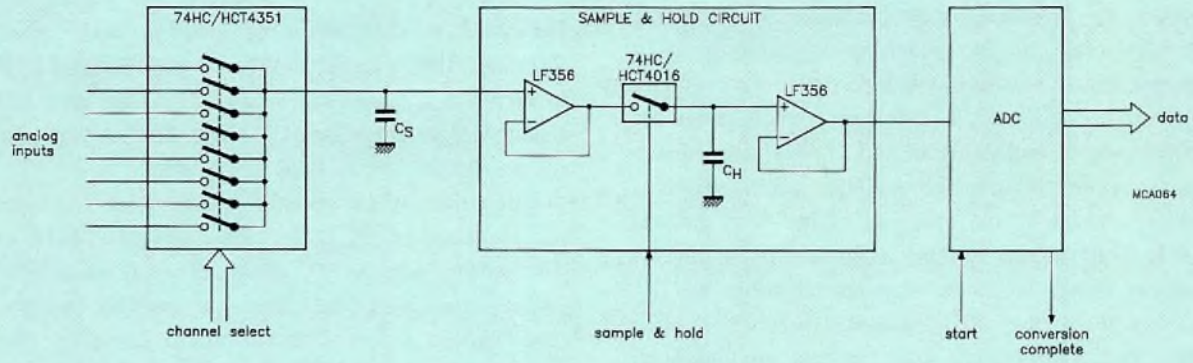


Fig.11 Multiplexer data-acquisition system

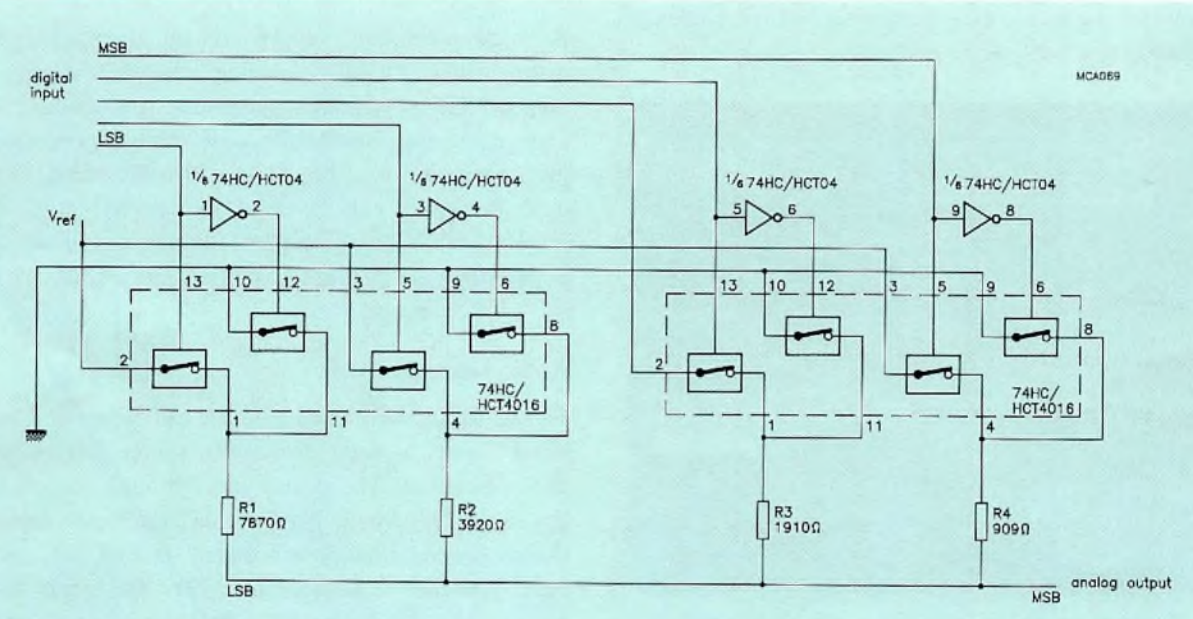


Fig.12 4-bit DAC using two 4016 circuits. Supplies not shown

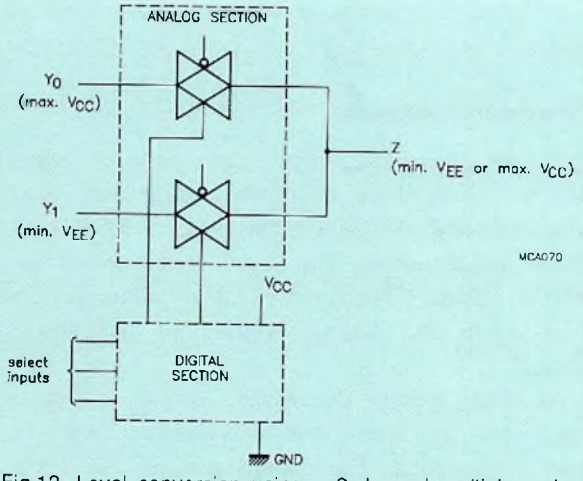


Fig.13 Level conversion using a 2-channel multiplexer in which the digital select inputs (GND or V_{CC}) are converted to a 'digital' signal output at the Z pin

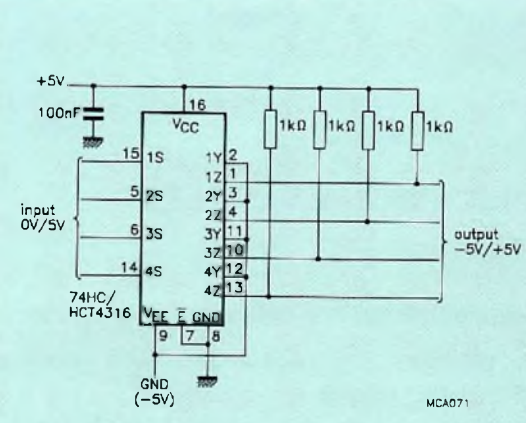


Fig.14 Level converter using a 4316 quad bilateral switch

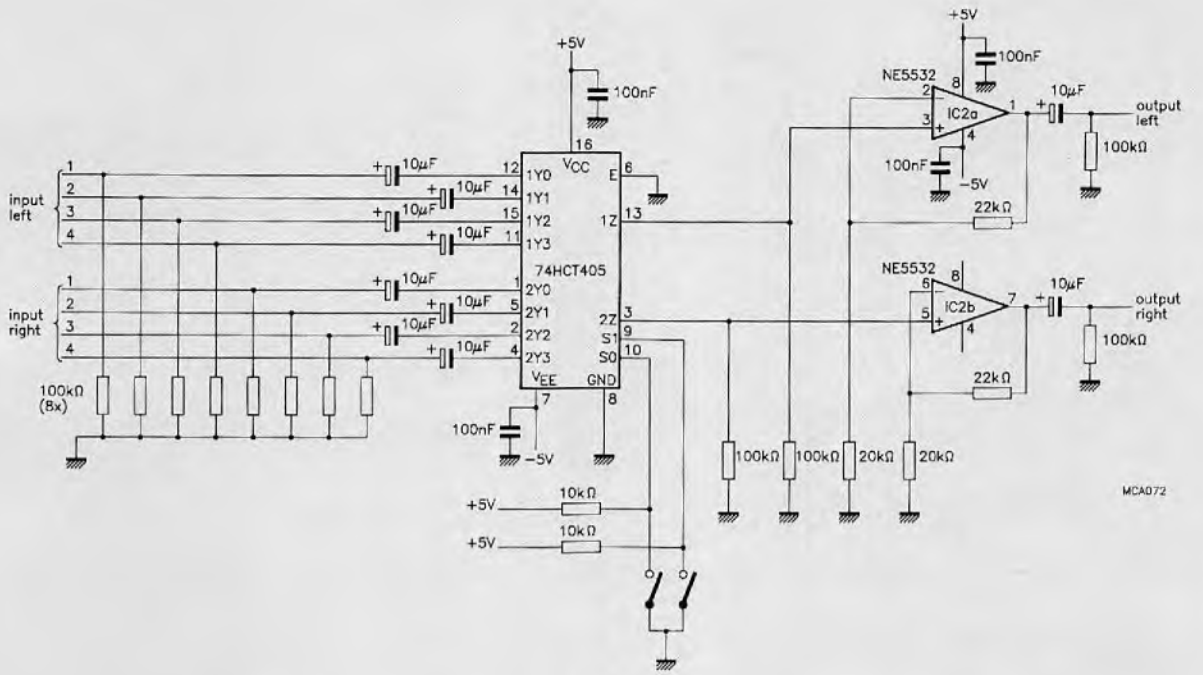


Fig.15 Four-channel stereo audio source selector using a 4052 multiplexer

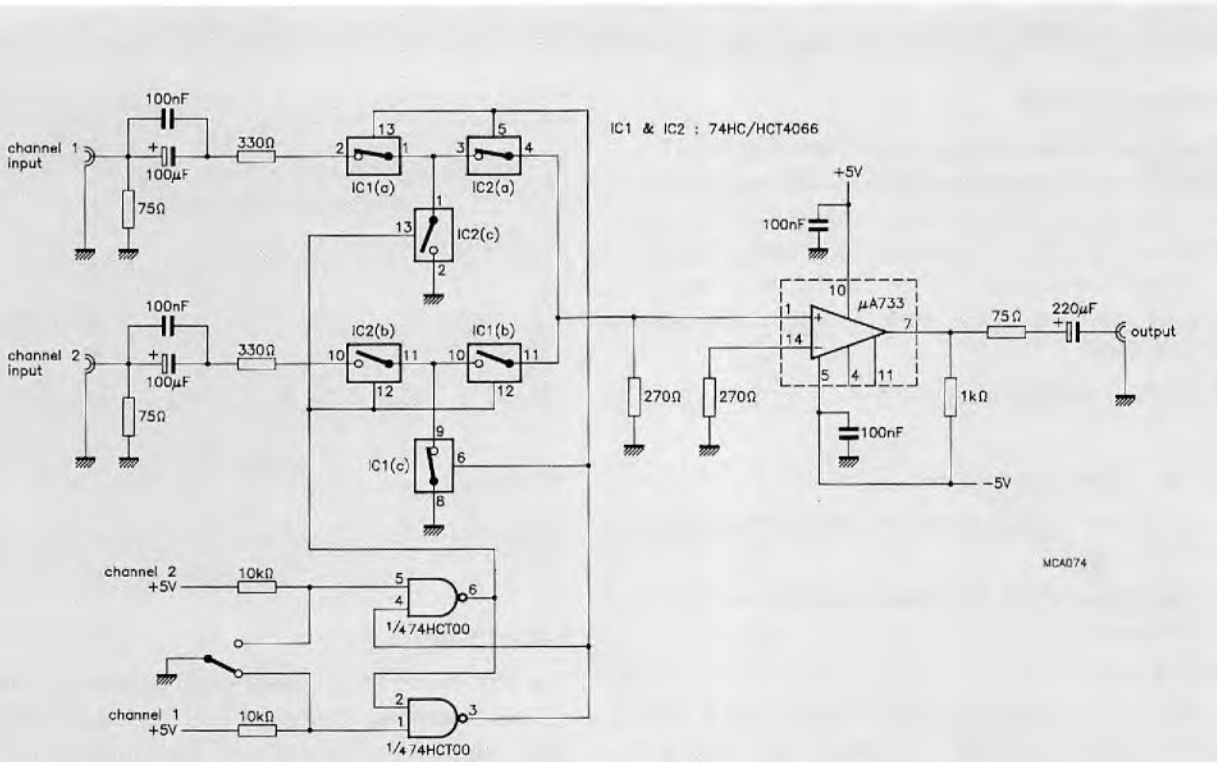


Fig.16 Video source selector using two 4066 circuits

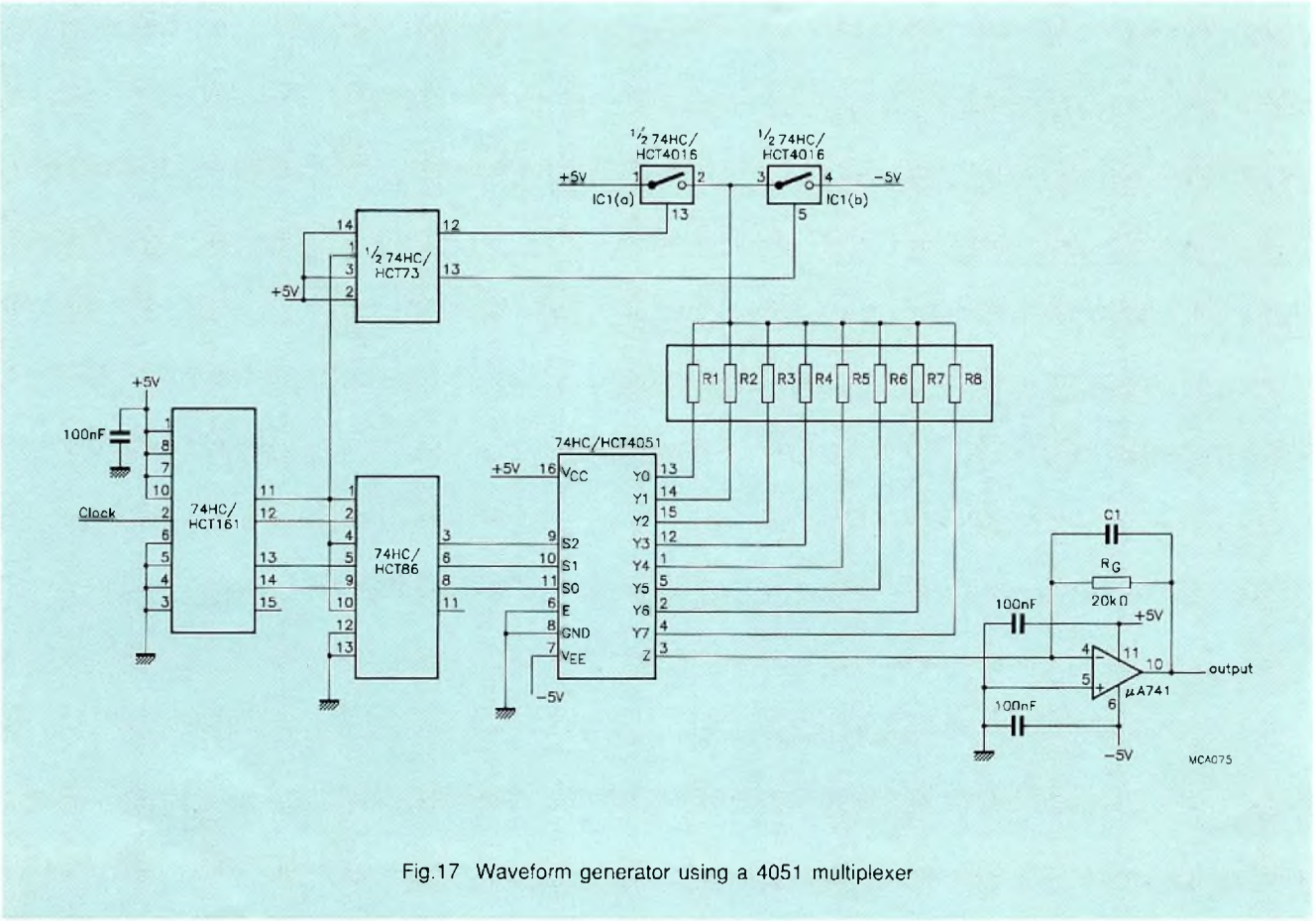


Fig.17 Waveform generator using a 4051 multiplexer

Waveform generator

The heart of the waveform generator shown in Fig.17 is a 4051 8-channel analog multiplexer. The multiplexer, which is controlled by a counter, switches in different resistances at the input of the opamp, altering its gain. The switched resistances can be altered to produce a variety of waveforms, see Table 2. The values were calculated from:

$$Ri = (5/V_A)(32fR_G/i) \quad k\Omega$$

where:

i is the output level increment (1 to 8);

V_A is the instantaneous level of the output increment in volts;

f is the frequency of the output waveform in kHz set by the counter;

R_G = 20 kΩ.

The 74HCT40161 counter together with the EXOR gate, 74HCT86, form an up/down counter. The 74HCT73 operating as a T flip-flop inverts the output signal periodically. Capacitor C1 gives the opamp a low-pass characteristic which suppresses the counter frequency (32 times the output frequency).

TABLE 2
Resistances for the sinewave and sawtooth generator shown in Fig.17.

	sinewave 2 V_{p-p} (kΩ)	sawtooth 1.5 V_{p-p} (kΩ)
R1	270	1000
R2	130	330
R3	91	200
R4	68	150
R5	62	110
R6	56	91
R7	51	75
R8	50	68

Logic circuits

The 4053 multiplexer can be used to generate a variety of logic functions, see Fig.18 (Ref.3). The advantage of using this circuit instead of pure gate components is that up to three different logic functions can be implemented with a single component. Besides saving space, the HCMOS multiplexers have a lower output impedance (R_{ON} < 100 Ω) than CMOS logic gates and inverters.

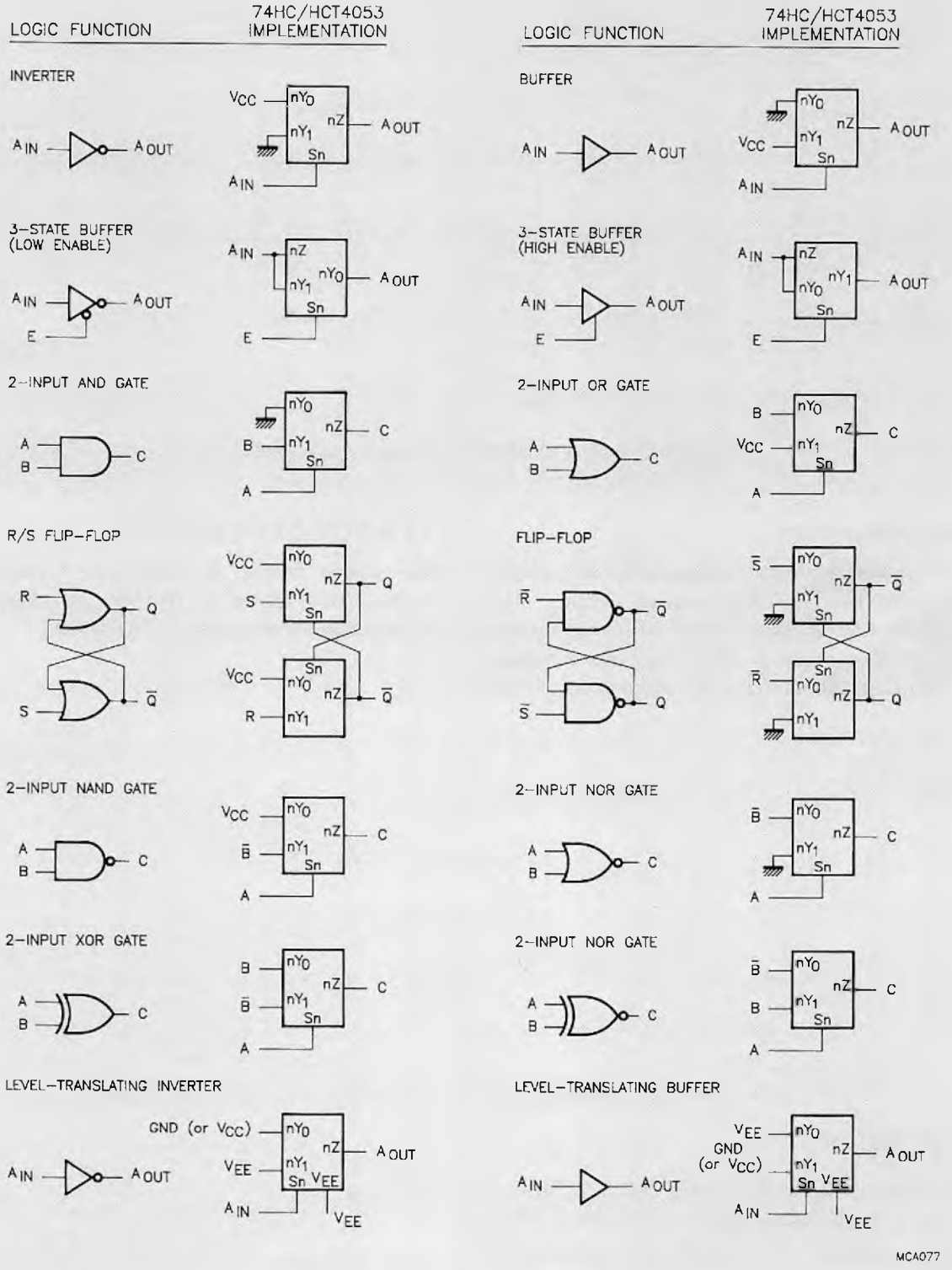


Fig.18 Logic functions can be implemented using 74HC/HCT multiplexers. Each function shown here requires only one third of a 4053 circuit, except for the flip-flops (two thirds)

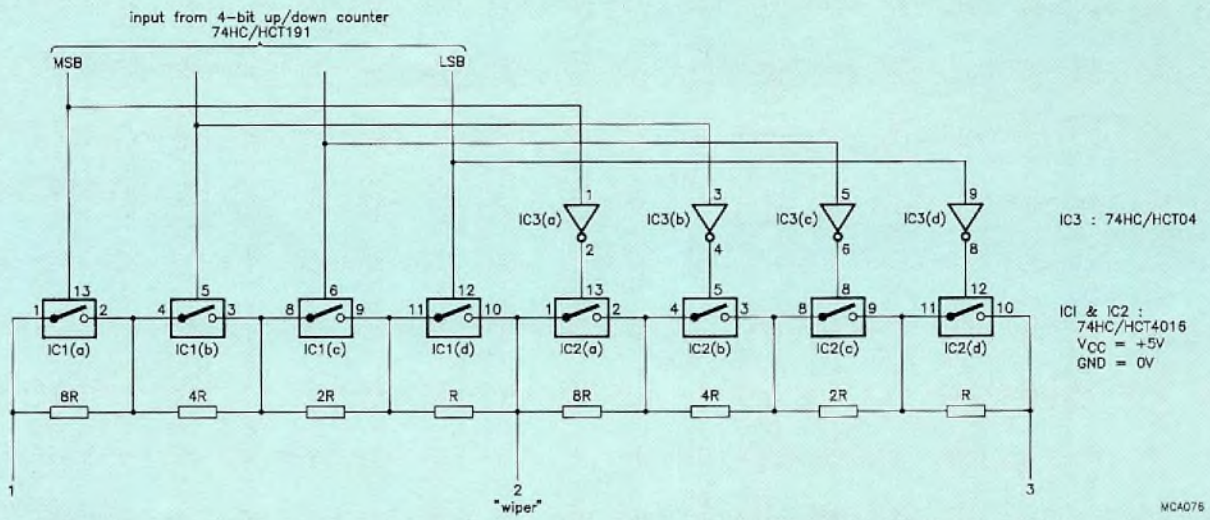


Fig.19 Electronic potentiometer using two 4016 switches

Electronic potentiometer

Figure 19 shows a simple digitally-controlled potentiometer using two 74HCT4016 quad switches. The signal from a 4-bit up/down counter is used to operate the switches. The circuit could be used for automatic offset compensation of opamps in data-acquisition systems.

ACKNOWLEDGEMENT

The author wishes to thank Mr. T. Stork, Philips Applications Laboratory, Hamburg, Germany for his assistance in the preparation of this article.

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2. Analog switches & multiplexers/demultiplexers, HCMOS Designer's Guide – Advance Information, ordering code 9398 639 70011, Philips Components, 1989.
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The Polygon gun... ...for a cleaner, sharper electron spot

JAN GERRITSEN and ERICH HIMMELBAUER

One of the major advances to be introduced into Philips' latest colour picture-tube range is the new 'polygon' electron gun. Known by this name because of the shape of its central aperture, the new gun solves a problem that has beset unitized gun designs (Fig.1) since their inception more than a decade ago: namely the problem of minimizing aberrations and associated effects in the electron-optical lens system to produce a sharp, clean electron spot.

The size of the electron spot striking the phosphor depends principally on four factors:

- *lens magnification*: spot diameter = object diameter × magnification (the object being the diameter of the electron-beam crossover in the object plane of the electron-optical lens system). Spot diameter can therefore be reduced by reducing the lens magnification, which can be done by increasing the diameter of the main lens
- *lens aberrations*: which cause the focal point of the lens system to be highly sensitive to electron trajectory. Electrons entering the main lens near the axis are not brought to the same focus as those entering near the periphery, causing axial spreading or blurring of the focal point and hence a smearing of the electron spot (located at the circle of least confusion). As with magnification, lens aberrations can be reduced by increasing the lens diameter
- *space-charge repulsion*: the intrinsic repulsion of the negatively-charged electrons causing further defocusing of the electron spot
- and finally, *deflection defocusing*, which at the tube corners can cause further increase in spot size, a phenomenon particularly troublesome in self-converging deflection systems.

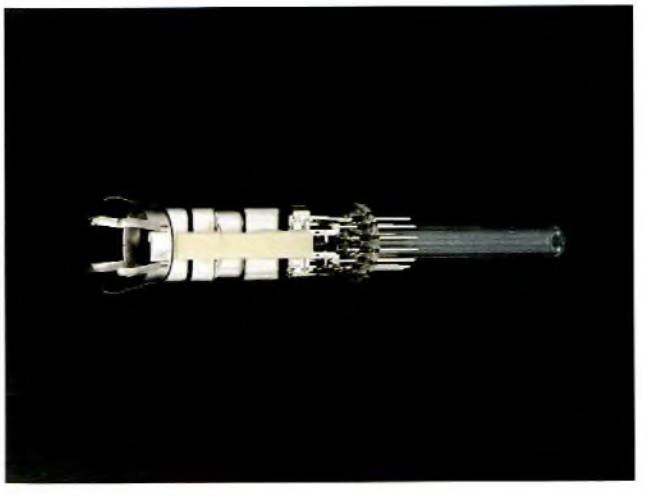


Fig.1 The unitized gun is formed by three physically discrete electron-optical units connected rigidly together, providing the benefits of a physically integrated system (compactness, close tolerances) whilst still maintaining electrically discrete electron-optical systems

With the exception of deflection defocusing, all these problems can be solved by increasing the lens diameter, i.e. by increasing the size of the three circular apertures in the main lens of the gun. A solution unfortunately not easy to realize under the physical constraints imposed by the narrow necks of modern tubes.

OVERLAPPING LENS SYSTEMS

A solution to this problem has been provided by electron guns that allow the electron-optical systems in the main lens to overlap and hence to produce larger electron-optical lenses than would be possible with conventional (non-overlapping) systems. Though highly successful at reducing spot size, these guns may still leave some residual aberrations generated by non-radially symmetric field components.

POLYGON - AN OVERLAPPING SYSTEM WITH ABERRATION COMPENSATION

These residual aberrations are significantly reduced in Philips' new 'polygon' gun (Fig.2), a development of the overlapping system in which the larger electron-optical lens is formed by an oval ridge (Fig.3), surrounding three apertures whose profiles have been precisely configured to compensate the non-radially symmetric electric field components. For ease of manufacture, the central aperture was originally in the shape of a polygon (hence the gun's name), but in current guns the aperture approximates an ellipse (with higher order terms).

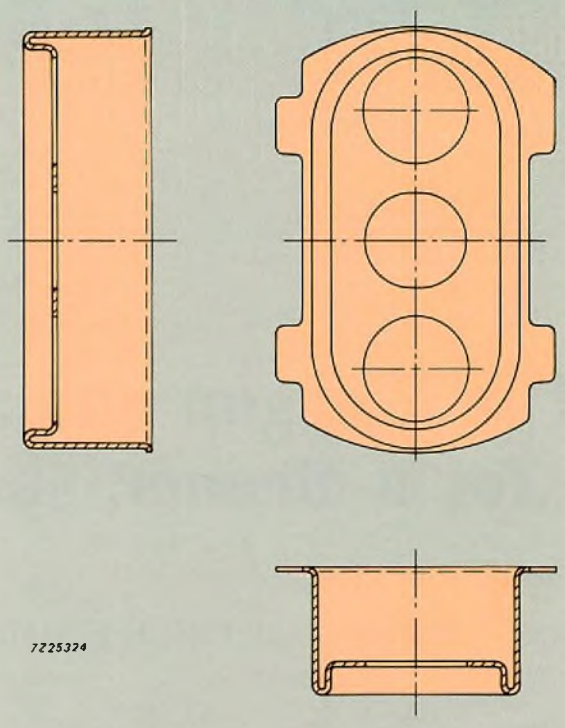


Fig.2 In the 'polygon' gun the three circular apertures of the conventional gun are replaced by an oval ridge, forming, in effect, a larger electron-optical lens, surrounding three apertures whose profiles have been precisely configured to compensate the non-radially symmetric electric field

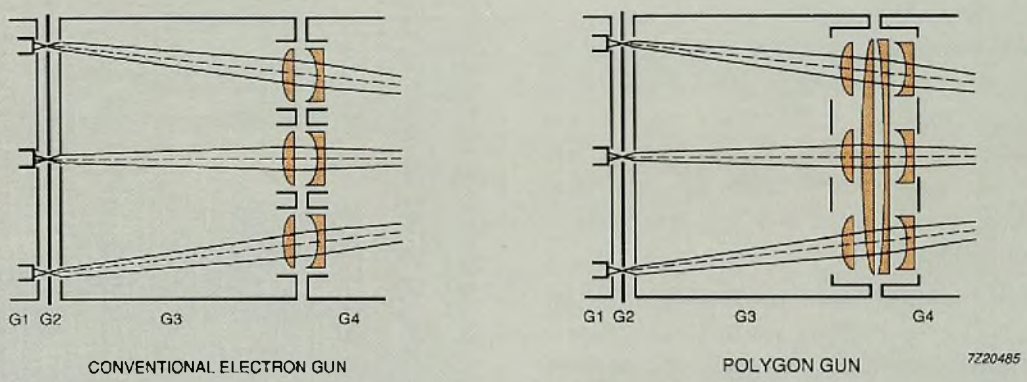


Fig.3 The larger electron-optical lens provides the dual benefits of lower spherical aberration and lower magnification for a sharper spot on the phosphor screen. It also allows the use of a somewhat wider electron beam, reducing space-charge repulsion and leading to further increase in spot sharpness

The important consequences of using the polygon gun are adequately demonstrated by a specific example: its use in the 33-inch colour picture tube (neck diameter 29.1 mm). For proper landing on the phosphor, the screen/mask geometry dictates that the three electron beams must pass through the lens 6.5 mm apart. So theoretically, this should be the maximum lens diameter attainable. Mechanical constraints dictate a minimum distance between the apertures of around 1 mm so in reality the lenses can be no larger than 5.5 mm. The polygon gun, however, in the same tube, gives an effective lens diameter of around 7.1 mm with all the consequent reductions in magnification, lens aberrations and space-charge repulsion.

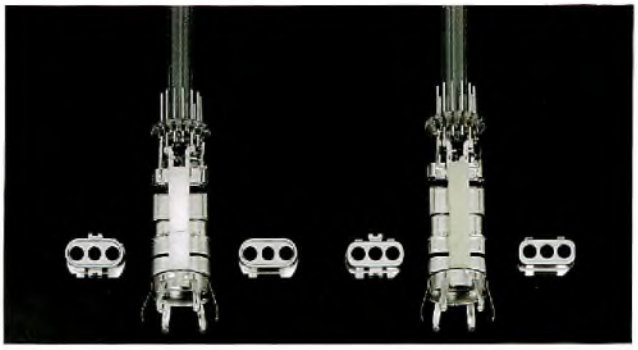


Fig.4 Standard electron gun with circular apertures (right) and polygon gun (left) with apertures configured to compensate the non-radially symmetric field generated by the lens formed by the oval ridge

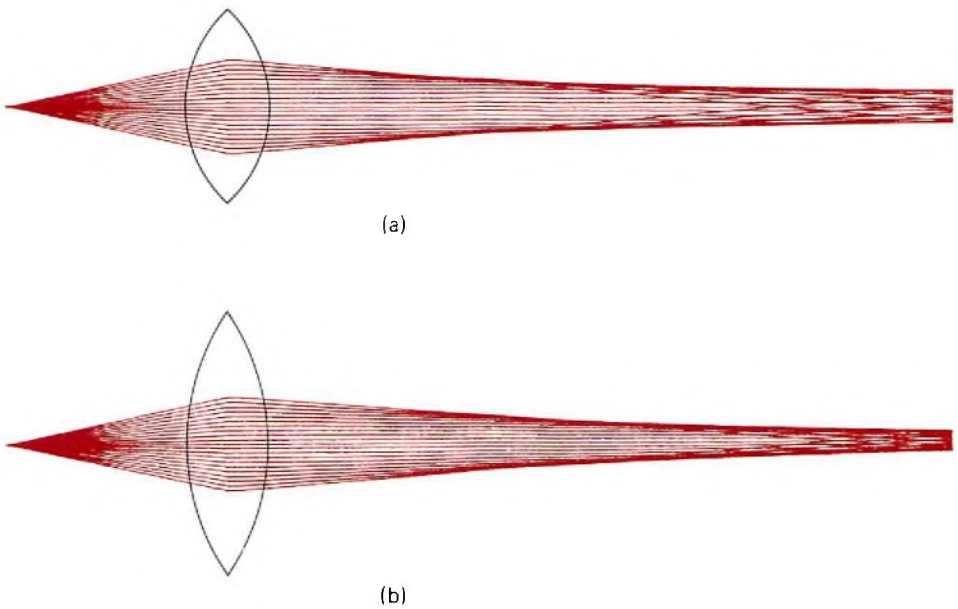


Fig.5 Schematic representation of electron trajectories produced (a) by a conventional gun and (b) by a polygon gun

Figure 5 compares the electron trajectories produced by a conventional gun with those produced by the polygon gun, and clearly demonstrates the reduction in spot size possible with the latter.

TUBE PERFORMANCE WITH THE POLYGON GUN

Figure 6 compares the spot diameter (screen centre) of a prototype tube incorporating a polygon gun with that of our 66FS tube incorporating a conventional gun, and shows that reductions in spot size of up to 15% are possible with the polygon gun.

The new gun is shortly to be introduced into our complete colour monitor-tube range, and will also gradually be introduced into our TV colour-picture tube range starting with the 33-inch tube.

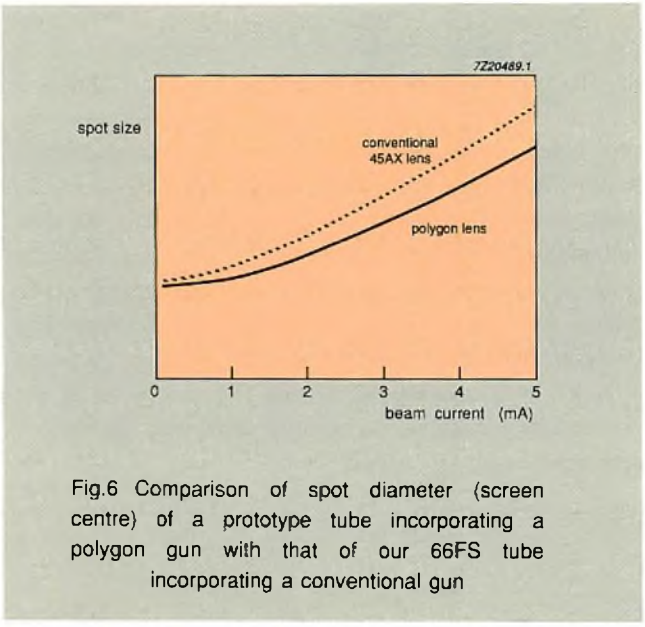


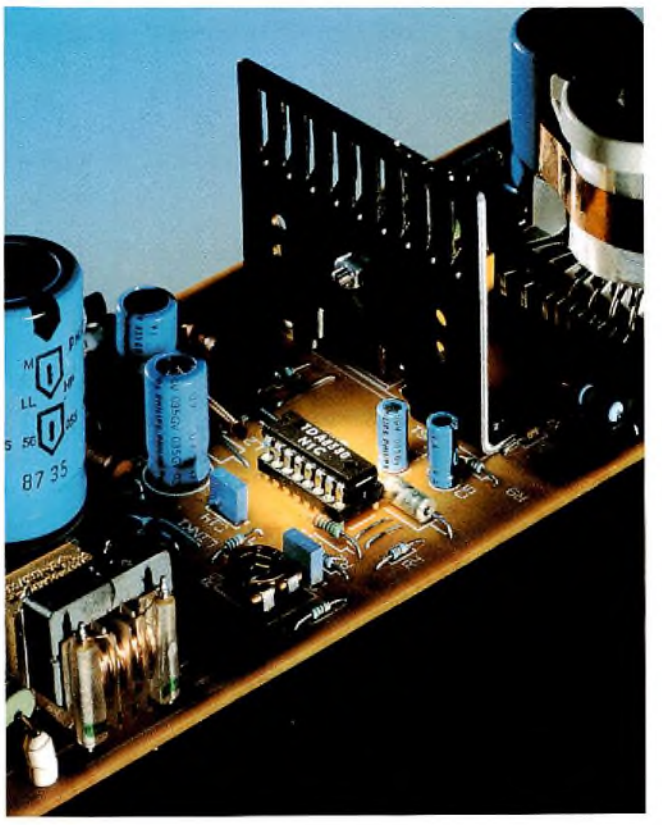
Fig.6 Comparison of spot diameter (screen centre) of a prototype tube incorporating a polygon gun with that of our 66FS tube incorporating a conventional gun

Integrated SMPS control circuit TDA8380

NICK PICHOWICZ

It's well-known that switched-mode power supplies are more efficient, smaller and lighter than conventional series regulator power supplies. However, the circuitry required to incorporate the necessary overload protection and to control the switching duty factor to compensate mains voltage and load variations is complex. To alleviate this problem and make an SMPS much easier to design, we have developed the integrated SMPS control circuit TDA8380 which offers many attractive operating facilities, even in simple SMPS circuits.

The TDA8380 can drive a variety of types of SMPS with a forward or flyback converter which can run in continuous or discontinuous current mode. It controls the SMPS power throughput and regulation by pulse-width modulation (PWM) of a fixed frequency drive signal for a bipolar or PowerMOS SMPS power switching transistor. PWM control is achieved by varying the duty factor of the SMPS power transistor switching between 0% and 80%.



Integrated SMPS control circuit TDA8380 being used in a 120 W SMPS evaluation board

The TDA8380 is shown in block diagram form in Fig.1. The IC is in a 16-pin DIL package and incorporates the following features:

- internally stabilized supply voltage
- direct initialization for battery operation
- low starting current initialization for mains operation
- high and low supply-voltage protection
- externally programmable reference currents
- operating frequency 10 to 100 kHz, can be synchronized
- internal error amplifier which can be frequency compensated externally
- access to pulse-width modulator to facilitate use of an alternative external error amplifier
- fail-safe control loop
- duty factor foldback
- slow-start or soft-start options
- anti-double-pulse logic
- direct-drive output stage
- first level cycle-by-cycle overcurrent protection
- second level trip overcurrent protection
- protected against power transistor short-circuit
- demagnetization sensing
- remote on-off switching facility.

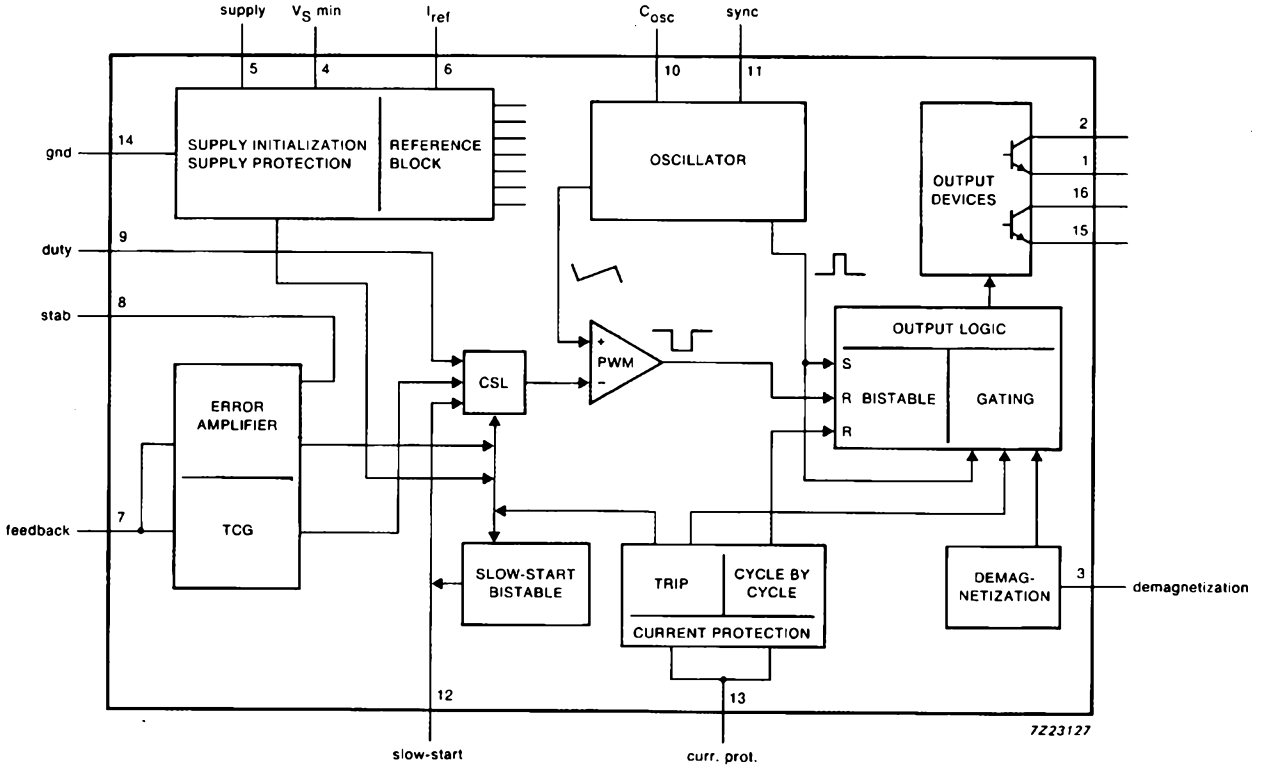


Fig.1 TDA8380 Block diagram

INTERNAL POWER SUPPLIES

Internally stabilized supply voltage

The TDA8380 has a fixed and internally stabilized supply voltage of 7.0 V which drives most of the internal circuitry, exceptions being the initialization circuit, the output stage and the voltage stabilizer. This relatively low operating voltage, derived from a bandgap-based reference, is consistent with the IC design which uses a small chip with maximum reliability.

Triggered initialization circuit

The internal power supply has an on-chip initialization circuit which is triggered at +17 V. The initialization logic circuit performs three functions as follows:

- It enables the internal stabilized bandgap reference supply voltage circuit
- It allows a slow-start capacitor at pin 12 to charge upon receipt of the bandgap reference signal
- If the trip protection operates, the initialization logic circuit pulls down the controlled slicing level (CSL) for the oscillator sawtooth before the next oscillator flyback period. It discharges the slow-start capacitor at pin 12 and disables the bandgap reference

Direct 12 V supply

The triggered initialization circuit (with trigger level normally set to 17 V) can be disabled by connecting the low supply protection pin (V_{smin}, pin 4) to the supply pin (pin 5) to make the IC operate as soon as its power supply voltage reaches 8.4 V, the minimum permissible supply voltage. In this mode, there is no take-over supply from the SMPS transformer and the supply source must directly provide all the current needed by the IC. This condition can be fulfilled by a car battery, for example.

Low starting current initialization for mains operation

The TDA8380 is initialized when the voltage on the supply pin 5 (derived from the rectified mains input) reaches 17 V. For low starting current initialization, a single low wattage resistor between the rectified mains input to the SMPS and pin 5 is used to define the charging current of the IC supply reservoir capacitor. When the voltage across this capacitor reaches 17 V, the IC initializes and a take-over winding on the SMPS transformer then provides the supply for the IC. A start-up current of 1 mA gives a 'dead time' of approximately 17 ms/µF of reservoir capacitance.

Supply take-over

If the take-over supply is derived from a forward rectifier connected to an auxiliary winding of the SMPS transformer, take-over will be almost instantaneous. If a flyback rectifier is used, the time before take-over will depend on the slow- or soft-start time and will be appreciably longer. This means that the IC supply voltage will be temporarily decreased. If the take-over time is long, the value of the supply reservoir capacitor will have to be increased, perhaps to several hundred microfarads. This, in turn, will increase the initialization time unless the initialization current is also increased.

IC SUPPLY VOLTAGE PROTECTION

High supply-voltage protection

High supply-voltage protection safeguards the IC against damage by overvoltage from the take-over winding of the SMPS transformer from which the supply is obtained. This trip, internally set at 22.9 V, causes the circuit to stop and then attempt to start up repeatedly using the slow-start procedure which is explained later.

Low supply-voltage protection

The low supply-voltage protection circuit is programmed at pin 4 (V_{smin}). If this pin is left open-circuit then a default value of 10.5 V is taken. Above an internally set minimum of 8.4 V, the protection level can be set with a resistor at pin 4. Operation below 8.4 V is impracticable because the base-drive to the SMPS power switching transistor cannot be adequately defined. The relationship between the low supply protection voltage level (V_{smin}) and the resistor value is:

$$R4 = 0.6 \times V_{smin} \times R6$$

where R4 is the value of the resistor connected to pin 4, V_{smin} is the minimum supply voltage required, and R6 is the value of the resistor connected to pin 6 (reference current). Figure 2 shows V_{smin} versus the voltage at pin 4.

The ratio of the user-defined low voltage trip value to the normal operating voltage must be chosen to minimize variation of base-current drive to the SMPS power switching transistor. The maximum value for the low supply protection should not be set higher than the initialization level of 17 V, or the circuit will not start.

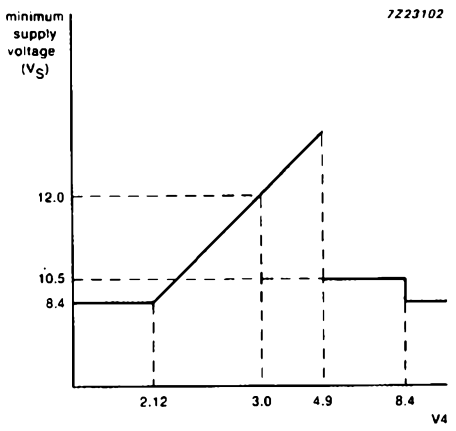


Fig.2 Minimum supply voltage as a function of the voltage on pin 4

PROGRAMMABLE REFERENCE CURRENT

The IC has a 'master' reference current which governs six other 'reflected' reference currents used in the IC.

A reference voltage V_{ref} which is nominally 2.5 V, is available at the I_{ref} pin, pin 6. The 'master' reference current is defined within the range 200 µA to 800 µA by the value of the resistor connected between this pin and ground.

$$I_{ref} = V_{ref}/R6$$

The recommended value of 'master' reference current for most applications is 500 µA, which is achieved with a 5.1 kΩ resistor connected to pin 6.

The six 'reflected' reference currents in the IC, each of which has a value equal to one sixth of the master reference current (I_{ref}) at pin 6, are internally applied to other pins of the IC as follows:

(a) oscillator capacitor charge current (pin 10)

(b) maximum duty factor setting (pin 12)

(c) low supply-voltage protection level (pin 4)

(d) power switching transistor overcurrent protection (pin 13)

(e) duty factor pin (pin 9)

(f) one other current is mirrored again (1:7) and discharges the oscillator capacitor during flyback, so the charge/discharge current ratio is 1:6.

OSCILLATOR

The oscillator produces a sawtooth waveform with a positive-going ramp and a negative-going flyback. The sawtooth waveform is sliced by the controlled slicing level (CSL) circuit in the pulse-width modulator to produce the correct output pulse. The fixed operating frequency of the oscillator, which can be selected between 10 and 100 kHz, is set at pin 10 and the circuit can be synchronized at pin 11.

Operating frequency adjustment

The oscillator capacitor is charged and discharged repeatedly between two reference levels defined by the bandgap reference. These are V_{high} = 5 V, and V_{low} = 1.4 V. The charge current is one sixth of I_{ref} whereas the discharge current equals I_{ref}. The period is given by:

$$T_{osc} = 10 \times R6 \times C10$$

where R6 is the value of resistor (normally 5.1 kΩ) at the reference pin (pin 6), and C10 is the value of the oscillator capacitor on pin 10.

The oscillator flyback sets the bistable in the output logic and inhibits output until the start of the next oscillator ramp.

Synchronization

The oscillator can be synchronized to negative-going pulses with an amplitude of 0.85 V to 5.6 V and a duration of more than 0.5 µs at synchronization pin 11. The start of the next oscillator ramp is inhibited as long as the sync pulse amplitude remains above the threshold of 0.85 V. If pin 11 is tied to the supply pin (pin 5), the oscillator will be free-running. Pin 11 must not be connected directly to ground because of the presence of the clamp circuit shown in Fig.6.

It is possible to operate the oscillator in a 'single pulse' mode in which it's synchronized with a pulse train at pin 11 at less than the oscillator free-running frequency. For this mode of operation, the time during which the synchronizing pulse remains below 0.85 V must be shorter than the oscillator free-running period as shown in Fig.3. The negative-going edges of the synchronizing pulses each trigger a single oscillator sawtooth ramp.

It's also possible to operate the oscillator in a 'burst' mode in which it's synchronized with a pulse train at pin 11 at less than half the oscillator free-running frequency. For this mode of operation, the time during which the synchronizing pulse remains below 0.85 V must be longer than one or more oscillator free-running periods as shown in Fig.4. The negative-going edges of the synchronizing pulses each trigger a burst of two or more oscillator sawtooth waveforms at the free-running frequency followed by a rest period which lasts until the next negative-going sync pulse edge occurs.

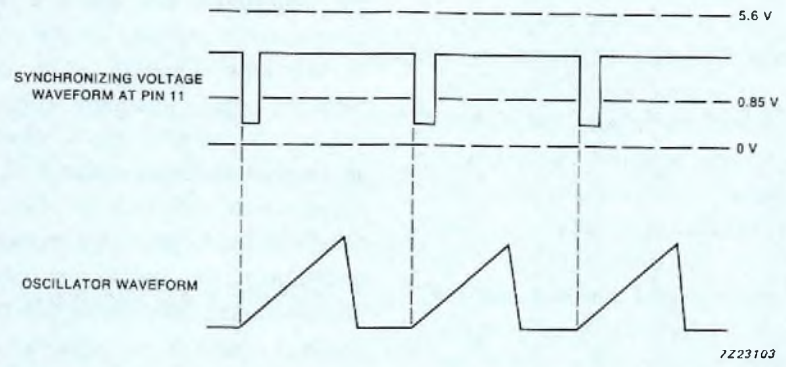


Fig.3 Typical waveform of synchronized SMPS

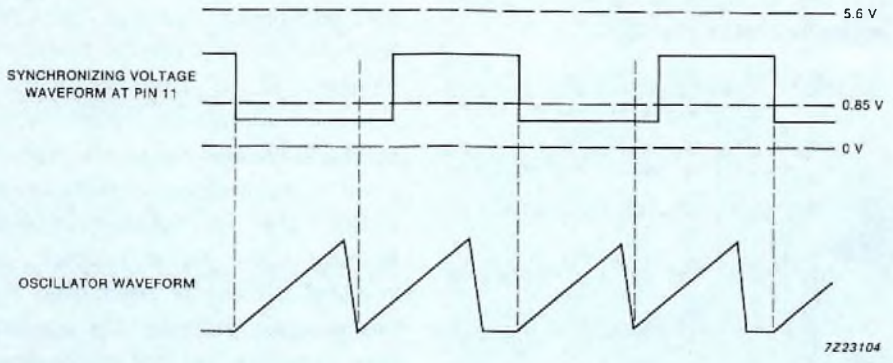


Fig.4 Typical waveform of an SMPS locked to a submultiple of the oscillator frequency

It's also possible to synchronize the oscillator to a pulse train at pin 11 similar to that shown in Fig.3 but which has a higher frequency than the free-running frequency of the oscillator. In this mode, the oscillator sawtooth is triggered by the negative-going edge of a sync pulse and all subsequent sync pulses are ignored until the oscillator sawtooth is completed. The oscillator is then inhibited until the next negative-going sync pulse edge occurs to trigger the next oscillator sawtooth.

Since an important advantage of an SMPS is the mains-isolation it provides, sync pulses for the TDA8380 must be derived via an opto-coupler or a loosely coupled pulse transformer.

Sync pulse coupling via an opto-coupler

In Fig.5, a negative going sync pulse is derived from a source such as the horizontal deflection stage of a TV set. Resistor R1 limits the current through the opto-coupler diode and R2 limits the current drawn from pin 11 of the TDA8380. This arrangement can be used with any of the previously described synchronization methods.

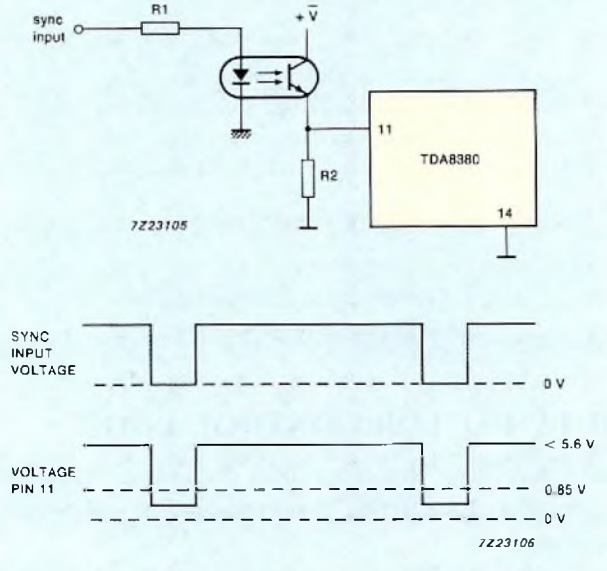


Fig.5 Example of synchronization of the TDA8380 using an opto-coupler

Sync pulse coupling via a pulse transformer

The pulse transformer in Fig.6 is a loosely coupled type such as the CI10d2. Resistor R1 limits the current in the primary winding of the transformer and R2 loads the secondary winding. The pulse transformer differentiates the sync pulse input to create negative and positive-going spikes in synchronism with the negative and positive-going transitions of the sync input. C1 AC couples the sync pulses to pin 11 of the TDA8380. The AC coupling shifts the entire signal positive and the internal circuitry of the IC clamps the negative-going excursions to 0.85 V. The positive-going spikes are removed by a transistor in the TDA8380 and the remaining negative-going spikes are used to synchronize the oscillator. Because of the limited duration of the negative-going spikes, this arrangement cannot be used for the synchronizing method shown in Fig.4.

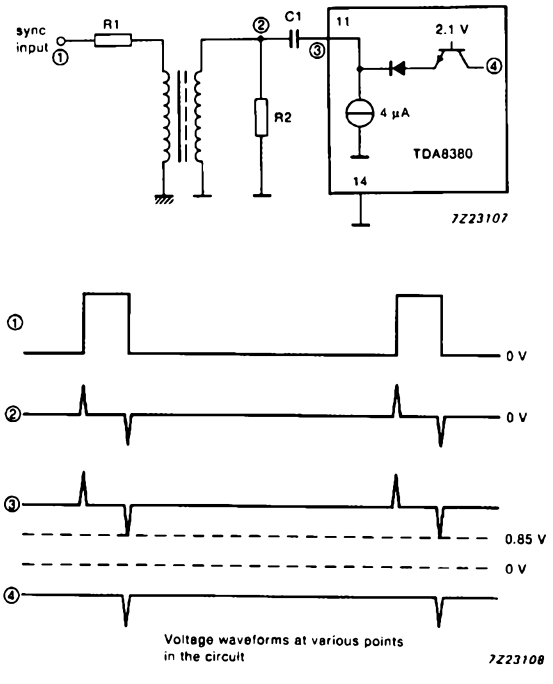


Fig.6 Example of synchronization of the TDA8380 using a pulse transformer

DUTY FACTOR CONTROL LOOP

The control loop elements consist of the error amplifier, the transfer characteristic generator, and the pulse-width modulator.

Error amplifier and transfer characteristic generator

The error amplifier at pins 7 and 8, and the transfer characteristic generator control the duty factor at all times. The output of the error amplifier is connected to the stabilization pin, pin 8 so that external frequency compensation and gain control can be applied.

The error amplifier is an inverting amplifier with high DC gain, internally compensated to give good stability. It compares the feedback voltage at pin 7 with an internal reference voltage (2.5 V) to give an error signal which modulates the duty factor. For applications using feedback from the primary side of the SMPS transformer, the stabilization pin (pin 8) is connected directly to the duty factor pin (pin 9) and a series RC feedback network is connected between the feedback pin (pin 7) and stabilization pin (pin 8) to adapt to the dynamics of the SMPS.

The transfer characteristic generator input is also internally connected to pin 7. Its function is to reverse the relationship between the duty factor and the feedback voltage when the latter is too low for the error amplifier to be active (<2.5 V). This reverse characteristic (decreasing duty factor with decreasing feedback voltage) is used to provide protection in the event of an overload or short-circuit at the output of the SMPS. This is explained in more detail under the heading 'Duty factor foldback during SMPS output overload'. It can be seen from Fig.7 that the transfer characteristic generator has no further effect once the duty factor has reached its maximum value. Thereafter, the duty factor is constant with increasing feedback voltage until the error amplifier enters its linear control range and produces the steep ramp of the characteristic where duty factor increases with decreasing feedback voltage. The maximum duty factor can be set to a lower limit if a resistor is connected at the 'slow-start pin' (pin 12). In this case, the feedback voltage range over which the duty factor dwells at maximum is increased.

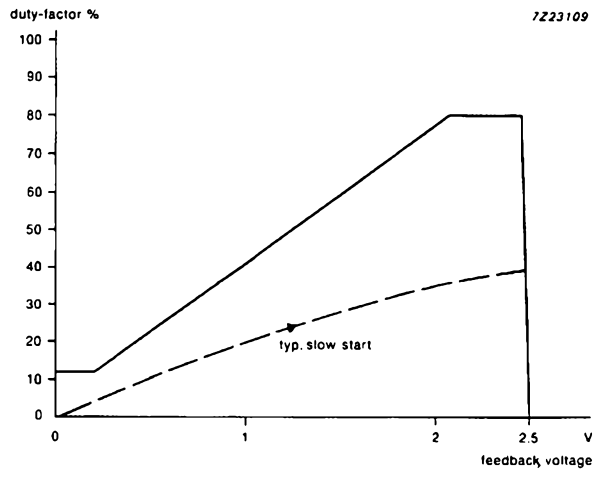


Fig.7 Duty factor transfer characteristic

For low feedback voltages on the feedback pin, the duty factor remains at the internally-set value of 12% of nominal, enabling the power supply to start.

The lowest of the three inputs to the controlled slicing level (CSL) circuitry from the error amplifier, the transfer characteristic generator (TCG), and the slow-start pin (pin 12) dictates the slicing level which is fed to the pulse-width modulator. The slicing level is compared with the oscillator waveform to produce the rectangular output pulse which begins at the start of the oscillator sawtooth and ends where the oscillator sawtooth ramp intersects the controlled slicing level as shown in Fig.8.

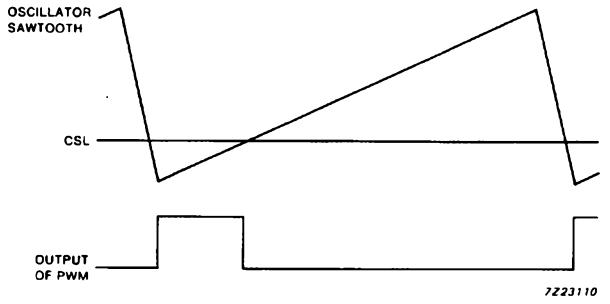


Fig.8 Waveforms associated with pulse-width modulation

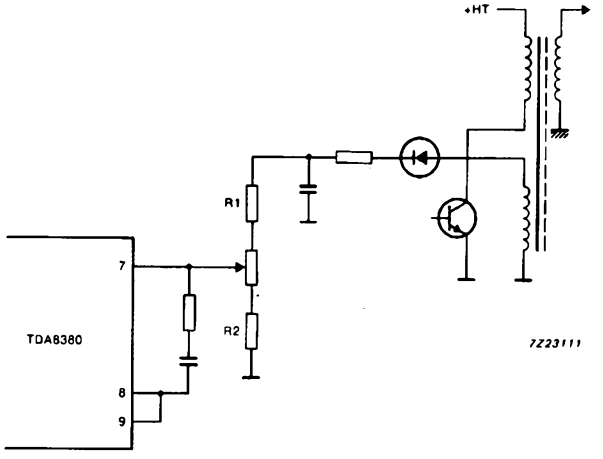


Fig.9 Typical arrangement of feedback from the primary winding of the SMPS transformer

Non-isolated feedback

The feedback signal for the TDA8380 can be derived from an auxiliary primary (hot) winding (e.g. the take-over winding) of the SMPS transformer. As shown in Fig.9, the voltage from this winding is rectified and smoothed so that it follows deviations of the SMPS output voltage. A resistive potential divider sets the nominal feedback level at 2.5 V before it's applied to the feedback signal input at pin 7 of the TDA8380.

Isolated feedback via an opto-coupler

Direct access to the pulse-width modulator input via the duty factor pin (pin 9) allows optional use of an external error amplifier. The error signal can be derived from the secondary winding of the SMPS transformer via the external error amplifier, and fed to pin 9 via an opto-coupler. The error amplifier is connected to the secondary side of the SMPS transformer to reduce the influence of the opto-coupler characteristics.

As shown in the example in Fig.10, the collector of the opto-coupler transistor is connected to pin 9 of the TDA8380 from where it receives a reference current ($I_{ref}/6$). The opto-coupler modulates this current with the error signal from the external error amplifier. The external error amplifier consists of two PNP transistors connected to form a high gain comparator. The stabilized reference voltage for the comparator is derived from a series-connected resistor and zener diode at the SMPS output.. The voltage to be compared with the reference voltage is a sample of the voltage from the secondary winding of the SMPS transformer derived from a potential divider. To ensure that the transfer characteristic generator (TCG) in the TDA8380 remains operational when using an external error amplifier, it's advisable to apply a 'pseudo' feedback voltage from the take-over winding of the SMPS transformer to the internal error amplifier at pin 7 of the TDA8380. It should be noted that, in this application, the output of the internal error amplifier at pin 8 of the TDA8380 isn't connected.

If the opto-coupler transistor were to fail open-circuit, the output from the SMPS would increase above a desirable level unless some precautions were taken. To prevent this, the TDA8380 incorporates a protection comparator with one input connected to pin 7 and the other connected to an internal reference voltage of 3.2 V which is 25% above the error amplifier reference voltage (2.5 V). During normal SMPS operation, the voltage set at pin 7 by R1 and R2 (Fig.10) should be close to the 125% overvoltage trip level. If the SMPS output voltage increases excessively, the TDA8380 will repeatedly go through the slow-start procedure.

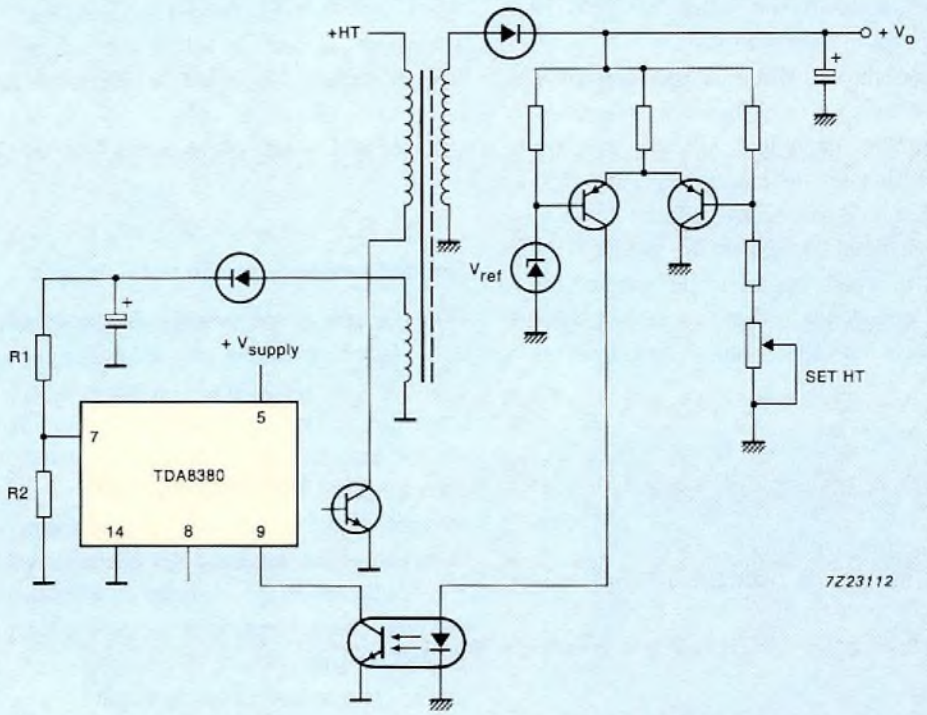


Fig.10 Example of feedback via an opto-coupler

Fail-safe control loop protection

The error amplifier circuit has been designed so that, if a fault develops in the feedback loop, the duty factor is reduced to its minimum value of 12%. Such a fault might be the external circuit connected to the feedback pin (pin 7) becoming either short-circuited or open-circuited. Either of these faults could occur during start-up or normal operation. During such faults, the duty factor cannot be greater than the internally-set minimum because the voltage of the feedback pin takes a value equal to, or close to 0 V.

If, during normal operation, the value of feedback attenuator resistor R1 in Fig.9 decreases or the value of R2 increases, the feedback at pin 7 will increase and the duty factor dictated by the error amplifier will be reduced. This is a safe condition but it will eventually reduce the supply voltage from the take-over winding on the SMPS transformer to below the low supply-voltage.

If the value of feedback attenuator resistor R1 increases or the value of R2 decreases, the duty factor will be increased by the error amplifier and the DC output(s) from the SMPS will increase. However, under this fault condition, one of the following four built-in safety features will limit the SMPS output level(s):

- demagnetization sensing at pin 3
- peak current limiting at pin 13
- maximum duty factor setting at pin 12 followed by duty factor foldback
- supply overvoltage protection at pin 5.

Which of these limiting actions occurs first depends on the overall design of the SMPS.

Duty factor foldback during SMPS output overload

The overload current foldback automatically reduces the duty factor in the event of an overload or a short-circuit at the output of the SMPS.

Initially, as the SMPS outputs overload, the duty factor increases to its set maximum value. If the overload continues to increase, the SMPS output voltage, and hence the error feedback voltage, begins to fall and the duty factor traverses right to left along the characteristic shown in Fig.7 until it eventually remains at the minimum value of 12%. The output voltage diminishes rapidly as soon as the feedback voltage at pin 7 falls below 2 V because the falling feedback level then results in a progressively lower duty factor (positive feedback).

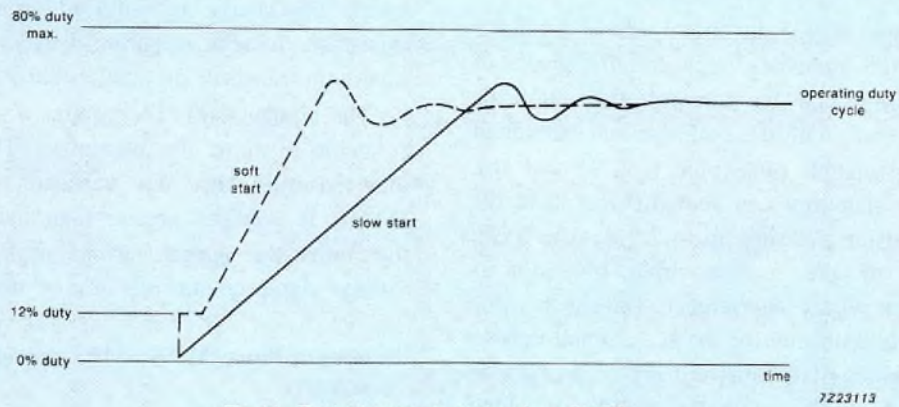


Fig.11 Typical start-up cycle of an SMPS

Slow-start or soft-start

After initialization of the TDA8380, the duty factor of the SMPS power switching transistor can be made to start from zero and its rate of increase is controlled until the SMPS output voltage reaches a stable level. This slow-start is achieved by connecting a capacitor between the slow-start pin (pin 12) and ground. At start-up, the capacitor quickly charges and the voltage on pin 12 rises rapidly to demand the 0% duty factor as shown in Fig.11. It then rises at a much slower rate determined by the value of the capacitor and slowly increases the duty factor. This slow-start reduces or minimizes the stresses on the SMPS power components and therefore results in more reliable operation.

A soft-start is obtained if pin 12 doesn't have a capacitor connected to it. As shown in Fig.11, the duty factor then rises rapidly to 12% and then steadily increases under control of one or more of the following:

- transfer characteristic generator (TCG)
- demagnetization sensing
- cycle by cycle current limiting

This control continues until the feedback increases to a level where the error amplifier starts to operate in the linear region of its transfer characteristic and takes over control of the duty factor.

Programmable maximum duty factor

The maximum duty factor can be programmed to any value below the maximum of 80% as shown in Fig.12 by selecting the value of an external resistor to define the voltage on the slow-start pin (pin 12). The voltage on pin 12 is given by:

$$V_{12} = (V_{ref} \times R12)/(6 \times R6)$$

where V_{ref} = 2.5 V nominal

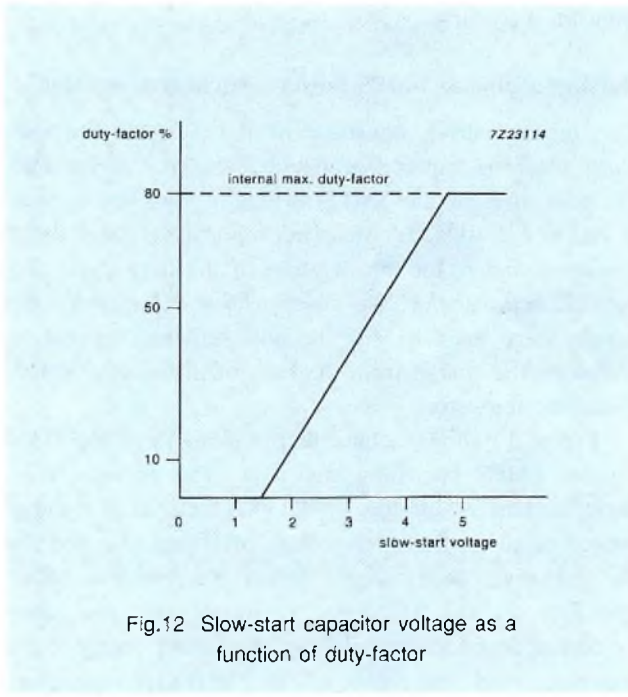


Fig.12 Slow-start capacitor voltage as a function of duty-factor

ANTI DOUBLE-PULSE LOGIC

Anti double-pulse logic interposed between the pulse-width modulator and the output stage ensures that only one output pulse can occur in each oscillator period.

This logic circuitry is necessary because the intersection points of the controlled slicing level and the oscillator sawtooth waveform shown in Fig.8 might be indeterminate due to noise on either or both of the signals. This would mean that the SMPS power switching transistor base drive pulse from the IC could also become indeterminate and appear as double or multiple pulses. The anti double-pulse logic circuitry ensures a single drive pulse with clean edges. This results in safer operation of the SMPS power switching transistor and improved reliability.

DIRECT DRIVE OUTPUT STAGE

The TDA8380 output stage can directly drive a bipolar or PowerMOS SMPS switching transistor. It consists of two NPN transistors, one for forward drive and the other for reverse drive, with the collector and emitter of each connected to separate pins (pins 1, 2, 15 and 16). The forward drive transistor can source 0.75 A and the reverse drive transistor can sink up to 2.5 A. The dV/dt of the collector of the reverse drive transistor is internally limited to reduce interference. During the time leading up to the initialization of the IC, a small current flows from the emitter of the forward drive transistor to ensure that, when using a bipolar SMPS switching transistor, the base coupling capacitor is primed (pre-charged) so that the transistor is correctly turned off from the very first cycle.

Driving a bipolar SMPS power switching transistor

The forward drive transistor of the TDA8380 output stage must be capable of feeding enough current into the base of a bipolar SMPS switching transistor to turn it on. For a BUT11A transistor the typical base drive current is 0.5 A for the duration of the duty cycle. To turn the transistor off, the reverse drive transistor of the output stage must be able to sink sufficient current to withdraw the charge from the base of the bipolar SMPS switching transistor.

Figure 13 shows a base drive circuit for a BUT11A bipolar SMPS switching transistor. The forward base drive current is limited by R1. C1 acts as a voltage source equal to the zener voltage of D1 and is used for the negative base drive. When the reverse drive transistor in the TDA8380 is turned on, the zener voltage appears across inductor L1 causing charge to be removed from the base of the BUT11A transistor, thereby turning it off. Inductor L1 limits the rate at which the charge is removed from the base of the transistor, thereby ensuring correct storage time and minimum transistor dissipation during turn-off.

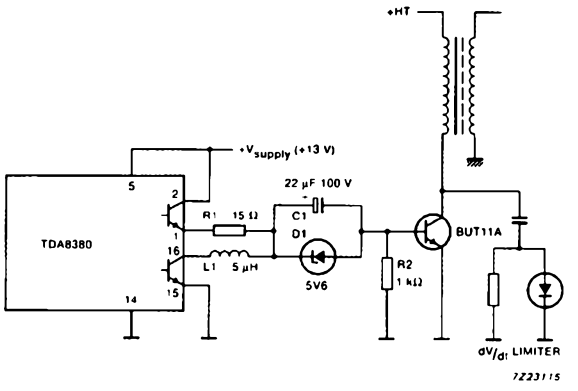


Fig.13 Typical drive circuit for the bipolar BUT11A

The bipolar BUT11A requires a snubber circuit at its collector to limit the maximum dV/dt to 1000 V/µs, thus ensuring that the transistor remains within its SOAR. If voltages greater than the maximum V_{CE} of the transistor appear across its collector/emitter, a voltage clamp circuit may also be needed.

Driving a PowerMOS SMPS power switching transistor

Because of their fast switching capability and low drive power requirements, PowerMOS switching transistors are being increasingly used in switched-mode power supplies. To switch a PowerMOS transistor on, a voltage which is more positive than the source potential must be applied to the gate. To turn the transistor off, the gate must be returned to the same potential as the source.

Figure 14 shows a typical drive circuit for a BUZ80 (BUK456-800B) PowerMOS transistor in an SMPS. When the forward drive transistor in the TDA8380 switches on, a 10 V step occurs at the junction of R1 and R3 and charges the input capacitance (1.6 nF typical) of the PowerMOS transistor with a current spike limited to 300 mA by R1. As long as the gate voltage is maintained, drain current continues to flow through the transformer winding. When the reverse drive transistor in the TDA8380 conducts, the PowerMOS transistor turns off because its input capacitance is discharged via R2 which limits the negative current spike to 300 mA. The resistance between the emitter of the forward drive transistor in the TDA8380 and the collector of the reverse drive transistor limits the current flow to ground during the brief period when both transistors are conducting. During the time leading up to initialization of the IC, the small current from the emitter of the forward drive transistor is conducted to ground via R3 to prevent the PowerMOS transistor turning on prematurely.

When using a PowerMOS transistor for SMPS switching, care should be taken not to exceed its drain-source voltage. In Fig.14, a dynamic voltage clamp limits the large voltage swings at the drain of the BUZ80. In some cases, it may be necessary to incorporate a snubber circuit to keep the switching transistor within its SOAR. Since the maximum gate-source voltage of the BUZ80 is 20 V, it will be necessary to connect an 18 V zener diode clamp to its gate if the TDA8380 supply voltage exceeds 20 V.

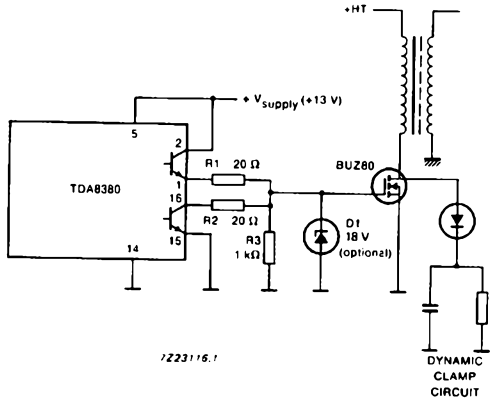


Fig.14 Typical drive circuit for the PowerMOS BUZ80

POWER SWITCHING TRANSISTOR OVERCURRENT PROTECTION

The TDA8380 incorporates two types of overcurrent protection. They will be described in relation to the circuit in Fig.15 and the waveforms in Fig.16.

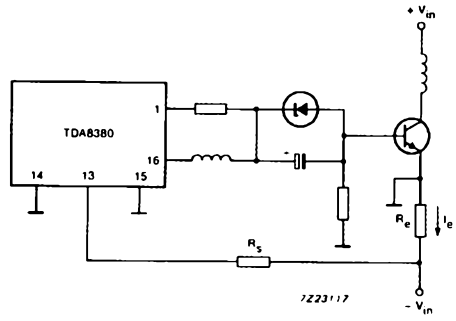


Fig.15 Monitoring the current through the SMPS power switching transistor

The sawtooth voltage pulses applied to the overcurrent protection pin (pin 13) are developed across a resistor connected to the grounded emitter of the SMPS power switching transistor as shown in Fig.15. Since the ground pin of the TDA8380 is connected to the emitter of the SMPS power switching transistor, the sawtooth voltage pulses across resistor R_e are negative-going with respect to ground. They're applied to the IC via a second resistor (R_s) with a much higher value and shifted positive with respect to ground by passing a reference current from pin 13 through resistor R_S. In the TDA8380, the sawtooth pulses are compared with two reference voltage levels to provide two protection thresholds. It should be noted that, if the current protection pin (pin 13) is grounded, or at a voltage above 5.6 V, the IC will not start.

First level cycle-by-cycle overcurrent protection

If, during any part of any cycle, the peak level of the negative-going sawtooth pulses at pin 13 reaches the first protection threshold of +200 mV, the IC turns the SMPS power switching transistor off for the remainder of that cycle. This may be repeated cycle-by-cycle, and the SMPS will continue to operate in this condition without reverting to a restart.

Second level trip overcurrent protection

If a fault causes the current through the SMPS power switching transistor to rapidly increase to an excessive level, the peak level of the negative-going sawtooth pulses at pin 13 will reach the second protection threshold of 0 V. This causes the IC to turn the SMPS power switching transistor off and the SMPS then attempts to restart via the slow-start procedure. This provides emergency protection against a typical current rise rate of at least 6 or 7 A/μs which can occur, for example, if the SMPS output is short-circuited while the SMPS power switching transistor is conducting.

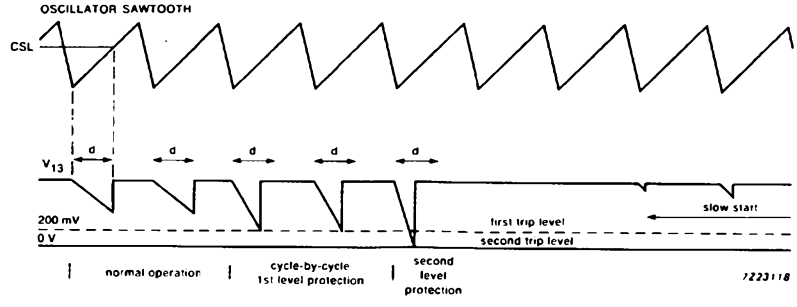


Fig.16 Voltage waveforms at the current protection pin (pin 13)

IC protection against power transistor short-circuit.

To ensure that the TDA8380 is protected in the event of a collector/emitter short-circuit in the SMPS power switching transistor it's very important that the current sensing circuitry in Fig.15 is correctly arranged.

If the emitter of the SMPS power switching transistor were to be grounded through R_e and the right-hand side of R_s connected directly to its emitter, a dangerous situation would occur in the event of collector/emitter short-circuit in the SMPS power switching transistor. Resistor R_e would burn-out but the full rectified mains input would appear at the drive output of the IC and the IC would be destroyed.

The arrangement shown in Fig.15 in which the ground pin of the TDA8380 and the emitter of the SMPS power switching transistor are connected to the same point provides full protection for the IC. In the event of a collector/emitter short-circuit in the SMPS power transistor, the rectified mains voltage doesn't appear on the drive output of the IC. However, the high current burns-out R_e and, since most of the rectified mains voltage appears across R_s, this resistor also burns-out. The IC incorporates a protection diode at pin 13 to prevent damage to the internal circuitry. Resistors R_e and R_s must be non-flammable types (NFR resistors) which fail open-circuit when they pass excessive current.

Overcurrent protection component values

Figure 17 shows a typical voltage-time characteristic for pin 13 under overload and fault conditions but, of course, other current protection levels can be used. The following values are required for determining the resistor values to achieve the required protection characteristic:

I_e = emitter current of the SMPS power switching transistor

V_i = DC voltage input to the SMPS

L_p = inductance of the primary winding of the SMPS transformer

t_d = delay of the IC

t_s = storage time of the SMPS power switching transistor.

The overshoot of the value of I_e beyond the first trip level is then given by:

$$(t_d + t_s) \times dI_e / dt$$

and, since $dI_e / dt = V_i / L_p$, this can be re-written as:

$$(t_d + t_s) \times V_i / L_p.$$

Since the overshoot shouldn't reach the second trip level an I_e overshoot of 0.9 A will be assumed so that:

$$(t_d + t_s) \times V_i / L_p = 0.9 \text{ A}$$

the intercept at 200 mV must therefore be made to correspond with an emitter current greater than 0.9 A. If, for this example, this current is chosen as 1 A, then:

$$R_e = 200 \text{ mV} / 1 \text{ A} = 200 \text{ m}\Omega.$$

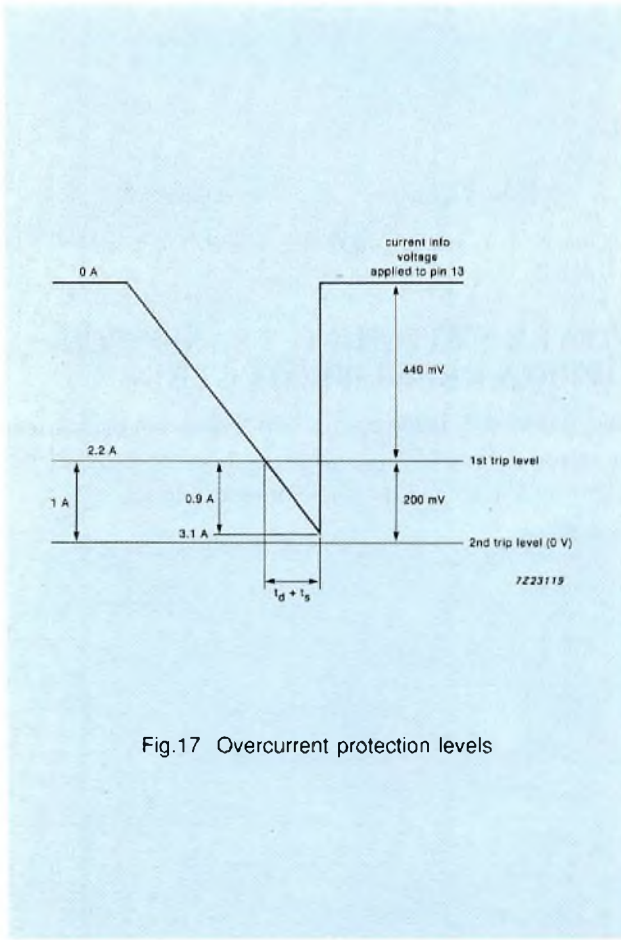


Fig.17 Overcurrent protection levels

The termination of I_e is required to be 3.1 A in this example. The trip current level (I_{trip}) is therefore derived from:

$$I_{trip} = 3.1 \text{ A} - 0.9 \text{ A} = 2.2 \text{ A}$$

The total offset voltage (V_{offset}) is therefore derived from:

$$V_{offset} = (2.2 \text{ A} + 1 \text{ A}) \times 200 \text{ m}\Omega = 640 \text{ mV}.$$

The value of R_s can then be determined from:

$$R_s = (V_{offset} \times 6 \times R6) / V_{ref}$$

where V_{ref} is the reference voltage at pin 6 (2.5 V nominal) and R6 is the value of the resistor connected between pin 6 and ground (usually 5100 Ω). R_s would therefore have a value of 7800 Ω.

SMPS TRANSFORMER CORE DEMAGNETIZATION SENSING

The demagnetization input (pin 3) of the TDA8380 is for sensing the magnetization state of the core of the SMPS transformer. If this pin is connected to a flyback winding of the SMPS transformer (normally the IC supply take-over winding), the drive to the SMPS power switching transistor will be inhibited throughout flyback as long as the transformer is delivering current to the SMPS output rectifiers.

Selecting continuous current mode

If the demagnetizing sensing pin (pin 3) is left unconnected, the circuit will not start. If pin 3 is connected to ground, the demagnetization sensing is disabled, allowing the IC to drive SMPS systems which are designed to operate in the continuous current mode.

Discontinuous current mode demagnetization sensing

For SMPS systems which are designed to operate in the discontinuous current mode, it's essential that the core of the SMPS transformer is demagnetized before the start of the next drive pulse. This is ensured by simply connecting a current limiting resistor between pin 3 of the IC and an SMPS transformer winding which delivers a positive flyback voltage. This winding is usually the same one that delivers the IC supply voltage. In some cases an additional low value capacitor is required for filtering out noise or ringing.

An example of this use of the demagnetization sensing pin (pin 3) is shown in the evaluation board circuit shown in Fig.19, where the IC monitors the AC voltage waveform of a transformer winding, one end of which is at ground potential. Typical waveforms are given in Fig.18.

During the time that the voltage from the SMPS transformer winding is above 0.6 V during the oscillator ramp period, the output drive from the IC is inhibited. The implication of this is that the SMPS power switching transistor cannot be turned on while energy is stored in the transformer core. This inhibiting of the drive pulses to the SMPS power switching transistor prevents a build-up of current through the transformer which could ultimately saturate its core and result in destruction of the SMPS power switching transistor. Such conditions could arise during an output overload, in the event of a feedback loop fault, or if the potentiometer connected to pin 7 is set incorrectly.

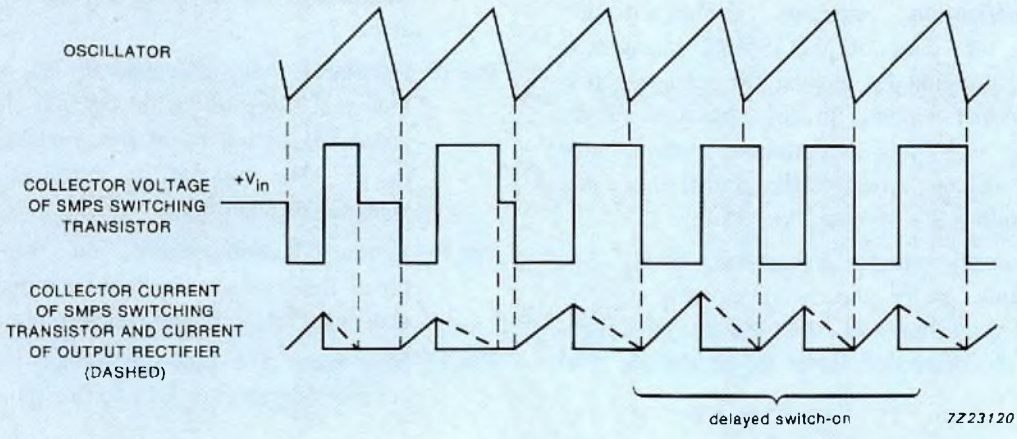


Fig.18 Demagnetizing sensing

120 W SMPS EVALUATION BOARD

The circuit of a 120 W SMPS evaluation board incorporating a TDA8380 control IC and an AT3010/110LL SMPS transformer is shown in Fig.19. The board layout is shown in Fig.20. The circuit uses a flyback converter and operates from a mains input voltage range of 180 to 265 V RMS, 50/60 Hz. It could be used as a simple supply for a TV set or a monitor.

Mains input and rectification

Diodes D1 to D4 bridge rectify the mains input voltage and the DC supply to the SMPS is smoothed by C13. R1 is connected in series with the mains input to limit the peak inrush current that occurs if the supply is switched on when C13 is fully discharged. C1/C3/L1 is a filter to prevent RFI being fed back into the mains supply. C6 to C9 suppress RFI generated by the diodes in the mains bridge rectifier

TDA8380 control IC and its peripherals

The peripheral circuitry for the TDA8380 will be explained by describing the function of each pin of the IC.

Pin 1 **Emitter of the forward drive transistor.** See information under the heading 'Direct drive output stage' for information about how to drive the bipolar BUT11A SMPS power switching transistor.

Pin 2 **Collector of the forward drive transistor.** Connected to the IC supply voltage.

Pin 3 **Demagnetization sensing.** Demagnetization protects the core of the SMPS transformer against saturation by sensing the voltage across a transformer winding. In this evaluation circuit, operation is in the discontinuous current mode and the voltage across SMPS transformer take-over winding 2/4 is sensed via R10.

Pin 4 **Low supply-voltage protection level.** See information under the heading 'low supply-voltage protection'. If this pin is left open-circuit, the protection is set to the default level of 10.5 V.

Pin 5 **IC supply.** When the mains input is ap-plied to the SMPS, the IC supply reservoir capacitor C15 is charged by a current defined by R19. When the voltage across C15 reaches 17 V, the IC initializes and diode D8 rectifies the flyback signal from winding 2/4 of the SMPS transformer to supply the IC with 13 V. R16 prevents peak rectification of spikes and C14 decouples HF noise.

Pin 6 **Master reference current setting.** Resistor R11 sets the master reference current for the TDA8380 to 500 μA as described un-der the heading 'programmable reference current'.

Pin 7 **Voltage feedback.** This is the input to the internal error amplifier. The flyback signal from winding 3/2 on the 'hot' side of the SMPS transformer is rectified and smoothed by D5/R9/C5 to give a DC level that varies in proportion to variations of the 145 V output from the SMPS. This level is reduced by potential divider R4/R5/R6 and fed to pin 7 of the TDA8380. The feedback level is set by R5.

Pin 8 **Error amplifier stabilization.** This is the error amplifier output pin that allows the connection of external frequency compens-ation network C2/R2.

Pin 9 **Duty.** This is an input to the pulse-width modulator which facilitates connection of an external error amplifier if required. Since this evaluation board doesn't use an external error amplifier, pin 9 is directly connected to the stabilization output of the internal error amplifier at pin 8.

Pin 10 **Oscillator.** 680 pF capacitor C4 connected to this pin, together with 5100 Ω resistor R11 connected to pin 6 set the oscillator frequency to 27 kHz nominal as explained under the heading 'oscillator'.

Pin 11 **Synchronization.** Since, on this evaluation board the oscillator is free running, this pin is connected to the positive supply pin of the IC.

Pin 12 **Slow-start.** The slow-start option is selected by connecting capacitor C11 to this pin.

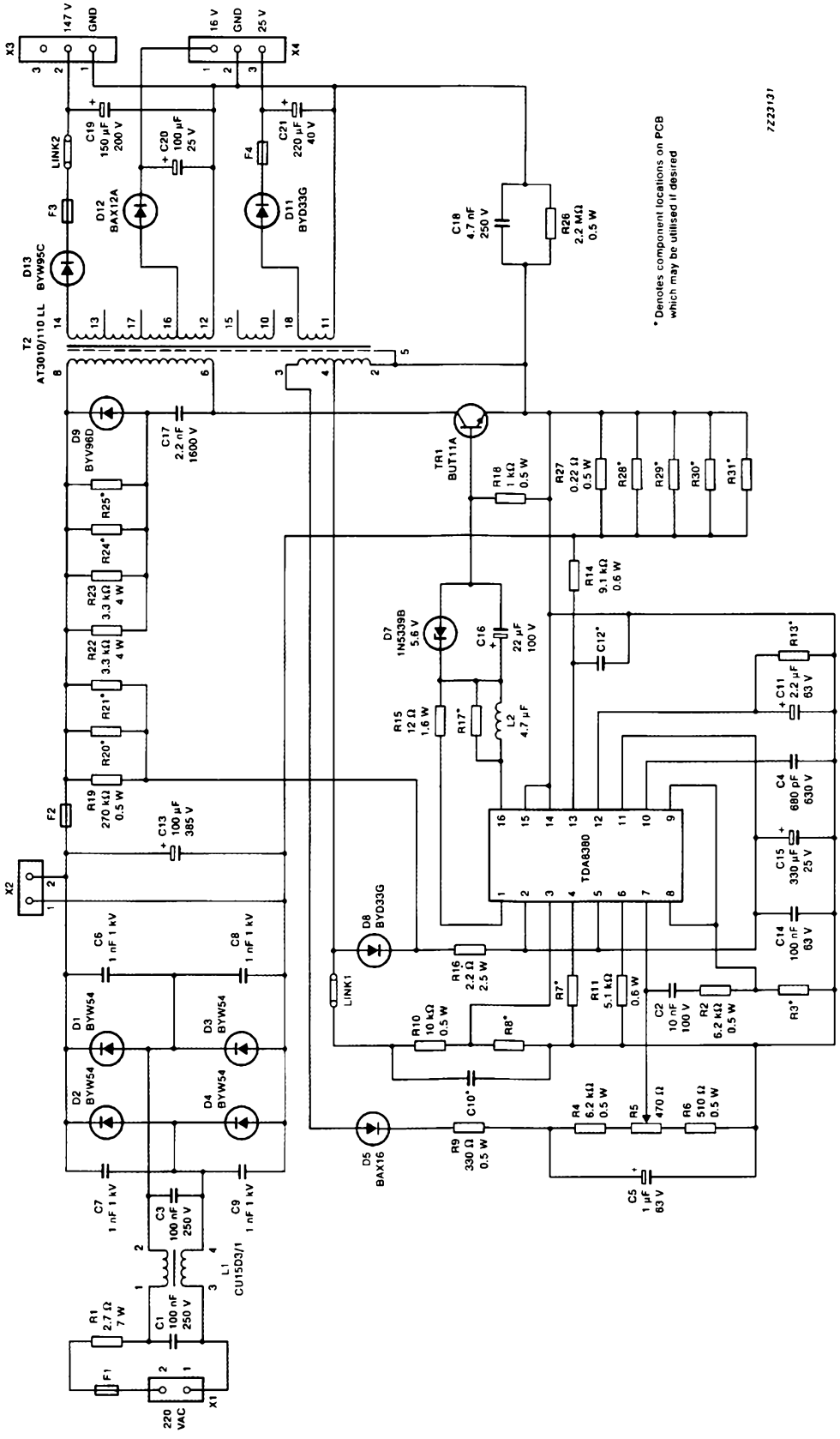


Fig.19 Circuit diagram of the TDA8380 evaluation board

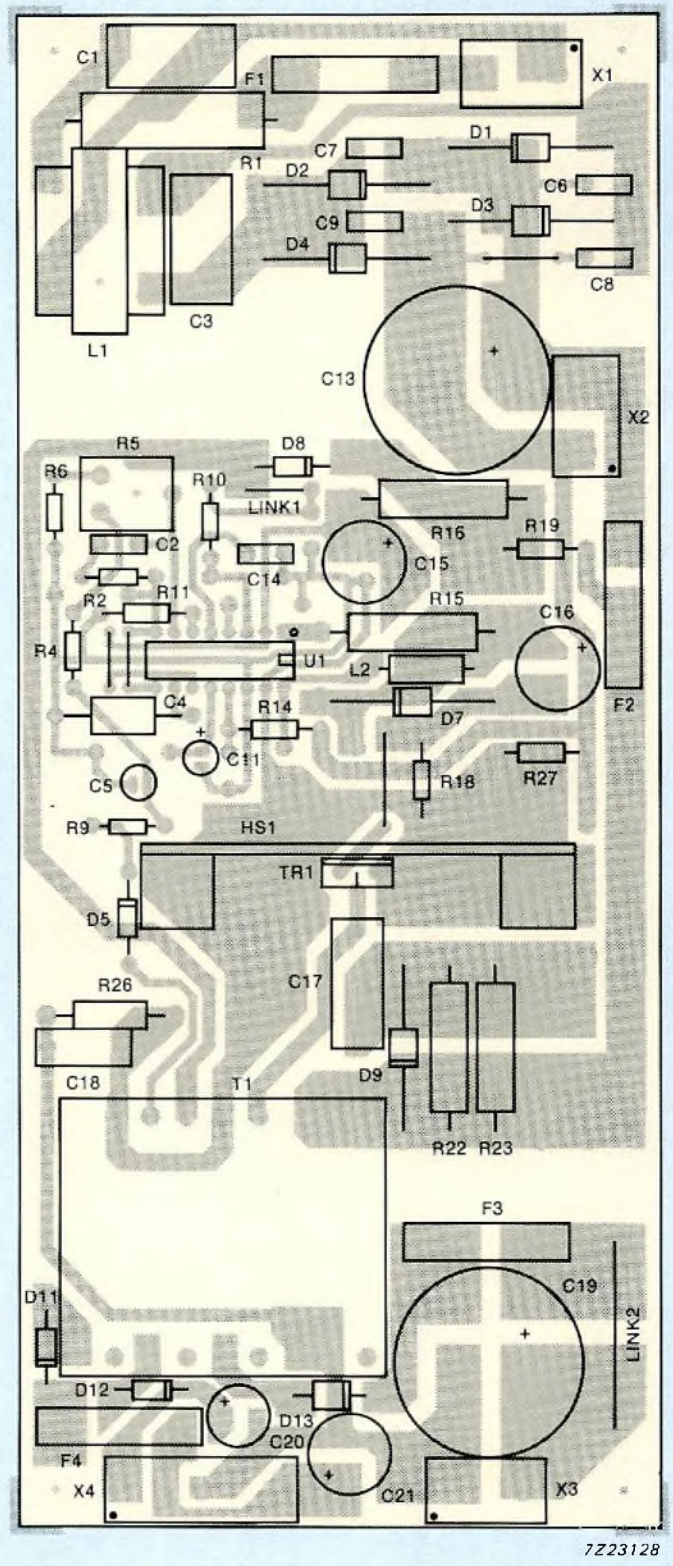


Fig.20 PCB layout for the evaluation board

Pin 13 **Overcurrent protection.** To keep the collector current of the SMPS power switching transistor within safe operating limits, the power supply incorporates overcurrent protection. R27 in the emitter circuit of the power switching transistor senses the current and provides a negative-going voltage because the emitter is grounded. The signal is converted into a positive level with respect to ground by R14 and the reference current passing through it. C12 removes noise spikes. This signal, which is proportional to the collector current of the SMPS power switching transistor is applied to pin 13 of the TDA8380 where it's internally compared with two reference voltage levels to provide the two different types of protection described under the heading 'overcurrent protection'.

Pin 14 **Ground.**

Pin 15 **Emitter of the reverse drive transistor.** Grounded.

Pin 16 **Collector of the reverse drive transistor.** See information under the heading 'Direct drive output stage' for information about how to drive the bipolar BUT11A SMPS power switching transistor.

SMPS power switching transistor protection

To protect the SMPS power switching transistor against excessive switching dissipation, a dV/dt limiting network D9/C17 is connected across the primary winding of the transformer. The two parallel connected resistors R22 and R23 have two functions:

- to discharge C17 prior to each flyback
- to damp the transformer ringing which follows each flyback. This damping must be sufficient to suppress the recurrence of positive pulses at the demagnetization input to the IC during the next oscillator cycle

SMPS outputs

The three outputs from the SMPS are rectified and smoothed by D13/C19, D12/C20 and D11/C21 to provide 145 V, 25 V and 16 V for the deflection stages, audio output and small signal stages respectively of a TV set for example. Fuse F3 in the 145 V output is only inserted for experimental purposes. Fuses should be used in the other two outputs to protect their rectifier diodes against the potentially high average currents which may flow here during overload before the protections on the primary side have had time to respond to the transformed overload current.

Performance of the evaluation board

Mains input:	180 to 265 V RMS, 50 to 60 Hz
DC outputs:	147 V, 0.68 A (102.5 W) 25 V, 0.4 A (10 W) 16 V, 0.5 A (8 W)
Switching frequency:	27.2 kHz
Line regulation	0.5%
Regulation with the two lower voltage outputs fully loaded and the main output loaded between 80 W and 102.5 W:	1.7%
Power switching transistor	
peak collector current:	2.6 A
peak collector voltage:	900 V
base current:	450 mA
duty factor:	20% to 43%

ADDITIONAL DESIGN INFORMATION

Designing for operation over the full mains input voltage range

The TDA8380 can be used in switched-mode power supplies that operate over the full AC mains input voltage range of 90 to 265 V RMS but the following points should be noted:

1. If an SMPS is operated at low mains voltages, the current drawn from the mains supply will be appreciably higher than that drawn with a high mains voltage input. The size of the mains input filter and mains reservoir capacitor will therefore have to be increased.
2. The mains rectifier diodes must be protected against the inrush current that occurs when the supply is first switched on. Such protection is particularly important if the supply is switched on when the mains reservoir capacitor is in a fully discharged state. Protection is normally provided by connecting a surge resistor in series with the bridge rectifier. However, the dissipation in such a protection resistor will be excessive if the SMPS is operated from a low mains input voltage. An alternative is to use a negative temperature coefficient (NTC) thermistor as a surge resistor. When the NTC thermistor is cold it has a high resistance and when it heats up during conduction of large current, its resistance decreases.

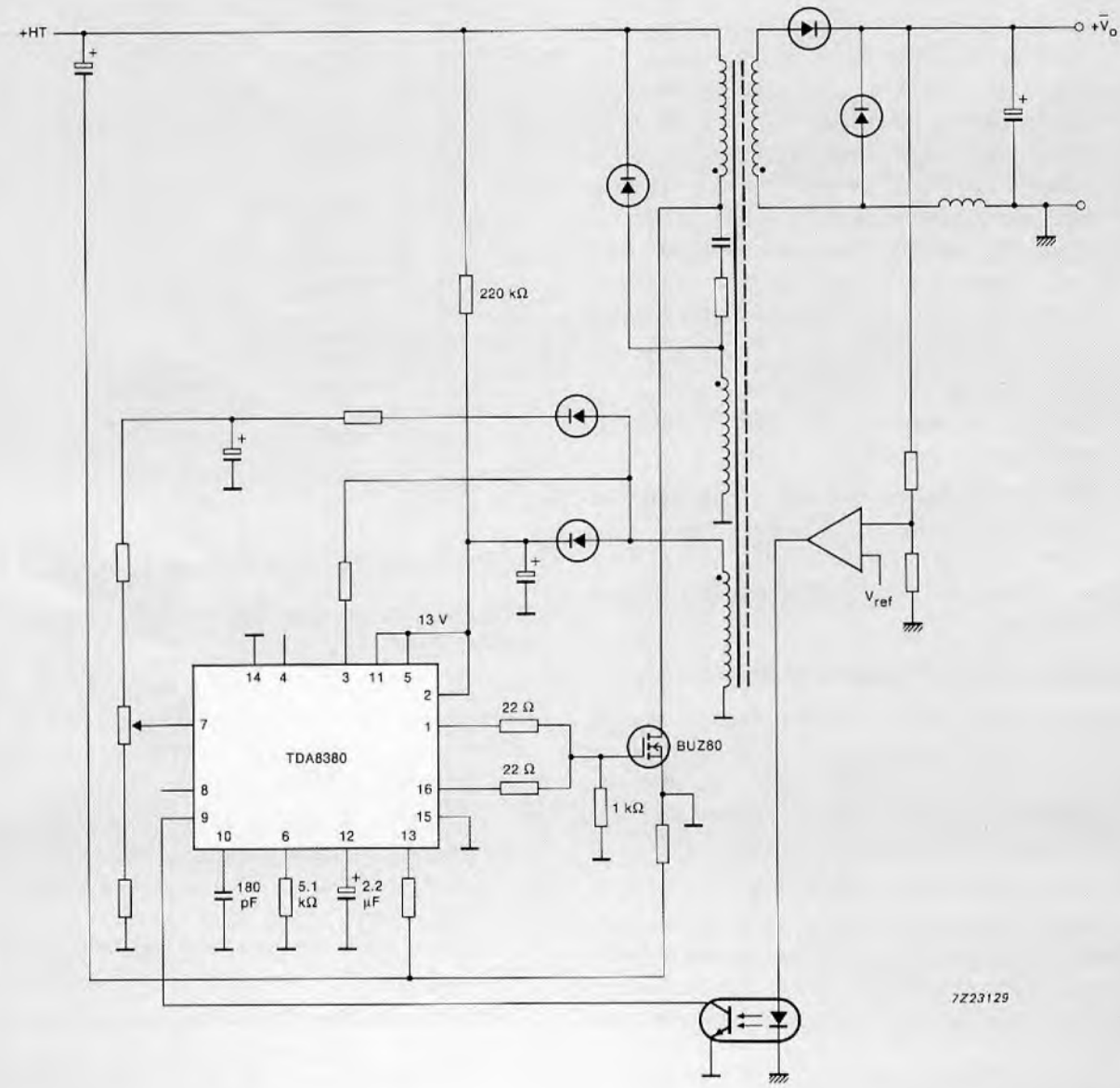


Fig.21 TDA8380 controlling a 100 kHz forward converter

There is a drawback however if the SMPS is switched off and then, after a brief interval, switched on again. Since the high power NTC thermistor has a long thermal time-constant it doesn't have sufficient time to cool down and its resistance remains low at switch on and the only protection remaining is the resistance of the mains input RFI filter. Another alternative is to increase the value of the surge limiting resistor and connect it in parallel with a thyristor which is made to conduct and short-circuit the surge resistor shortly after switch on.

3. If the unstabilized forward voltage from the SMPS transformer take-over winding is used to power the TDA8380, ensure that the low supply-voltage protection isn't activated with low mains voltage inputs, and that the high supply-voltage protection isn't activated with high mains voltage inputs.
4. Ensure that the SMPS transformer is rated to cope with power required over the full mains input voltage range. For example, the AT3010/110LL transformer can provide 120 W of output power over the mains input voltage range 180 to 265 V RMS, but can only provide 70 W over the extended mains input voltage range of 90 to 265 V RMS.

Designing for operation at high switching frequencies

The TDA8380 can operate satisfactorily at frequencies from 10 kHz to 100 kHz. However, when operating it at the higher frequencies, cross interference between the small-signal and large-signal paths must be eliminated by careful PCB design. In particular, the current protection feature is sensitive to coupling from the high current output pulses from the IC via the ground tracks.

An example of a circuit using the TDA8380 in a 100 kHz SMPS is given in Fig.21. The SMPS is based on a forward converter using opto-coupled feedback and having a low-voltage high-current output. The power switching element is a BUZ80 (BUK456-800B) Power-MOS transistor. The transformer is hand wound and incorporates a recovery winding on the primary side. If the power switching transistor fails short-circuit, a high current flows in the primary winding of the transformer. The TDA8380 is protected by grounding it to the source of the BUZ80. The resistors used in the current protection circuitry should be fusible types (NFR resistors) which are designed to fail open-circuit when they pass excessive current.

Incorporating remote on/off switching

The TDA8380 can remotely render the SMPS inactive by either disconnecting the loads from its outputs, switching it off, or reducing its output voltages.

Disconnecting the loads from the SMPS outputs

A relay can be used to disconnect the output loads from the power supply. The drawback of this method is that the power supply remains fully operational when the load is disconnected. However, if the feedback is connected to the TDA8380 via an opto-coupler, the loads can be disconnected from the SMPS without any adverse consequences because the output voltage will continue to be regulated. If direct feedback is derived from the primary side of the SMPS transformer, the SMPS output voltages will increase if the loads are disconnected. This is because the SMPS transformer isn't included in the control loop and output voltage spikes due to the leakage inductance of the transformer will be peak rectified at the outputs.

Switching off the SMPS

A switch-off signal can be passed across the mains isolation between the secondary winding of the SMPS transformer and the TDA8380 via an opto-coupler. The actual switching off can be done by suppressing the slow-start voltage at pin 12 of the TDA8380. A disadvantage of this method, however, is that since the SMPS is deactivated, a small standby power supply is necessary to power the standby control circuitry and the LED of the opto-coupler.

A circuit for switching off the SMPS by suppressing the slow-start voltage is given in Fig.22. For normal SMPS operation, the remote on/off input is held at 0 V.

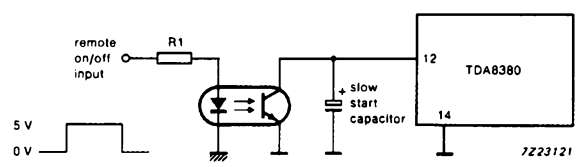


Fig.22 Remote on/off switching by suppressing the slow-start voltage

The SMPS is deactivated by holding the remote on/off input HIGH, causing the slow-start input (pin 12) of the TDA8380 to be pulled LOW, thereby forcing the duty cycle to go to zero. It should be noted that, in this condition, the IC supply voltage will cycle between 17 V (the initialization level) and 10.5 V (the low supply protection level).

Reducing the SMPS output voltages

With this method of remote SMPS on/off switching, the SMPS is set in a standby mode during which its output voltages are reduced to, say 50% of their normal level. An advantage of this method over switching off the SMPS as previously described is that the reduced voltages can still be used to power any control circuitry making a separate standby power supply unnecessary. An example of this type of remote control in a TV SMPS is given in Fig.23. A description of the error feedback via an opto-coupler is given earlier and will not therefore be repeated here. For normal SMPS operation, the remote on/off input is held at 0 V so that transistor TR1 is turned off to allow error-feedback and regulation to function normally. In the standby mode, the remote on/off input is held at +5 V to turn on transistor TR1 and increase the input to the error amplifier. The increased error amplifier output then passes via the opto-coupler to pull the 'duty' pin of the TDA8380 low enough to demand a small SMPS duty cycle that reduces its output by 50%. The 16 V SMPS output which supplies any low current control circuitry at the secondary side of the SMPS transformer is then reduced to 8 V which is still sufficient to power the 5 V regulator to maintain a supply to the control circuits. However, care should be taken to ensure that, during standby, the supply to the TDA8380 doesn't fall below the low supply voltage protection limit set at pin 4.

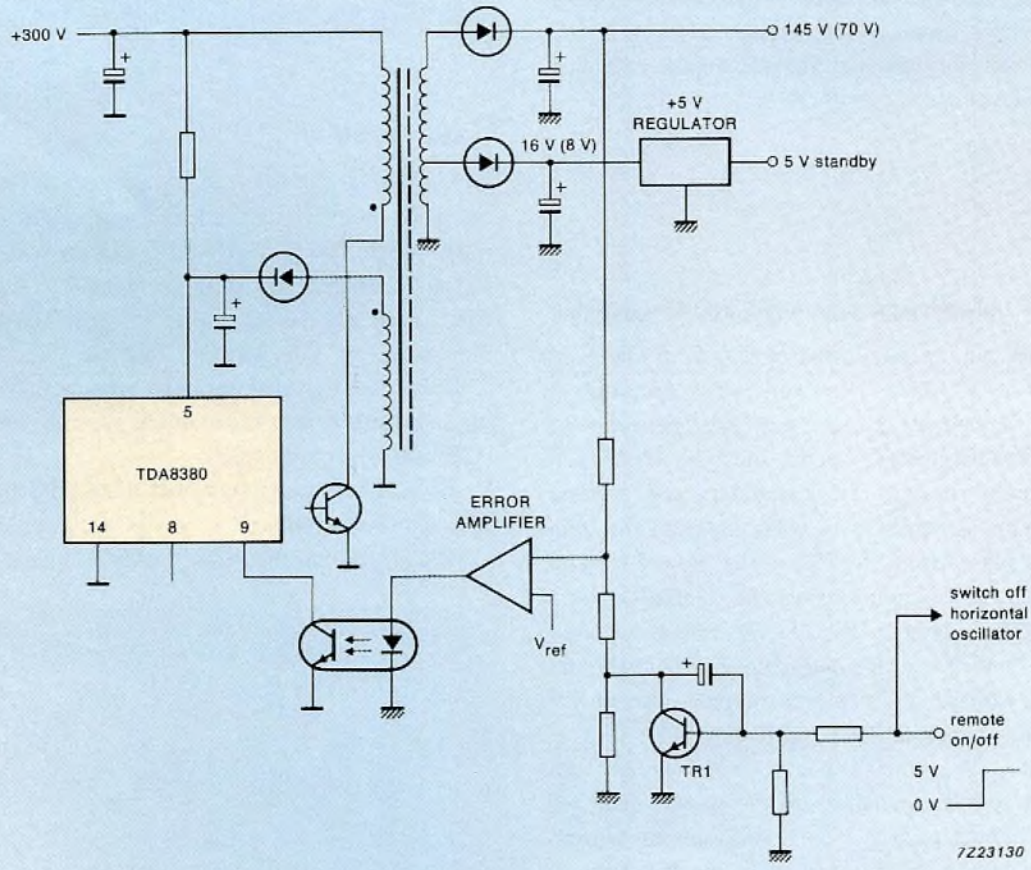


Fig.23 Remote on/off switching by reducing the SMPS output voltages via opto-coupler feedback. The values in brackets are the stand-by values

Fast initialization

When using a high value IC supply reservoir capacitor, the low starting current initialization may result in an unacceptably long delay before initialization. The delay can be reduced, at the expense of more dissipation in the supply series resistor, by increasing the charging current of the IC supply reservoir capacitor with a fast initialization circuit.

The fast initialization circuit can consist of a PTC thermistor combination, a high voltage thyristor or a transistor connected between the rectified mains input to the SMPS and the IC supply reservoir capacitor. When the SMPS is switched on, the thyristor or transistor is biased on because the IC supply voltage is low, and it supplies a charging current to the reservoir capacitor. When the voltage across the capacitor reaches 17 V, the IC initializes and starts to pulse the SMPS power switching transistor. The voltage from the SMPS transformer take-over winding then rises and stabilizes when the SMPS is fully operational. Once the take-over has been established, the thyristor or transistor must be turned off and the take-over winding then continues to provide the supply voltage for the IC.

Self synchronization mode

The demagnetization input at pin 3 of the TDA8380 simply inhibits the IC output while the oscillator continues to run. Alternatively, by deriving a sample of SMPS power switching transistor collector pulses from the SMPS transformer take-over winding and applying them to the sync input (pin 11) of the TDA8380, the oscillator can be temporarily stopped until the completion of demagnetization. This self-synchronized mode of operation is shown in Fig.24.

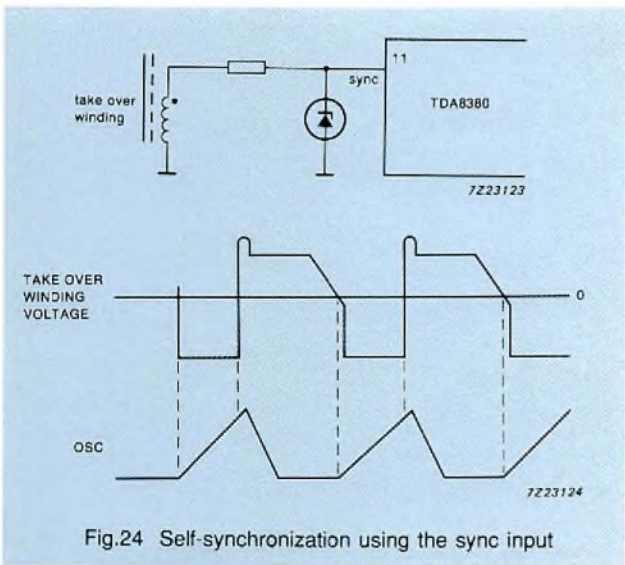


Fig.24 Self-synchronization using the sync input

Current mode operation

The direct access to the input of the pulse-width modulator at the duty pin (pin 9) of the TDA8380 can also be used to add other control signals to the error amplifier output to control the duty factor. For example, a form of current-mode control is possible by adding information about the current through the SMPS power switching transistor as shown in Fig.25. Here, the SMPS current sensing signal and the output from the error amplifier at pin 8 (or the output from an external error amplifier) are passed through summing resistors and applied to the duty pin (pin 9). The amplitude of this composite signal is compared with that of the oscillator sawtooth at the input to the pulse-width modulator and, at the intersection point, the output drive pulse to the SMPS power switching transistor is terminated. The duty factor of the SMPS switching is then an inverse function of both feedback level and SMPS switching transistor current.

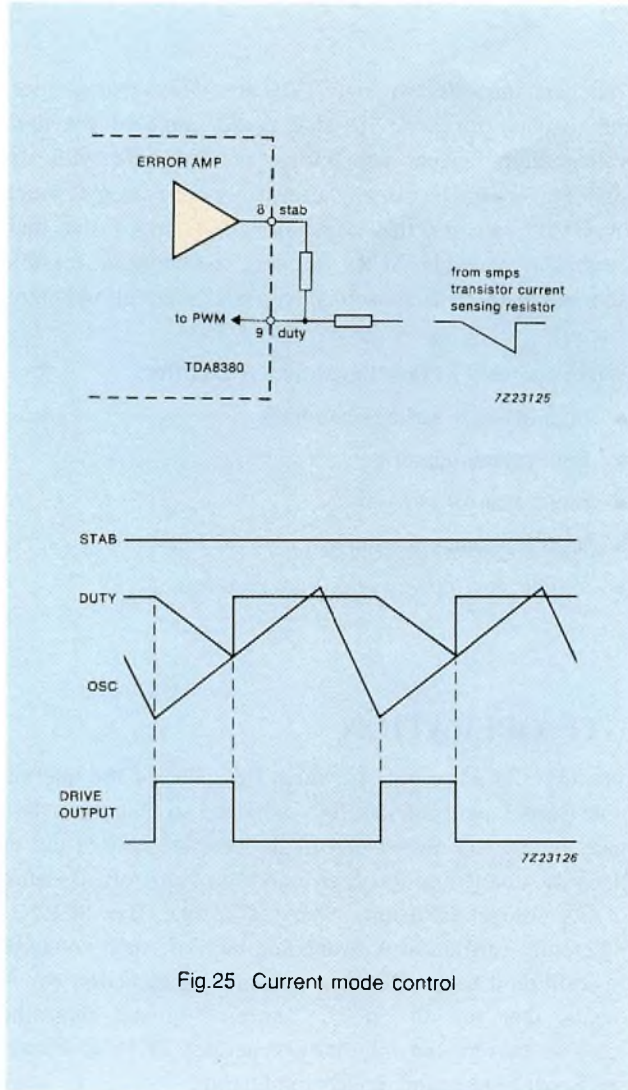


Fig.25 Current mode control

The GTO as a fast thyristor

ARTHUR WOODWORTH

The gate turn-off switch (GTO) was developed to meet the demand for a device that could combine the high voltage/high current capabilities of thyristors with the switching characteristics of transistors. The present range of GTOs satisfies this demand - switching faster than currently available SCRs as well as being a feasible alternative to transistors in many conventional switching circuits.

When operated as fast thyristors, GTOs offer:

- high off-state voltage handling
- high current handling
- rapid turn-off (<1 μs)
- high frequency operation
- simple, low-power gate drive requirements.

GTO OPERATION

The GTO is a thyristor in which the gains of the internal transistors have been carefully adjusted so that a negative gate voltage can divert part of the on-state current out of the gate, unlatching the device and turning it off. Because of its 4-layer structure, the GTO, like the SCR, is inherently capable of withstanding high off-state voltages. In addition it has an SCR's regenerative gate action which means that for all on-state currents greater than the latching current the internally generated drive is always sufficient to keep the device conducting.

Like any other semiconductor switch, the GTO does have some limitations, especially when used in the gate turn-off mode. Limitations such as:

Tail loss. A GTO used in, for example, a flyback converter (see Fig.1), has the turn-off current and voltage waveforms shown in Fig.2. The current flowing during time t is known as the tail current and is caused by the residual stored charge being swept from the GTO. During this time the voltage across the device is rising, leading to losses (present in any semiconductor switch) which limit the maximum usable power at a given operating frequency.

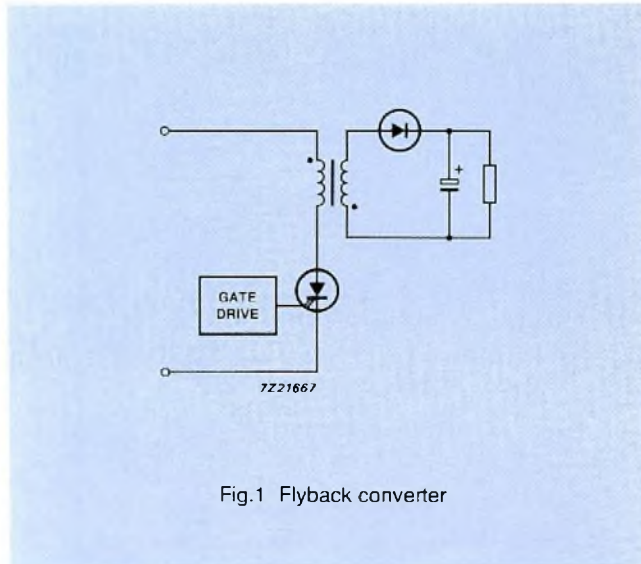


Fig.1 Flyback converter

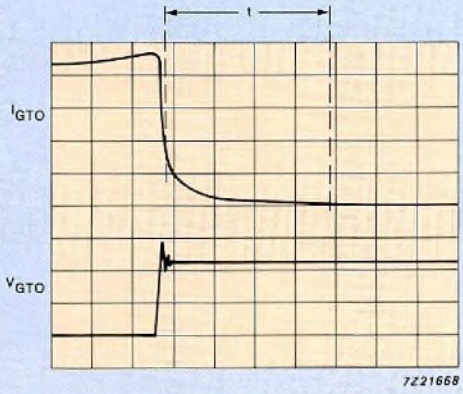


Fig.2 GTO turn-off waveforms

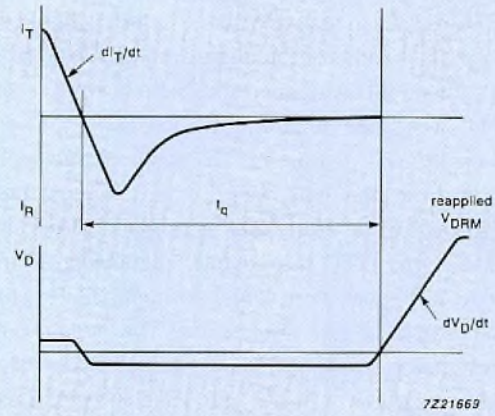


Fig.3 Turn-off time

Gate drive. To turn off a GTO, a negative gate voltage is needed and this causes part of the main current to be diverted through the gate. The gate drive circuit must be capable of sinking this current. Direct drive circuits can handle this current, but in circuits with isolated drive, the combination of a relatively complex drive circuit and high currents can cause difficulties. This problem also exists with the drives for bipolar transistors in similar circuits.

Maximum current. The maximum on-state current that a GTO can turn off at a given dV/dt is less than the maximum current that the device is capable of handling. Therefore, in a conventional switching circuit where the maximum current is the current to be turned off, the full capability of the GTO is not being used.

CONVENTIONAL THYRISTORS (SCR/ ASCR) AND THEIR LIMITATIONS

The regenerative action of the SCR ensures that when the anode current exceeds the latching current, the SCR is always turned fully on, even if the gate drive is removed. SCRs do, however, have two main limitations:

- they can be turned on via the gate but can only be turned off by reducing the anode current to near zero. This restricts the use of the SCR to circuits where the anode current regularly falls to zero, e.g. in mains-fed or resonant circuits
- it takes a relatively long time to remove their stored charge and to be completely turned off. The minimum off-time (t_q) of an SCR is the time taken for the charge stored in the SCR to be removed, see Fig.3. Until this charge is removed a reapplied voltage can cause the SCR to turn on again.

The value of t_q is important in determining the maximum usable operating frequency and the values of inductors and capacitors in forced commutation circuits. Reducing t_q will allow higher frequency operation, and reduce the size and cost of commutating components, but the minimum off-times achievable with the fastest conventional SCR, the ASCR, are around 6 µs, limiting their operating frequency to about 20 kHz.

OVERCOMING GTO LIMITATIONS

The limitations of the GTO when used in the gate turn-off mode are greatly reduced if the GTO is used in a conventional SCR circuit. The magnitude and duration of the GTO tail loss is proportional to the anode current at the point of turn-off. If the anode current is reduced to zero, which is the case in self-commutating or forced commutated SCR circuits, then the tail losses are zero. With no anode current at turn-off, the current in the gate circuit will be very low. This considerably reduces gate drive requirements.

Under these conditions, the maximum on-state current limitation disappears as the GTO is no longer controlling the current via the gate, and the full current rating can be utilized. Very large peak currents can then be handled without the saturation restrictions of a transistor.

OVERCOMING SCR LIMITATIONS

Situations can occur, particularly in resonant circuits during start-up, where the anode current does not return to zero. If this current is greater than the holding current,

a conventional SCR will not turn off. A GTO, however, can still be switched off using a suitable gate drive circuit. In ASCRs a negative voltage is often applied to the gate to extract some of the charge stored in the region under the cathode diffusion, and thus help keep t_q as short as possible. The gate area of an ASCR is, however, relatively small and so some of the stored charge will be a long way from the gate, see Fig.4(a). The negative potential has very little effect on this remote charge.

In contrast, the GTO has an inter-digitated pattern of gate/cathode diffusions (Fig.4(b)), so none of the stored charge is far from a gate connection. The negative gate voltage now has a strong influence over all of the stored charge which can be quickly and efficiently extracted. This gives a GTO an effective t_q of less than 1 µs, which is very much shorter than that possible with any ASCR.

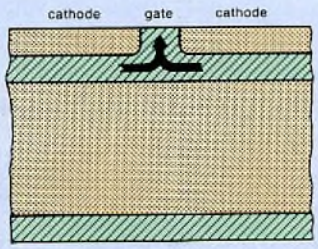


Fig.4(a) ASCR section

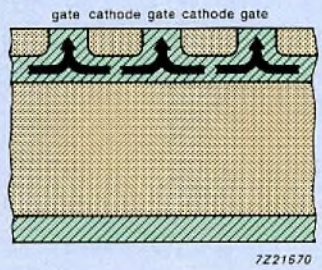


Fig.4(b) GTO section

APPLICATIONS

AC motor control

A three-phase AC motor control supply consists of three identical circuits, one for each phase. An example of one of these circuits using ASCRs is shown in Fig.5. Th1 and Th2 are the main thyristors which regulate the power. Diodes D1 and D2 carry the reactive and regenerative currents from the load to the supply. Th3 and Th4 are the commutation thyristors for Th1 and Th2 respectively.

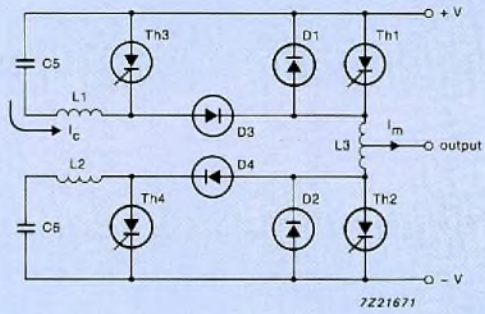


Fig.5 AC motor control circuit (one phase)

When it is required to turn-off one of the main thyristors, say Th1, which is passing load current I_m, Th3 is triggered. Because commutation capacitor C5 has already been charged to the supply voltage, triggering Th3 causes a sinusoidal current (I_c) to flow via Th3, L1 and C5. After one half cycle of I_c, the voltage on C5 has reversed, the current in Th3 is zero and Th3 turns off. The direction of I_c now reverses and flows via D3 to provide an increasing part of I_m. If I_c exceeds I_m, D1 is forward biased and there will be no current in Th1 which will start to turn off. If I_c exceeds I_m for a time greater than the t_q for the thyristor, Th1 will turn off completely and can block a re-applied forward voltage.

To turn off Th1, the commutation components must be large enough to supply a current in excess of the maximum possible I_m for a period greater than the t_q of the main thyristors. In a 4 kW drive using ASCRs with a t_q of 9 µs, C5 and C6 would need to be 650 nF and L1 and L2 would both be 48 µH. If, however, GTOs were used instead of ASCRs, the t_q would then be less than 1 µs allowing C5/C6 to be 72 nF and L1 /L2 to be 5.4 µH. This provides a very worthwhile reduction in the size and cost of the components.

Resonant converters

Although the concept of resonant converters has been known for many years, they have recently had a revival. One problem suffered by all switching devices in conventional circuits is that of switching loss. This occurs for example in the conventional flyback converter (Fig.1). At turn-on and turn-off, the rate of change of current and voltage is very high. The finite switching speed of the GTO incurs large switching losses. As the frequency and power of converters increase, switching losses increase and limit the safe area of operation for the device. To use a switching device beyond this limit, a different approach to circuit design is required. One option available is a resonant switch using a GTO.

In a resonant switch circuit shown in Fig.6, a capacitor, inductor and diode are added to the conventional flyback design to give the waveforms shown in Fig.7. When the GTO is turned on, the rate of rise of current is much slower, reducing turn-on loss. As the current passes through zero the voltage across C_a will be greater than the supply voltage, so the off-state voltage will appear across D_a and the GTO can be turned off without loss.

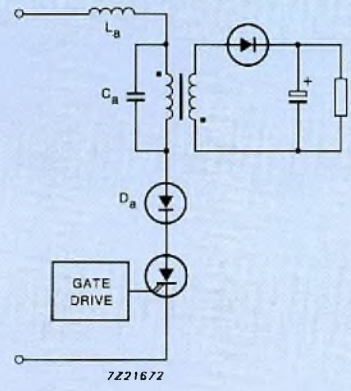


Fig.6 Resonant switch flyback converter

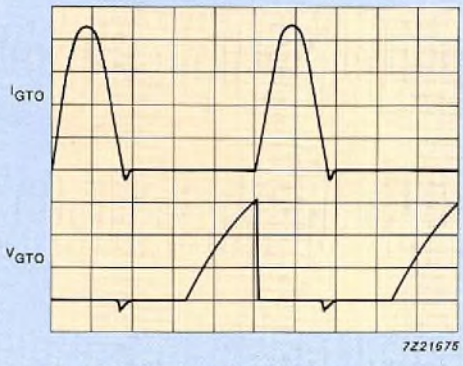


Fig.7 Resonant switch GTO waveforms

A possible disadvantage of this circuit is the large increase in peak current, which could cause drive difficulties if the switching device were a transistor. However, the GTO is essentially an SCR so its regenerative gate action automatically copes with peak on-state currents. Under certain circumstances peak currents of 550 A can be carried by a GTO with an average current rating of only 6.5 A, triggered by an initial gate drive of 0.5 A. This gives an effective DC current gain (hFE) of 1200 from a device with a voltage rating of 1500 V.

A common problem with high-power switching converters is that of mains harmonic distortion caused by large input smoothing capacitors. This problem can be overcome by using a resonant configuration. The circuit shown in Fig.8 is a mains-fed 1.2 kW HV power supply designed for use in a domestic appliance, so restricting mains interference was essential. To avoid using an expensive filtering circuit, a variation of a resonant switch boost converter was chosen.

A feature of resonant switch circuits is the almost fixed-duration pulse (determined by the LC resonance circuit), which means that the duty factor can be adjusted by varying the frequency and not the pulse width, thus giving a much greater range of adjustment. The range of adjustment is further increased by having a second resonant action during the delivery phases of each cycle. This means that the required output voltage can be obtained from a wide range of input voltages and there is no need for large smoothing capacitors. Typical values for the input capacitors are 2 µF, so the supply presents an almost resistive load to the mains.

The waveforms for the GTO in this circuit are as shown in Fig.9. At full power, the circuit operates at 40 kHz. At this frequency, the time between the zero crossing of the current and the reapplication of the forward voltage is less than 4 µs which precludes the use of conventional fast SCRs but is well within the t_q capabilities of GTOs.

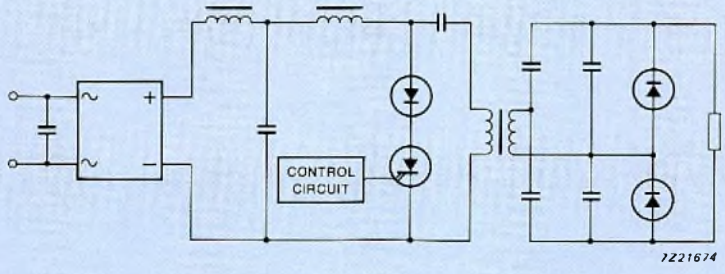


Fig.8 Resonant HV power supply

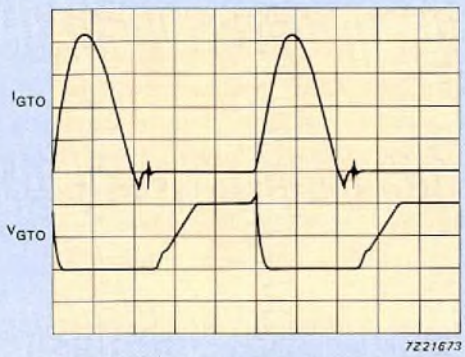


Fig.9 HV power supply GTO waveforms

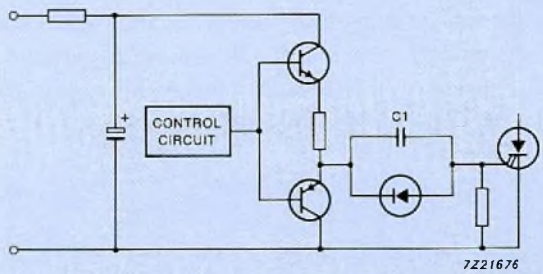


Fig.10 GTO gate drive

Figure 10 shows the type of gate drive used in this circuit. Because the required gate current is only 0.5 A, the transistors used are TO-92 types. The supply to the gate drive circuit is from a 15 V rail, while the negative gate drive is generated by the charge stored in C1 during turn-on. A buffer IC in the control circuit controls the drive by turning off the GTO when it senses that the voltage across the series diode is negative.

Abstracts

Engine management with the PCB83C552 single-chip 8-bit microcontroller

The PCB83C552 is an 8-bit single-chip high-performance CMOS microcontroller for use in real-time applications such as instrumentation, industrial control and engine management systems. It's a derivative of the 8051 and possesses its powerful instruction set. It also possesses dedicated on-chip peripherals for these applications, plus additional special function registers to control these on-chip peripherals. The PCB83C552 performs complete engine management for multi-point injection, ignition control, idle control and exhaust gas recirculation (EGR).

Inexpensive monochrome TV camera design – brings CCD imaging into everyday applications

For applications such as home-surveillance cameras, video phones, door security systems, automotive rear-view systems, etc., many of today's CCD TV cameras are over-complicated and thus needlessly expensive. For these reasons, we've designed a monochrome CCD camera that brings all the advantages of solid-state imaging within the price range of many consumers. The secret of our design is a simple but effective signal-processing technique specifically for low-cost image-sensors with pixel defects. And with simple processing of only the low frequency components of the image-sensor output signal, the influence of pixel defects on picture quality can be reduced to an acceptable level. The horizontal resolution of such a camera is, however, lower than usual but it is perfectly adequate for many applications.

HCMOS Analog Switches and Analog Multiplexers/Demultiplexers

High-speed CMOS (HCMOS) integrated analog switches have a lower on-resistance, a wider frequency response and switch even faster than standard CMOS switches such as those in Philips' HEF4000B series. In this publication, the design of the HCMOS analog switch and its features are described. These HCMOS switches and multiplexers are ideal for use in A/D conversion systems, signal source selectors, audio and video equipment, and in level shifters to name a few of the applications described. Each circuit is pin-compatible with the HEF4000B version except for the four completely new circuits in a range of ten. Each circuit has the standard HCMOS features such as wide operating voltage range and input/output protection circuitry.

The polygon gun...
...for a cleaner, sharper electron spot

One of the major advances to be introduced into Philips' latest colour picture-tube range is the new 'polygon' electron gun which solves a problem that has beset unitized guns since their inception over a decade ago: i.e. that of minimizing aberrations and associated effects in the electron-optical lens system to give a sharp, clean electron spot. Compared with conventional guns, the polygon gun has a larger electron-optical lens formed by an oval ridge surrounding three apertures whose profiles have been precisely configured to compensate non-radially symmetric electric field components. Reductions in spot size of up to 15% are possible with the polygon gun.

Integrated SMPS control circuit TDA8380

Although switched-mode power supplies are more efficient, smaller and lighter than conventional series regulator power supplies, the circuitry required to incorporate the necessary overload protection and to control the switching duty factor to compensate mains voltage and load variations is complex. To alleviate this problem and make an SMPS much easier to design, we have developed the integrated SMPS control circuit TDA8380 which can drive a variety of types of SMPS with a forward or flyback converter which can run in continuous or discontinuous current mode. It control the SMPS power throughput and regulation by pulse-width modulation (PWM) of a drive signal for a power switching transistor. PWM control is achieved by varying the duty factor of the SMPS power transistor switching between 0% and 80%.

GTO as a fast thyristor

The GTO switch combines the high voltage/high current capabilities of thyristors with the switching characteristics of transistors. When operated as fast thyristors, GTOs offer high frequency operation and simple, low-power gate drive requirements. Also, in contrast to conventional thyristors, the GTO's inter-digitated pattern of gate/cathode diffusions ensures that stored charge in the device is quickly and efficiently extracted, giving the GTO a very fast switching time. This article describes the operation of the GTO, discusses limitations of SCRs and GTOs and how to overcome them, and includes application examples.

Steuerung und Regelung von Verbrennungsmotoren mit dem 8-bit-Einchip-Mikrocontroller PCB83C552

Der PCB 83C552 ist ein 8-bit-Hochleistungs-Einchip-Mikrocontroller für Echtzeitanwendungen, z.B. in Meßgeräten, industriellen Steuerungen sowie Motorsteuer- und -regelsystemen. Er ist ein Derivat des Mikrocontrollers 8051 und verfügt über dessen leistungsfähigen Befehlssatz. Auf dem Chip sind außerdem für derartige Anwendungen geeignete pheriphere Einheiten sowie zusätzliche spezielle Funktionsregister integriert, die diese Einheiten steuern. Der PCB 83C552 übernimmt die komplette Motorsteuerung und -regelung für Mehrfach-Einspritzung, Zündeinstellung sowie Leerlauf- und Abgaseinstellung.

Preisgünstige Schwarzweiß-Fernsehkamera mit CCD-Frame-Transfer-Bildaufnehmer; Bauvorschlag

Für Anwendungen wie Heim-Überwachungskameras, Bildfernsprecher, Tür-Sicherungssysteme, Systeme, die in Kraftfahrzeugen die Rückbereichserkennung ermöglichen u.dgl., sind viele der heute eingesetzten CCD-Fernsehkameras zu kompliziert und daher unnötig teuer. Wir haben deshalb einen Bauvorschlag für eine Monochrom-CCD-Kamera entwickelt, die alle Vorteile der Festkörper-Bildaufnahme zu einem Preis bietet, der für viele Anwender attraktiv ist. Das Geheimnis unserer Konstruktion ist eine einfache aber wirksame Signalverarbeitungstechnik, die sich speziell für preisgünstige Bildaufnehmer mit Pixel-Fehlern eignet. Bei einfacher Verarbeitung nur der niederfrequenten Komponenten des Bildaufnehmer-Ausgangssignals läßt sich der Einfluß von Pixel-Fehlern auf die Bildqualität auf ein annehmbares Niveau verringern. Die Horizontalauflösung einer solchen Kamera liegt zwar unter den üblichen Werten, genügt für viele Anwendungen aber völlig.

HCMOS-Analogschalter und -Analog-Multiplexer/Demultiplexer

Schnelle integrierte CMOS-(HCMOS-)Analogschalter weisen einen kleineren Durchlaßwiderstand sowie einen breiteren Arbeitsfrequenzbereich auf; außerdem schalten sie noch schneller als Standard-CMOS-Schalter wie die der Reihe HEF 4000 B von Philips. Der vorliegende Beitrag beschreibt den Aufbau und die Leistungsmerkmale des HCMOS-Analogschalters. Die neuen HCMOS-Schalter und -Multiplexer eignen sich hervorragend für den Einsatz in A/D-Umsetzersystemen, Signalquellenwählern sowie Audio- und Videogeräten, um nur einige der beschriebenen Applikationen anzuführen. Alle Schaltungen - mit Ausnahme der vier völlig neu entwickelten Versionen innerhalb der zehn Schaltungen umfassenden Familie - sind anschlußkompatibel zur Reihe HEF 4000 B. Jede Schaltung weist die HCMOS-spezifischen Vorteile auf, z.B. einen breiten Versorgungsspannungsbereich und eingebaute Eingangs-/Ausgangsschutzschaltungen.

Das Polygon-Elektronenstrahlsystem mit dem schärferen Leuchtfleck

Eine der bedeutendsten Errungenschaften in der Elektronenoptik, die in der neuesten Farbbildröhrenreihe von Philips erstmalig zur Anwendung kommt, ist das neue "Polygon"-Elektronenstrahlsystem. Dieses Elektronenstrahlsystem löst ein Problem, das "unitized" Elektronenstrahlsysteme seit jeher beeinträchtigt, nämlich die Notwendigkeit, "Aberationen" und damit zusammenhängende Effekte im elektronenoptischen Linsensystem zu minimieren, um einen scharfen und sauberen Leuchtfleck zu erzielen. Im Vergleich zu konventionellen Elektronenstrahlsystemen hat das Polygon-System eine größere elektronenoptische Hauptlinse. Diese wird aus einem großen ovalen Steg gebildet, der die drei Aperturen umgibt. Deren Querschnitte sind exakt so geformt, daß symmetrische, nicht radiale Komponenten des elektrischen Feldes weitgehend kompensiert werden. Verringerungen der Leuchtfleckgröße um bis zu 15% sind mit dem Polygon-Strahlsystem möglich.

Integrierte Steuerschaltung TDA8380 für Schaltnetzteile (SMPS)

Die Hauptvorteile von Schaltnetzteilen (SMPS = Switch Mode Power Supply) liegen in höherem Wirkungsgrad, kleineren Abmessungen und geringerem Gewicht im Vergleich zu konventionellen Netzteilen mit Serienregelung. In den meisten Fällen ist jedoch ein erheblicher schaltungstechnischer Zusatzaufwand nötig, um den erforderlichen Überlastschutz zu realisieren und das Schalt-Tastverhältnis so zu steuern, daß Netzspannungsschwankungen und Laständerungen kompensiert werden. Um diesen Zusatzaufwand zu reduzieren und den Entwurf von Schaltnetzteilen erheblich zu erleichtern, wurde das SMPS-Steuer-IC TDA8380 entwickelt, das preisgünstige Schaltnetzteil-Applikationen in der Konsumelektronik und auch im professionellen Bereich erlaubt. Das IC ist sowohl in Sperrwandlern als auch in Durchflußwandlern einsetzbar. Es arbeitet mit Impulsbreitenregelung bei fester Frequenz und verfügt über zwei Startprozeduren: Softstart und Slowstart. Beim anlaufsicheren Slowstart beispielsweise wird das Tastverhältnis des Steuersignals für den Leistungstransistor, ausgehend von 12%, allmählich auf einen extern festlegbaren Wert (max. 80%) erhöht. Die internen Schutzschaltungen des IC wirken sowohl begrenzend als auch abschaltend mit anschließendem Neustart.

GTO als schneller, abschaltbarer Thyristor

Der GTO-Schalter verbindet die Fähigkeiten von Thyristoren zur Verarbeitung hoher Spannungen und Ströme mit den Schalteigenschaften von Transistoren. Beim Einsatz als schnelle Thyristoren ermöglichen GTOs hochfrequenten Betrieb mit geringem Schaltungsaufwand und kleiner Leistung an der Steuerelektrode. Außerdem sorgt - im Unterschied zu konventionellen Thyristoren - eine spezielle Struktur der Gate/Katoden-Diffusion bei GTOs dafür, daß die im Bauelement gespeicherte Ladung schnell und wirksam ausgeräumt wird, so daß GTOs sehr kurze Schaltzeiten aufweisen. Der vorliegende Artikel beschreibt den Betrieb des GTO, geht auf die Grenzen von Thyristoren (SCRs und GTOs) ein, wobei auch Möglichkeiten zu deren Überwindung aufgezeigt werden, und stellt darüber hinaus einige Applikationsbeispiele vor.

Caméra de télévision monochrome peu onéreuse munie de capteur d'image CCD pour transfert de charge

Pour des applications telles que les caméras de surveillance à domicile, les visiophones, les systèmes de protection de portes, les rétroviseurs pour voitures, etc., nombre de caméras de télévision CCD actuelles sont très complexes et donc inutilement coûteuses. Nous avons conçu à cet effet une caméra CCD monochrome offrant tous les avantages de la conception monobloc dans une gamme de prix accessible à la majorité des utilisateurs. Le secret de notre conception réside en une technique de traitement des signaux simple mais efficace, en particulier pour les capteurs d'image peu onéreux présentant un certain nombre de pixels défectueux. En traitant simplement les composantes basse fréquence du signal de sortie du capteur d'image, il est possible de réduire à un niveau acceptable l'influence des pixels défectueux sur la qualité de l'image. La résolution horizontale d'une telle caméra est toutefois plus faible qu'à l'ordinaire, mais est parfaitement adaptée à la plupart des applications.

Commutateurs analogiques HCMOS et multiplexeurs/ démultiplexeurs analogiques

Les commutateurs analogiques intégrés C-MOS à haute vitesse (HCMOS) ont une résistance plus faible à l'état passant, une réponse en fréquence plus large et assurent une commutation plus rapide que les commutateurs C-MOS standards, tels ceux de la série HEF4000B de Philips. Cette publication décrit la conception et les caractéristiques du commutateur analogique HCMOS. Ces commutateurs HCMOS et les multiplexeurs conviennent parfaitement aux systèmes de conversion analogiques-numériques, aux sélecteurs de source, aux équipements audio et vidéo ainsi qu'aux régulateurs de niveau, pour ne citer que quelques applications décrites. Chaque circuit est compatible broche à broche avec la version HEF4000B, sauf pour les quatre nouveaux circuits dans la série de dix. Chaque circuit présente les caractéristiques standard HCMOS, comme une large gamme de tension de fonctionnement et des circuits de protection entrée/sortie.

Le canon polygon...
... pour un faisceau d'électrons plus propre et plus "pointu"

L'une des améliorations principales dont est dotée la dernière série de tubes couleur de Philips est le nouveau canon à électrons "polygon", destiné à résoudre un problème qui a accompagné l'ensemble des canons depuis leur apparition il y a une dizaine d'années, à savoir réduire les aberrations et les effets secondaires présents dans le système optique électronique afin d'offrir un faisceau d'électrons pointu et propre. Comparé au canon ordinaire, le canon polygon est muni de lentilles optiques électroniques formées d'une bordure ovale entourant trois ouvertures dont les profils ont été précisément conçus pour compenser les composantes d'un champ électrique qui ne sont pas radialement symétriques. Le canon polygon permet des réductions de la taille du faisceau pouvant atteindre 15%.

Contrôle des moteurs à explosion grâce au microcontrôleur de 8 bits à une seule puce PCB83C552

Le PCB83C552 est un microcontrôleur C-MOS performant à une seule puce de 8 bits, utilisé dans les applications en temps réel comme les systèmes d'équipement d'instrument, de contrôle industriel et de réglage des moteurs. Il s'inspire du 8051 et dispose d'un jeu d'instructions puissant. Il est également muni de périphériques sur puce spécialisés pour ces applications, ainsi que d'enregistreurs supplémentaires pour fonction spéciale afin de contrôler ces périphériques sur puce. Le PCB83C552 contrôle totalement le moteur à injection multipoint, le réglage d'allumage, le réglage du régime stationnaire et la circulation de gaz d'échappement (EGR).

Circuit intégré TDA8380 pour le contrôle des alimentations à découpage (SMPS)

Bien que les alimentations à découpage soient plus efficaces, plus petites et plus légères que celles des régulateurs conventionnels, les circuits nécessaires pour la protection contre les surcharges et au contrôle du facteur de forme du découpage destiné à compenser les variations de tension alimentions et de charge sont complexes. Pour résoudre ce problème et faciliter la conception des alimentations à découpage, nous avons mis au point le circuit intégré TDA8380 pour le contrôle des alimentations à découpage pouvant commander divers types d'alimentation avec convertisseur de type forward ou flyback, fonctionnant en courant continu ou alternatif. Il contrôle le rendement et la régulation de puissance des alimentations à découpage par modulation d'impulsions en largeur ou en durée (PWM) d'un signal de commande pour un transistor commutateur de puissance. Le contrôle de modulation d'impulsions en largeur ou en durée s'obtient en faisant varier le facteur de forme du découpage du transistor entre 0% et 80%.

Thyristor blocable (GTO) utilisé comme thyristor rapide

Le GTO blocable allie les caractéristiques de haute tension/courant élevé des thyristors et les caractéristiques de commutation des transistors. Lorsqu'ils sont utilisés comme thyristors rapides, les GTO offrent un fonctionnement à haute fréquence et nécessitent une commande de porte de faible puissance. Ainsi, à la différence des thyristors conventionnels, la topologie interdigitée de diffusion des portes/cathodes permet l'extraction rapide et efficace de la charge emmagasinée dans le dispositif, ce qui donne au GTO un temps de commutation très rapide. Cet article décrit le fonctionnement du GTO, analyse ses limites ainsi que celles des Redresseurs Silicium Commandé (SCR), indique comment les surmonter et présente des exemples d'application.

Control del motor con el microcontrolador de 8-bit y un solo chip, PCB83C552

El PCB83C552 es un microcontrolador CMOS de 8 bits en un solo chip de altas prestaciones para uso en aplicaciones de tiempo real, tales como sistemas de instrumentación, control industrial y regulación de motores. Es un producto derivado del 8051 y tiene su potente juego de instrucciones. Asimismo tiene incorporados en el chip periféricos dedicados para estas aplicaciones y registradores adicionales de función especial para controlar estos periféricos en chip. El PCB83C552 controla en su totalidad el motor para inyección de multipuntos, control de ignición, control sin carga y recirculación de gases de escape (EGR).

Cámara de televisión monocroma de bajo coste que utiliza sensor de imagen con transferencia de cuadro CCD

En aplicaciones tales como sistemas de vigilancia, videoteléfonos, sistemas de seguridad de puertas, sistemas retrovisores del automóvil, etc., muchas de las cámaras TV CCD de hoy en día son sumamente complicadas y por lo tanto innecesariamente caras. De ahí que hayamos diseñado una cámara CCD monocroma que ofrece todas las ventajas de la formación de imágenes de estado sólido a un precio que está al alcance de muchos consumidores. El secreto de nuestro diseño es un método sencillo, pero eficaz de procesamiento de la señal para sensores de imagen de bajo coste con defectos de los elementos de imagen. Procesando tan sólo los componentes de baja frecuencia de la señal de salida del sensor de imagen se consigue reducir a un nivel aceptable la influencia de los defectos de los elementos en la calidad de la imagen. Si bien la resolución horizontal de esta cámara es algo menor que la normal, es perfectamente adecuada para múltiples aplicaciones.

Conmutadores analógicos HCMOS y multiplexores/demultiplexores analógicos

Los conmutadores analógicos integrados de alta velocidad CMOS (HCMOS) tienen una resistencia en conducción más baja, una respuesta de frecuencia más amplia y una conmutación incluso más rápida que los CMOS standard, como los de las series HEF4000B de Philips. En esta publicación se describen el diseño del conmutador analógico HCMOS y sus características. Estos conmutadores HCMOS y multiplexores son ideales para uso en sistemas de conversión analógico/digital, selectores de fuente de señal, equipo de audio y video y en cambiadores de nivel, por citar algunas de las aplicaciones descritas. Excepto para los cuatro nuevos circuitos de la serie de diez, cada uno de los circuitos es compatible en patillas con el HEF4000B. Cada uno de los circuitos tiene las características standard HCMOS como son, un amplio margen de tensiones de funcionamiento y circuitos protectores de entrada/salida.

El cañón poligonal...
...para un punto electrónico más limpio y nítido

Uno de los principales adelantos que se ha introducido en la última serie de tubos de imagen en color de Philips es el nuevo cañón electrónico "poligonal" que viene a solucionar un problema que ha perseguido a los cañones de construcción, en forma de unidad normalizada, desde su aparición hace una década, es la minimización de aberraciones y efectos secundarios en el sistema óptico electrónico que ofrece un punto electrónico nítido y limpio. Comparado con los cañones corrientes, el poligonal tiene una lente electrónica óptica mayor que está formada por tres aberturas ovaladas circundantes con resaltes interiores, cuyos perfiles se han configurado con toda exactitud para compensar los componentes de campo eléctrico simétricos no radiales. Con el cañón poligonal se consigue reducir hasta un 15% el tamaño del punto.

Circuito integrado de control de SMPS, TDA8380

Aunque las fuentes de alimentación por conmutación (SMPS) son más eficientes, más pequeñas y más ligeras que las que tienen regulador, los circuitos que hacen falta para incorporar la protección necesaria contra exceso de carga y para controlar el factor de trabajo de conmutación destinado a compensar las variaciones de carga y de tensión de red son muy complejos. Para solucionar este problema y hacer una SMPS mucho más fácil de diseñar, hemos desarrollado el circuito integrado de control de SMPS, TDA8380 capaz de accionar varios tipos de SMPS con un conversor directo o inverso que funciona con corriente continua o alterna. Controla el rendimiento y regulación de potencia de un SMPS mediante modulación del ancho de impulsos (PWM) de una señal excitadora para un transistor conmutador de potencia. La modulación del ancho de impulsos se logra variando el factor de trabajo de la conmutación del transistor de potencia SMPS entre 0 y 80%.

GTO como tiristor rápido

El conmutador GTO combina las características de alta tensión y alta corriente de los tiristores con las características conmutadoras de los transistores. Cuando se utilizan como tiristores rápidos, los GTOs ofrecen un funcionamiento de alta frecuencia y requisitos excitadores de puerta sencillos y de baja potencia. Además, a diferencia de los tiristores corrientes, los GTOs modelo interdigitalizado de difusiones de puerta/cátodo garantizan que la carga almacenada en el dispositivo se extrae rápida y eficientemente, lo que da al GTO un tiempo de conmutación muy rápido. El presente artículo describe el funcionamiento del GTO, analiza las limitaciones de los SCRs y GTOs y la forma de superarlas e incluye varios ejemplos de aplicación.

Authors

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