Options for plotting waveforms will be provided.

All output files will use a random record length directoried access structure. Directories will be placed in separate files to enable almost unlimited expansion.

Fortran 77 file access statements and character variables will be used.

Error messages will be read from disc files.

The current version has been evolving since 1979. Structured coding techniques have made enhancements and modifications relatively easy to incorporate. The major problem in adding new features is usually the limited 64K byte address space in the HP-1000 computer. This ofter requires restructuring of overlays.

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A Programmable Precision Voltage-Step Generator for Testing Waveform Recorders

HOWARD K. SCHOENWETTER, SENIOR MEMBER, IEEE

Abstract—**A pulse generator for testing the approximate step-response of waveform recorders is described. The initial and final levels of voltage steps are each programmable within the range of ±1 V for a 50-Ω termination and within ±5 V for a high-impedance load. Voltage steps within these ranges settle to within ±0.02 percent of full-scale range (FSR) in less than 30 and 40 ns, respectively, for a load capacitance ≤30 pF. The corresponding 10-90-percent transition durations are approximately 7 and 12 ns.**

I. Introduction

PULSE GENERATORS with well-characterized step-like voltage transitions are desirable for testing the step-response of waveform recorders and other very wide-band devices that employ attenuators, amplifiers, or A/D converters. As part of the National Bureau of Standards (NBS) program to develop methods for characterizing waveform recorders and other wide-band devices a number of step generator or waveform standards have been developed, using various techniques. For example: The step generator described in [1] and [2] employs very fast, precision Schottky diode switching circuits to obtain an output step from +0.50 to 0.00 V with a transition duration of 600 ps. Reference [3] describes the development of a solid-state waveshaping filter that yields a transition duration of 400 ps, when the filter is excited by a tunnel diode step generator.[1] The voltage step generation described in this paper complements the above step generators. It has a considerably longer transition duration, but has the following fea-

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The author is with the Electrosystems Division, The National Bureau of Standards, Washington, DC 20234.

[1] These three papers also briefly describe or reference other pulse generators or waveform standards that have been developed for testing high-speed instruments.

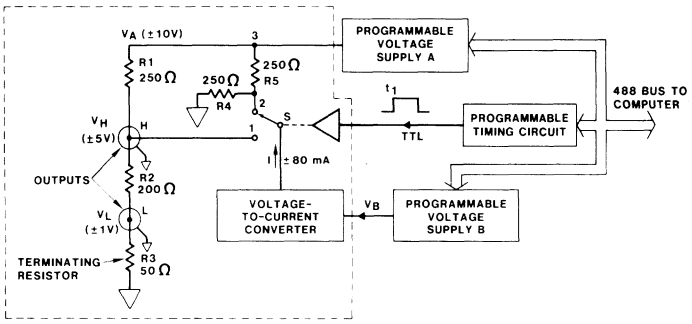

Fig. 1. Precision pulse generator. Pulse level following voltage step (transition) is determined by V_A. Amplitude and polarity of transition are determined by current I, which is a linear function of V_B. Voltage ranges are +5 and ±1 V from outputs H and L, respectively. Pulse width and repetition rate are determined by the TTL input from the timing circuit.

tures, not generally available before: 1) very smooth voltage transitions with known settling times (ST's) to within ±0.02 percent, 2) programmability of voltage transitions between any two levels in the ±5-V range, where the voltage level following the transition is known (or can be established) to better than 0.1 percent; 3) any duty cycle and repetition rate from single shot to 10 MHz (within minimum 50 ns ON and OFF time constraints), determined by the TTL input pulse; and 4) packaging of the pulse generator output circuit for direct connection to the test device, thus avoiding losses from a connecting coaxial cable.

II. General Description

A functional diagram of the pulse generator is shown in Fig. 1. Two output ranges are provided: a ±5-V range from output H, intended for high-impedance loads, and a ±1-V range from output L for 50-Ω-loads. Operation is as follows: the voltage-to-current converter linearly converts programmable voltage V_B to current I over the range of ±80 mA. When the TTL input is HIGH, current I is steered to output 2 of switch S. Output voltage V_H is determined by the programmable voltage V_A and the ratio $(R2+R3)/(R1+R2+R3)$ formed by the resistive voltage divider. Hence, $V_H = V_A/2$. When the TTL input is LOW, current I is steered to output 1 of S, changing V_H by IR_p V, where R_p is the parallel resistance of $R1$ and $(R2+R3)$. Thus $V_H = V_A/2 + IR_p$. Resistance R_p, equal to 125 Ω, is also the source impedance for V_H. The low-level output V_L is equal to $V_H/5$.

Switch S operates within a few nanoseconds after the TTL input changes state. Also, when it switches current I from terminal 1 to termimal 2, all active elements are isolated from terminal 1. Consequently, the transition from $(V_A/2 + IR_p)$ to $V_A/2$, is an exponential waveform determined by R_p and the total capacitance between terminal 1 and ground. Since the transition to $V_A/2$ involves only passive elements, it can be much more accurately characterized than the reverse transition, which involves active elements. Therefore, the transition to $V_A/2$ is recommended for waveform recorder testing. Output voltage $V_L(t)$ has a smaller settling time than $V_H(t)$, but has essentially the same waveshape. The pulsewidth and repetition rate are determined by the timing circuit, which is under computer control, as are voltage supplies A and B, via an IEEE 488 bus. In practice, the timing circuit is a programmable pulse generator with TTL-type output pulses.

Since rapid load current changes cause output voltage transients in most commercial voltage supplies, dummy load R4-R5 and complementary switching circuits in current switch S and the voltage-to-current converter are employed to maintain constant load currents for voltage supplies A and B. Also, terminal 3, placed physically close to $R1$, is carefully bypassed so that the impedance to ground is essentially zero for the frequency range of interest. In order to enhance the effective accuracies of V_H and V_L, corrections to the resistance ratios and values of V_A can be stored in a computer for later application to test data. Since the relative heat dissipation in $R1$ and $(R2+R3)$ varies with changes in V_A, I and pulse duty cycle, resistors $R1$ and $R2$ (metal film) were chosen to have small temperature coefficients.

As indicated above, connector L is usually terminated in a 50-Ω impedance. This impedance can be a 50-Ω coaxial termination, or the input impedance of a test or measuring device. If the input connector of the latter device is internally connected to a 50-Ω transmission line, it may be desirable to have a 50-Ω output impedance from the step generator. This is provided by internally soldering a 56-Ω resistor between connector L and ground. This circuit change decreases the ranges of V_L and V_H to approximately ±0.55 and ±4.75 V, respectively. The computer can, of course, be programmed to output selected values of V_H and V_L within these ranges.

The pulse generator was designed for use in automated test systems. However, the pulse generator output circuit, shown within the dashed lines of Fig. 1, can also be used with manually adjustable power supplies, and the TTL pulses can be obtained from a manually adjustable pulse generator.

III. Detailed Description

The pulse generator output circuit, shown within the dashed lines of Fig. 1, is packaged in a small, lightweight container that is separate from the voltage supplies and timing circuit. Output connectors H and L are male BNC connectors which permit direct connection to a waveform recorder, or other measuring device, without the use of a coaxial cable. The pulse generator actually consists of two, essentially complementary, voltage step generators—one for each polarity of transistion. A simplified schematic diagram of the circuit used for producing positive voltage steps is shown in Fig. 2. Transistors $Q1$ and $Q2$ perform the function of switch S in Fig. 1, switching current I to terminal 1 or I' to terminal 2. Collector currents I and I' are proportional to the common base current gains of $Q1$ and $Q2$, and typically differ by less than 2 percent. The magnitude of I is approximately $(|V_B|-7)/125$. (Example: for a 6-V step at connector H, I = 48 mA and $|V_B| = 13$). Schottky TTL buffers $U1$ and $U2$ provide the drive currents for $Q3$ and $Q4$, which alternately bias $Q1$ and $Q2$ off. Operation is as follows: prior to the TTL input pulse, the outputs of $U1$ and $U2$ are LOW and HIGH, respectively, so that $Q3$ is biased off and $Q4$ is conducting. Therefore, $Q2$ is biased off and $Q1$ conducts current I to terminal H, yielding an output voltage $V_H = VA/2 - IR_p$. Upon application of the TTL pulse at time T_1, the outputs of $U1$ and $U2$ switch to

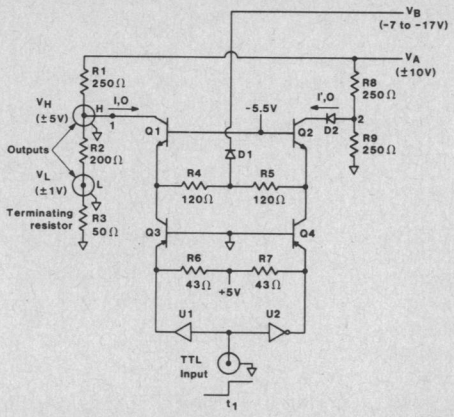

Fig. 2. Simplified diagram of circuit for producing positive voltage steps. Transistors $Q1$ and $Q2$ perform the function of switch S in Fig. 1.

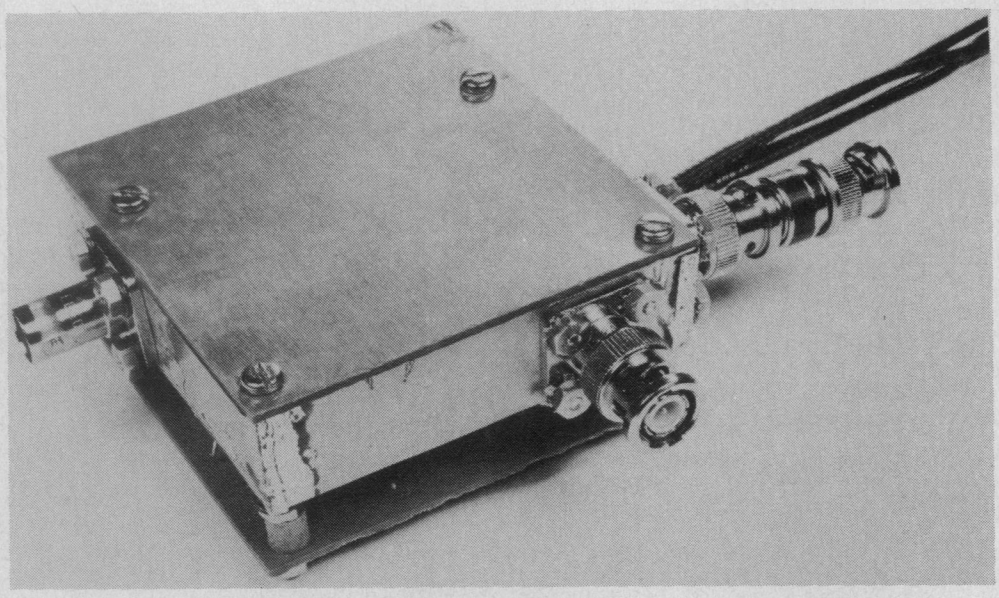

Fig. 3. Laboratory model of pulse generator output circuit.

HIGH and LOW levels, respectively, switching $Q3$ on and $Q4$ off. This action switches $Q1$ off and $Q2$ on. Consequently, voltage V_H switches to level $V_A/2$.

Except for some modification of the TTL buffer circuits and the biasing of the lower pair of transistors, the circuit for producing negative voltage steps is essentially the complement of the circuit shown in Fig. 2. A latching DPDT relay is employed to connect $Q1$ or its complementary counterpart to connector H or to ground. A second DPDT relay is used to apply +5 V to $Q3$, $Q4$, $U1$, $U2$, or their counterparts. Thus programming the pulse generator includes pulsing the appropriate relay windings to select the voltage step polarity. Diodes $D1$ and $D2$ protect $Q1$ and $Q2$ when these transistors are disabled.

A laboratory model of the pulse generator output circuit is shown in Fig. 3. Its dimensions are approximately 7.6 × 7.6 × 3.2 cm, excluding connectors, and its weight is 200 g. A 7.6 × 7.6 × 1.9-cm chassis made of 0.025-cm-thickness brass was used for component mounting. Except for the connectors, the discrete components were mounted on both sides of the 7.6 × 7.6-cm plane of the chassis, using miniature teflon feedthrough terminals and direct soldering to the chasis. Two small printed circuit boards were used for the TTL buffers. The protective covers are made of plastic instead of metal to minimize weight and component capacitance to ground. No electromagnetic interference has been experienced in laboratory use with this construction.

IV. Measurement Methods

The voltage transistions from the step generator can be divided into two parts: 1) the latter 1–2 percent of the transition in which differential voltage measurements are made between $V(t)$ and the "final" value, using ST measurement techniques; and 2) the part that proceeds it, in which the measured values of voltage have some estimated maximum error ϵ_m, relative to the "true" values of $V(t)$. For small capacitive loads, the rate of change of $V(t)$ from the step generator is in the order of 1000 V/μs. The estimated uncertainty ϵ_m in measuring voltages that change this rapidly is approximately ±(2 percent

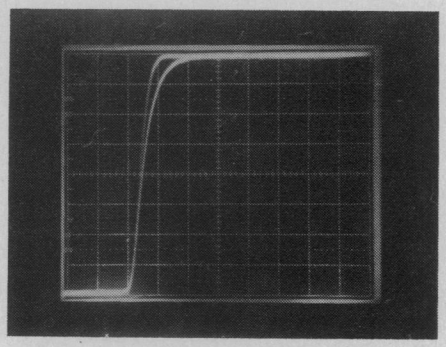

Fig. 4. Transition of V_H from −5 to +5 V, and transition of V_L from −1 to +1 V. The horizontal time base was 10 ns/cm for both traces, and in both cases, the vertical sensitivity was adjusted to give the full-screen deflections shown. V_L has the smaller transition duration.

FSR + 3 mV).[2] This uncertainty applies to voltages obtained from a 50-Ω source and in the range of ±500 mV. Measurement of voltages from sources with higher output impedances or larger voltage ranges will require the use of voltage dividers, resulting in increased uncertainty. It is planned to use a combination of the APMS and ST measurements to characterize the step generator waveform.

Since high-speed ST measurements are susceptible to systematic errors, it is very desirable to have at least two independent methods for making a given ST measurement. Independent methods are generally available for making ST measurements as short as 40 ns to within an error of 0.01 percent [6]. The sampling voltage tracker (SVT) is a fast analog comparator circuit, designed for analyzing very high-speed periodic signals [7]. Similar circuits have been used recently to measure the ST's of 8-bit [8] and 12-bit [9] D/A converters (DAC's) as short as 5 and 35 ns, respectively, to within 1/2 least significant bit (LSB). Peak detector circuits have been used at NBS as an independent check on ST measurements as short as about 10 ns. Some applications of this circuit are described in [10].

A version of the SVT, peak detector circuits, and a sampling oscilloscope were used to characterize the output waveforms of the step generator described in this paper. For the purpose of comparing the results from these methods of measurement, all measurements were made on the positive transition for the 50- and 125-Ω outputs (see waveform in Fig. 4).

The SVT consists of a high-speed sampling comparator and a voltage integrator in a feedback loop, and can be represented by Fig. 5. The strobe pulses, 5- to 10-ns wide, cause the input waveform $f(t)$ to be sampled (compared with the output voltage V_D of the integrator) at instants in time coinciding with the trailing edges of these pulses. Assume that the period of $f(t)$ is T and that the value $f(t_1)$ is to be measured. Then, the strobe pulses must be timed to sample $f(t)$ at times $t_1, t_1 + T, t_1 + 2T, \cdots$. The result of these comparisons is to drive V_D positive or negative until it nearly equals the value of $f(t)$ at the instants of comparison. If some other value of $f(t)$, say $f(t_2)$, is to be measured, $f(t)$ must be sampled at times $t_2, t_2 + T, t_2 + 2T, \cdots$, etc.

[2]Based on measurements using the NBS Automatic Pulse Measurement System (APMS) [4], [5].

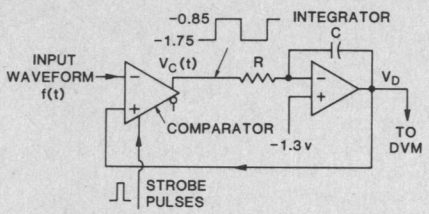

Fig. 5. Sampling voltage tracker (SVT). Input waveform $f(t)$ is sampled (compared with voltage V_D) at instants in time coinciding with the trailing edge of strobe pulses. The comparator has an ECL output.

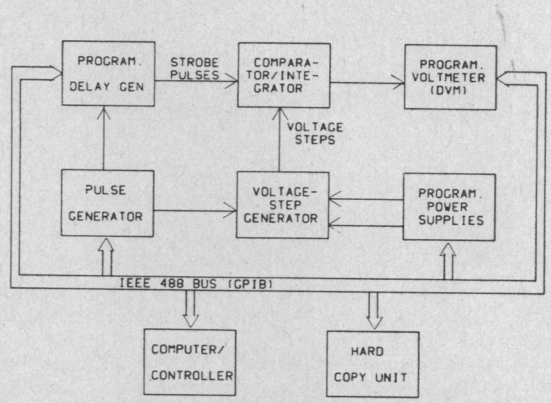

Fig. 6. System to measure settling time and transition duration of voltage steps from NBS Voltage-Step Generator. DC voltage from comparator/integrator equals voltage from step generator at instant of strobe pulse. DVM output, representing step-generator response, is plotted by controller and copy unit. Step-generator function block is actually generator output circut.

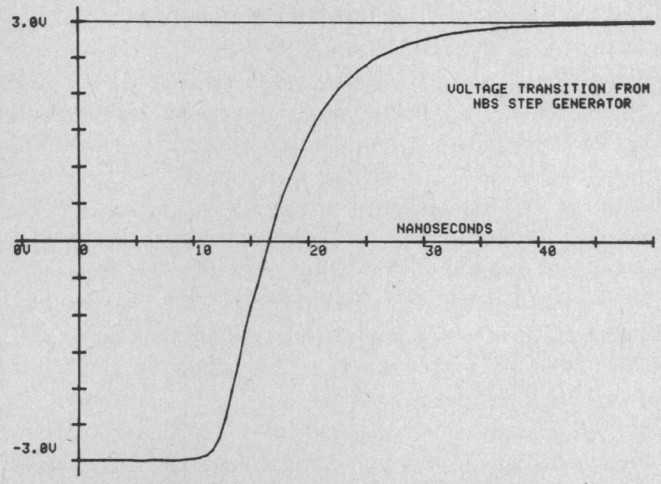

Fig. 7. Plot by system shown in Fig. 6 of −3 to +3 V transition of step-generator, when loaded with 30-pF capacitance.

The SVT (labeled comparator/integrator) was employed in the automatic measuring system shown in Fig. 6, with the delay generator programmed to have delay steps (increments) of 0.5 ns. The maximum allowable voltage range for the comparator in the SVT is ±3 V. Fig. 7 is a plot of a −3 to +3-V transition of the step generator, when loaded with 30-pF capacitance, a typical input capacitance for waveform recorders. Based on tabulated DVM readings, the transition duration (10-90-percent rise time) was 11 ns and the ST's to within ±0.1 and ±0.02 percent of FSR were 35 and 39 ns, respectively. When the load capacitance was decreased to 6

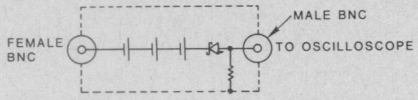

Fig. 8. Peak detector using small H_g hearing aid batteries, ~1.4 V each. Reverse bias on diode is determined by number of batteries employed. Shunt capacitance of diode is less than 1 pF. Terminating resistance is typically less than 180 Ω.

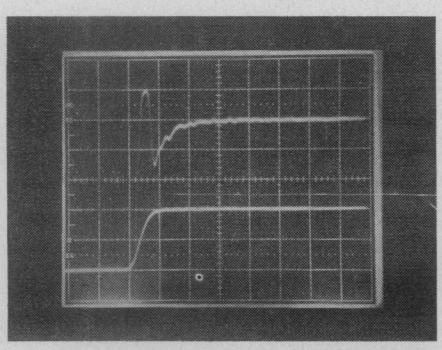

Fig. 9. Upper trace shows peak detector response to 2-V transition of V_L (lower trace). Sweep speed is 10 ns/cm and detector sensitivity is 0.25 percent of 2 V FSR/cm. The initial narrow pulse in detector output is caused by shunt capacitance of the detector diode (see Fig. 8). Waveform following this pulse accurately represents transition of V_L.

pF, the input capacitance of the measuring system, the corresponding ST's decreased to 17 and 22 ns. The transition duration decreased to 5.9 ns. ST measurements, using a peak detector, agreed with the above values to within ±10 percent. With a 30-pF load, the ST of the 2-V output was approximately 28 ns to ±0.02 percent of FSR and the transition duration was less than 7 ns. The ST measurement was made with a peak detector. The peak detector used for negative transitions is shown in Fig. 8. Battery and diode polarities are reversed for positive transitions. The voltage step (applied to the female BNC connector) is adjusted so that the diode conducts during approximately the last 1 percent of the voltage transition. This permits the latter part of a transition to be examined, using a sensitive range of the oscilloscope. Since the minimum battery voltage is 1.4 V and the diode forward drop is ~0.3 V, the ST of the 2-V output was obtained using approximately a −0.3 to +1.7 V transition.

Fig. 9 shows a ST measurement of a 2-V transition from connector L, using a peak detector with negligible input capacitance (~3 pF) and a calibrated sensitivity of 0.25 percent of FSR/cm. The sweep speed was 10 ns/cm. The measured ST, approximately 12 ns to within 0.2 percent of FSR, was used as a check on a similar measurement using a sampling oscilloscope with a 50-Ω input impedance. For the latter measurement, connector V_L was shunted with a 56-Ω resistor to obtain a 50-Ω output impedance. This decreases the FSR to 1.11 V, as was discussed previously. Fig. 10 shows that the ST is approximately 10 ns to with 0.2 percent of FSR.

V. Conclusion

A pulse generator has been designed which has very fast, smooth transitions between programmable initial and final levels. These levels are selectable within the range of ±1 V for a 50-Ω termination and within ±5 V for a high-impedance load. An SVT circuit has been used to measure the voltages

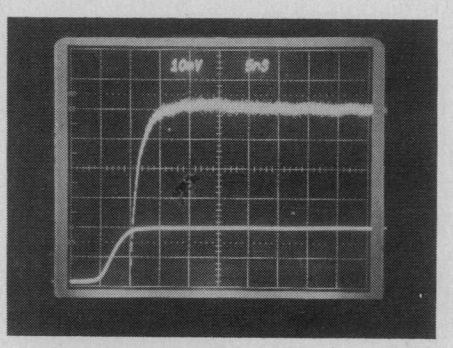

Fig. 10. Upper trace shows sampling ocilloscope response to 1.11-V transition from connector L of step generator (lower trace).

during these transitions. These measurements indicate that the transitions are monotonic, settle smoothly to within ±0.02 percent of FSR, and are approximately exponential in shape. Peak detector measurements confirm the smooth settling to selectable settling errors ranging from 2 to 0.02 percent. At this time, insufficient information is available on the SVT circuit to estimate its measurement accuracy on voltages changing at rates in the order of 1000 V/μs. Therefore, it is planned to characterize the fastest part of the step generator transitions using the APMS. The estimated APMS accuracy is ±(2 percent of FSR + 3 mV); however, its range is limited to ±500 mV and its input impedance is 50 Ω. In order to measure larger voltage ranges from higher impedance sources, without using voltage dividers, efforts will be made to determine the SVT measurement accuracy for very fast waveform.

Acknowledgment

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