PRODUCT SPECIFICATION

8296N-PR

Wi-Fi Dual-band 2x2 + Bluetooth 5.2

PCIE Combo Module

Version:v1.1

Customer: _____

Customer P/N: _____

Signature: _____

Date: _____

Office: 14th floor, Block B, phoenix zhigu, Xixiang Street, Baoan District, Shenzhen

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8296N-PR Module Datasheet

	Part NO.	Description
Ordering Information	FG8296NPRX-00	QCA6696,2.4G&5GHz a/b/g/n/ac/ax Wi-Fi 2T2R +BT5.2, 23x23mm,PCIE+UART/PCM,2antenna type,车规

CONTENTS

Revision History

Version	Date	Contents of Revision Change	Draft	Checked	Approved
V1.0	2023/03/03	New version	FC	LXY	QJP
V1.1	2023/09/25	NC pin37 BT port,update BT power value	LXP	LXY	QJP

1. General Description

1.1 Introduction

8296N-PR is a highly integrated nodule,supporting 802.11 ax Wi-Fi, Bluetooth (BT) 5.2. It supports simultaneous operation on 2.4 GHz and 5 GHz, also known as Dual Band Simultaneous (DBS). compliant with AEC-Q100 Qualification Specifications for Automotive Applications.

1.2 Description

Model Name	8296N-PR
Product Description	Support Wi-Fi/Bluetooth functionalities
Dimension	L x W x H: 23 x 23 x 5.6 mm
Host Interface	Support PCIE/UART / PCM
Operating temperature	-40°C to 85°C
Storage temperature	-55°C to 150°C

2. Features

General

- Compliant with IEEE 802.11a/b/g/n/ac/ax
- Supports 2x2 Multi-User Multiple-Input Multiple-Output(MU-MIMO)
- Dual Band Simultaneous (DBS) with dual MAC, up to 1774.5 Mbps data rate (2x2+2x2 11ax DBS)
- Dual band 2.4G/5G chains,20 MHz/40 MHz channel bandwidth for 2.4 GHz and 20 MHz/40 MHz/80 MHz channel bandwidth for 5 GHz
- Dynamic Frequency Selection
- Dedicated Bluetooth antenna
- Offloading traffic for minimal host utilization at 11ac/ax speeds

WLAN Interface

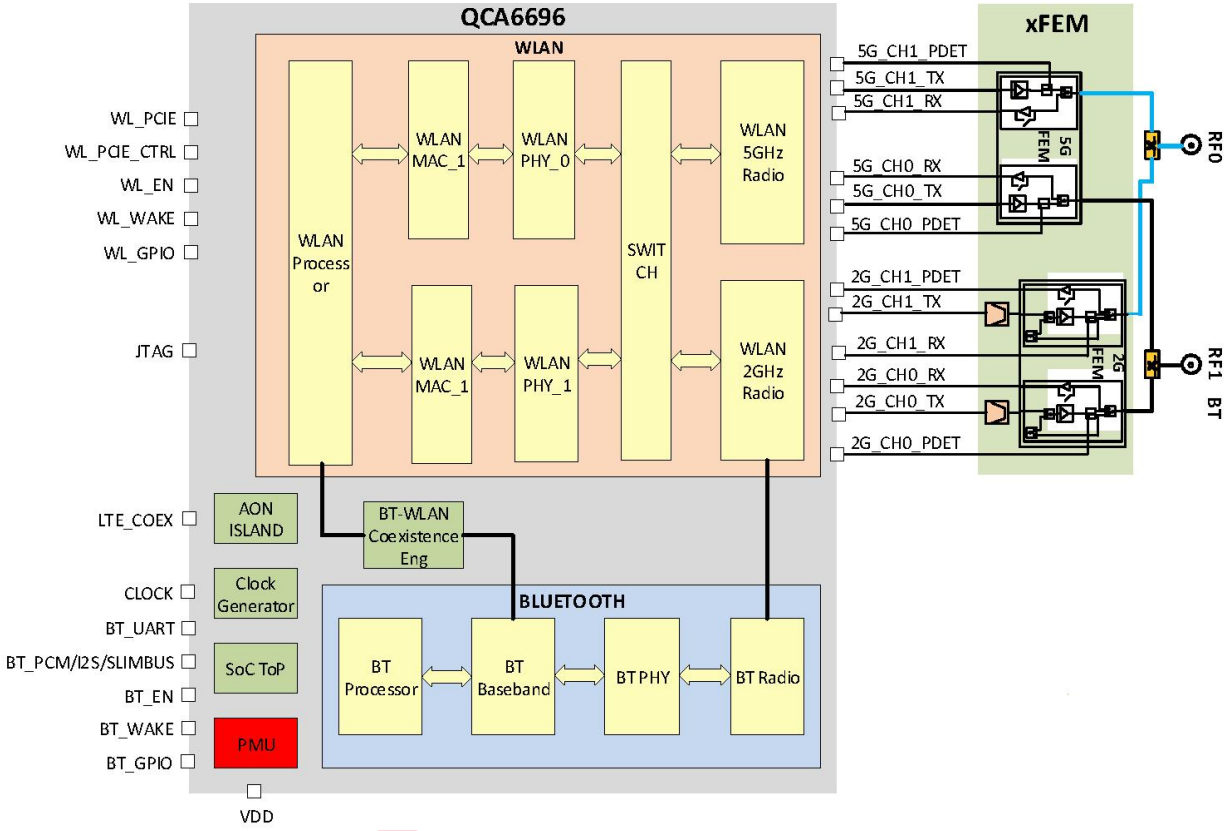
- Low power PCIe (w/L1 sub-state) interface

Bluetooth Features

- Compliant with Bluetooth 5.2 and ANT+

- Supports Bluetooth low energy (BLE), with 1 Mbps and 2 Mbps BLE long range
- Split ACL support for A2DP true stereo
- Backward compatible with previous Bluetooth standards.
- Flexible interface Slimbus/PCM/I2S for Bluetooth audio

3. Block Diagram



4. General Specification

4.1 2.4GHz RF Specification

Feature	Description	
WLAN Standard	IEEE 802.11 b/g/n Wi-Fi compliant	
Frequency Range	2.400 GHz ~ 2.4835 GHz (2.4 GHz ISM Band)	
Number of Channels	2.4GHz：Ch1 ~ Ch14	
Test Items	**Typical Value**	**EVM**
Output Power[2]	802.11b /11Mbps : 19.5dBm ± 3 dB	EVM ≤ -10dB
	802.11g /54Mbps : 17dBm ± 3 dB	EVM ≤ -25dB
	802.11n /MCS7 : 16dBm ± 3 dB	EVM ≤ -28dB
	802.11ac /MCS9 : 14.5dBm ± 3 dB	EVM ≤ -32dB
	802.11ax /MCS11 : 13dBm ± 3 dB	EVM ≤ -35dB
Spectrum Mask	Meet with IEEE standard	
Freq. Tolerance	±20ppm	
SISO Receive Sensitivity (11b,20MHz) @8% PER	- 1Mbps @ -94 dBm	≤-82 dBm
	- 11Mbps @ -85 dBm	≤-76 dBm
SISO Receive Sensitivity (11g,20MHz) @10% PER	- 6Mbps @ -90 dBm	≤-82 dBm
	- 54Mbps @ -71 dBm	≤-65 dBm
SISO Receive Sensitivity (11n,20MHz) @10% PER	- MCS=0 @ -90 dBm	≤-82 dBm
	- MCS=7 @ -69 dBm	≤-64 dBm
SISO Receive Sensitivity (11n ,40MHz) @10% PER	- MCS=0 @ -87 dBm	≤-82 dBm
	- MCS=7 @ -66 dBm	≤-61 dBm
SISO Receive Sensitivity (11ac,20MHz) @10% PER	- MCS=0 @ -90 dBm	≤ -82 dBm
	- MCS=8 @ -64 dBm	≤ -59 dBm
SISO Receive Sensitivity (11ac ,40MHz) @10% PER	- MCS=0 @ -87 dBm	≤ -79 dBm
	- MCS=9 @ -59 dBm	≤ -54 dBm
SISO Receive Sensitivity (11ax,20MHz) @10% PER	- MCS=0 @ -90 dBm	≤-82 dBm
	- MCS=11 @ -60 dBm	≤-52 dBm
SISO Receive Sensitivity (11ax ,40MHz) @10% PER	- MCS=0 @ -87 dBm	≤-79 dBm
	- MCS=11 @ -57 dBm	≤-49 dBm
Maximum Input Level	802.11b : -10 dBm	
	802.11g/n : -20 dBm	

4.2 5GHz RF Specification

Feature	Description	
WLAN Standard	IEEE 802.11a/n/ac/ax, Wi-Fi compliant	
Frequency Range	5.15 GHz ~ 5.850 GHz (5 GHz Band)	
Number of Channels	5.0GHz：Please see the table[1]	
Test Items	**Typical Value**	**EVM**
Output Power[2]	802.11a /54Mbps: 14.5 dBm ± 3 dB	EVM ≤ -25dB
	802.11n /MCS7: 13 dBm ± 3 dB	EVM ≤ -28dB
	802.11ac VHT80/MCS9: 11 dBm ± 3 dB	EVM ≤ -32dB
	802.11ax HE80/MCS11: 10 dBm ± 3 dB	EVM ≤ -35dB
Test Items	**Test Value**	**Standard Value**
SISO Receive Sensitivity (11a,20MHz) @10% PER	- 6Mbps @ -90 dBm	≤-82 dBm
	- 54Mbps @ -71 dBm	≤-65 dBm
SISO Receive Sensitivity (11n,20MHz) @10% PER	- MCS=0 @ -90 dBm	≤-82 dBm
	- MCS=7 @ -69 dBm	≤-64 dBm
SISO Receive Sensitivity (11n,40MHz) @10% PER	- MCS=0 @ -87 dBm	≤-82 dBm
	- MCS=7 @ -66 dBm	≤-61 dBm
SISO Receive Sensitivity (11ac,20MHz)@10% PER	- MCS=0, NSS1 @ 90 dBm	≤-82 dBm
	- MCS=8, NSS1 @ -64 dBm	≤-59 dBm
SISO Receive Sensitivity (11ac,40MHz) @10% PER	- MCS=0, NSS1 @ -87 dBm	≤-76 dBm
	- MCS=9, NSS1 @ -59 dBm	≤-51 dBm
SISO Receive Sensitivity (11ac,80MHz) @10% PER	- MCS=0, NSS1 @ -84 dBm	≤-79 dBm
	- MCS=9, NSS1 @ -56 dBm	≤-51 dBm
SISO Receive Sensitivity (11ax,20MHz) @10% PER	- MCS=0 @ -90 dBm	≤-82 dBm
	- MCS=11 @ -60 dBm	≤-52 dBm
SISO Receive Sensitivity (11ax,40MHz) @10% PER	- MCS=0 @ -87 dBm	≤-79 dBm
	- MCS=11 @ -57 dBm	≤-49 dBm
SISO Receive Sensitivity (11ax,80MHz) @10% PER	- MCS=0 @ -84 dBm	≤-76 dBm
	- MCS=11 @ -54 dBm	≤-46 dBm
Maximum Input Level	802.11a/n: -30 dBm	
Antenna Reference	Small antennas with 0~2 dBi peak gain	

[2]outputpower may update in future version.

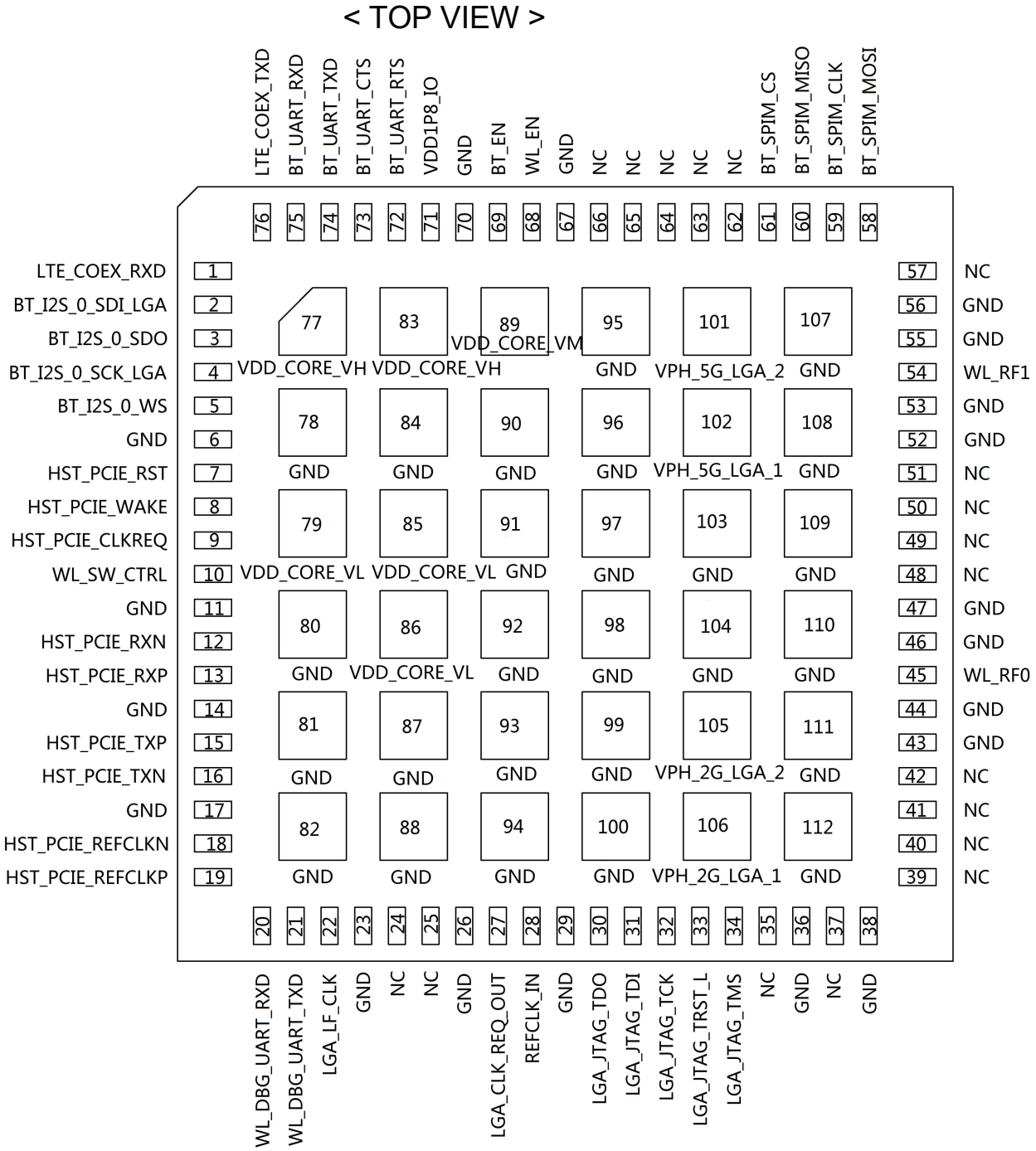
[1]5GHz(20MHz) Channel table

4.3 Bluetooth Specification

Feature	Description
General Specification	
Bluetooth Standard	BDR(1Mbps),EDR(2Mbps & 3Mbps),LE(1Mbps),2LE(2Mbps)
Host Interface	UART
Frequency Band	2400 MHz ~ 2483.5 MHz
Number of Channels	79 channels for classic,40 channels for BLE
Modulation	GFSK, π/4-DQPSK,8DPSK
RF Specification	
Output Power , tolerance ±3 dB	
Level9	**CL1**(dBm)
BDR Output Power	9
EDR Output Power	7
BLE Output Power	9
Sensitivity, tolerance : /	
Sensitivity @ BER=0.1% for GFSK (1Mbps)	-89
Sensitivity @ BER=0.01% for π/4-DQPSK (2Mbps)	-86
Sensitivity @ BER=0.01% for 8DPSK (3Mbps)	-85
Sensitivity @ BLE=30.8% for LE (1Mbps)	-89
Sensitivity @ BLE=30.8% for 2LE (2Mbps)	-89
Maximum Input Level	GFSK (1Mbps):-20dBm
	π/4-DQPSK (2Mbps) :-20dBm
	8DPSK (3Mbps) :-20dBm

5. Pin Definition

5.1 Pin Outline



5.2 Pin Definition details

NO.	Name	Type	Description	Voltage
1	LTE_COEX_RXD	I	GPIO10, LTE coexistence UART RXD	VDDIO
2	BT_I2S_0_SDI_LGA	I	GPIO4, Bluetooth I2S Data In ,PCM IN	VDDIO
3	BT_I2S_0_SDO	O	GPIO5, Bluetooth I2S Data Out, PCM OUT	VDDIO
4	BT_I2S_0_SCK_LGA	I	GPIO7, Bluetooth I2S Clock In, PCM CLK	VDDIO
5	BT_I2S_0_WS	I	GPIO6, Bluetooth I2S Word Select, PCM SYNC	VDDIO
6	GND		Ground connections	
7	HST_PCIE_RST	I	GPIO57, PCIe reset	VDDIO
8	HST_PCIE_WAKE	O	GPIO58, PCIe wake, an external pull-up resistor to VDDIO_1P8 is required	VDDIO
9	HST_PCIE_CLKREQ	O	GPIO59, PCIe clock request, an external pull-up resistor to VDDIO_1P8 is required	VDDIO
10	WL_SW_CTRL	O	GPIO46, Control PMIC outputs	VDDIO
11	GND		Ground connections	
12	HST_PCIE_RXN	I	PCIe Receive differential signal	VDDIO
13	HST_PCIE_RXP	I		VDDIO
14	GND		Ground connections	
15	HST_PCIE_TXP	O	PCIe transmit differential signal	VDDIO
16	HST_PCIE_TXN	O		VDDIO
17	GND		Ground connections	
18	HST_PCIE_REFCLKN	I	PCIe clock differential input signal	VDDIO
19	HST_PCIE_REFCLKP	I		VDDIO
20	WL_DBG_UART_RXD	I/O	GPIO45, UART RXD for debug,WLAN I2C SDA	VDDIO
21	WL_DBG_UART_TXD	I/O	GPIO44, UART TXD for debug， WLAN I2C SCL	VDDIO
22	LGA_LF_CLK	I	GPIO14, External 32.768 KHz sleep clock input.	VDDIO
23	GND		Ground connections	
24	NC		Floating (NC)	
25	NC		Floating (NC)	
26	GND		Ground connections	
27	LGA_CLK_REQ_OUT	O	GPIO56, (CLK_REQ_OUT is a hardware control signal. It is driven by a signal in AO domain. Whenever the chip is in ACTIVE or WAKEUP state CLK_REQ_OUT will	VDDIO

			be high to request Reference Clock. This signal is used to enable the 48 MHz TCXO.) Not supported in this version.	
28	REFCLK_IN	I	Crystal intput. Vpp = 1.3V (Max)This pin is an input pin if clock signal is from TCXO, AC coupling may be required when TCXO is used. Not supported in this version.	1.7V
29	GND		Ground connections	
30	LGA_JTAG_TDO	I/O	TDO for JTAG. NC if JTAG is not used	VDDIO
31	LGA_JTAG_TDI	I/O	TDI for JTAG. NC if JTAG is not used	VDDIO
32	LGA_JTAG_TCK	I/O	TCK for JTAG. NC if JTAG is not used	VDDIO
33	LGA_JTAG_TRST_L	I/O	TRST for JTAG. NC if JTAG is not used	VDDIO
34	LGA_JTAG_TMS	I/O	TMS for JTAG. NC if JTAG is not used	VDDIO
35	NC		Floating (NC)	
36	GND		Ground connections	
37	NC	I/O	Floating (NC)	
38	GND		Ground connections	
39	NC		Floating (NC)	
40	NC		Floating (NC)	
41	NC		Floating (NC)	
42	NC		Floating (NC)	
43	GND		Ground connections	
44	GND		Ground connections	
45	WL_RF0	I/O	Chain0 RF antenna port for 2.4G/5G, and 2antenna type BT port.	
46	GND		Ground connections	
47	GND		Ground connections	
48	NC		Floating (NC)	
49	NC		Floating (NC)	
50	NC		Floating (NC)	
51	NC		Floating (NC)	
52	GND		Ground connections	

53	GND		Ground connections	
54	WL_RF1	I/O	Chain1 RF antenna port for 2.4G/5G	
55	GND		Ground connections	
56	GND		Ground connections	
57	NC		Floating (NC)	
58	BT_SPIM_MOSI		GPIO8, BT SPI MOSI	VDDIO
59	BT_SPIM_CLK		GPIO13, BT SPI CLK	VDDIO
60	BT_SPIM_MISO		GPIO13, BT SPI MISO	VDDIO
61	BT_SPIM_CS		GPIO9, BT SPI CS	VDDIO
62~66	NC		Floating (NC)	
67	GND		Ground connections	
68	WL_EN	I	WLAN enable signal from Host External weak pull down may be required.	VDDIO
69	BT_EN	I	BT enable signal from Host External weak pull down may be required.	VDDIO
70	GND		Ground connections	
71	VDD1P8_IO	P	VDDIO 1.8V input	1.8V
72	BT_UART_RTS	O	GPIO3, Bluetooth UART RTS signal	VDDIO
73	BT_UART_CTS	I	Bluetooth UART CTS signal	VDDIO
74	BT_UART_TXD	O	Bluetooth UART TX signal	VDDIO
75	BT_UART_RXD	I	Bluetooth UART RX signal	VDDIO
76	LTE_COEX_TXD	O	GPIO11, LTE coexistence UART TXD	VDDIO
77	VDD_CORE_VH	P	1.95 V power input for RFA and PCIe	1.95V
78	GND		Ground connections	
79	VDD_CORE_VL	P	0.95 V power supply input	0.95V
80~82	GND		Ground connections	
83	VDD_CORE_VH	P	1.95 V power input for RFA and PCIe	1.95V
84	GND		Ground connections	
85	VDD_CORE_VL	P	0.95 V power supply input	0.95V
86	VDD_CORE_VL	P	0.95 V power supply input	0.95V
87~88	GND		Ground connections	
89	VDD_CORE_VM	P	1.35 V power input	1.35V
90~100	GND		Ground connections	
101	VPH_5G_LGA_2	P	5G FEM power supply	3.85V
102	VPH_5G_LGA_1	P	5G FEM power supply	3.85V
103	GND		Ground connections	
104	GND		Ground connections	

105	VPH_2G_LGA_2	P	2G FEM power supply	3.85V
106	VPH_2G_LGA_1	P	2G FEM power supply	3.85V
107~112	GND		Ground connections	

P:POWER I:INPUT O:OUTPUT

6. Electrical Specifications

6.1 Power Supply DC Characteristics

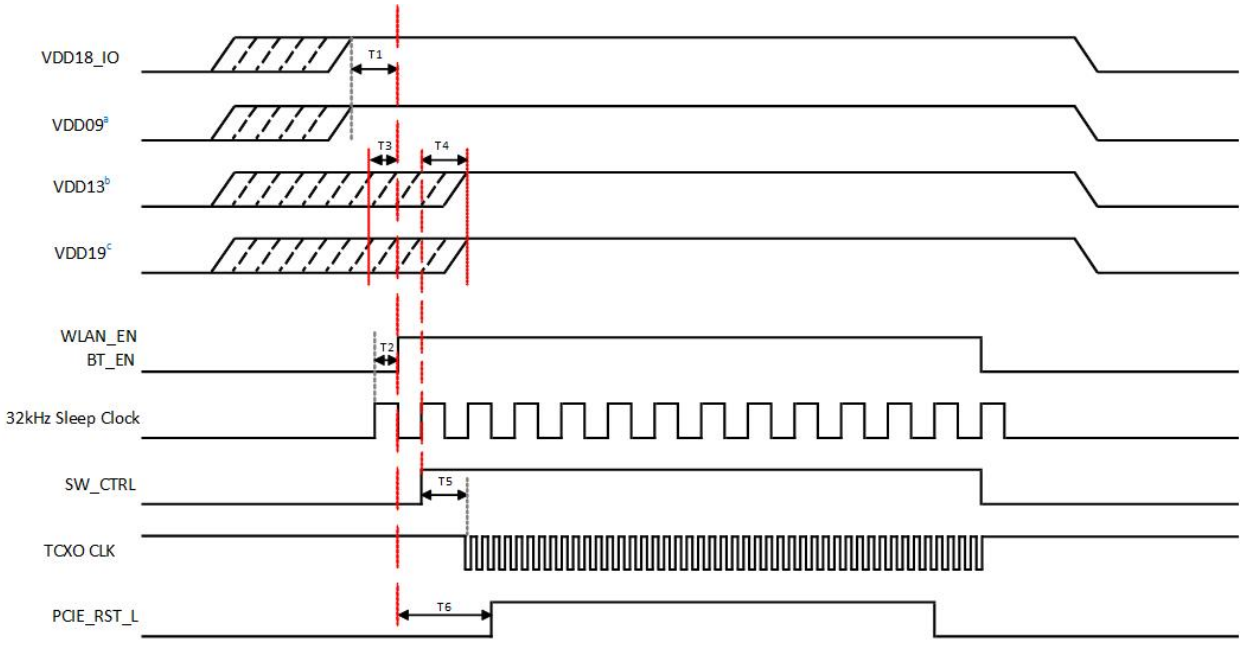
	MIN	TYP	MAX	Unit
Operating Temperature	-40	25	85	deg.C
VDD1P8_IO	1.71	1.8	1.89	V
VDD_CORE_VH	1.85	1.95	2.0	V
VDD_CORE_VL	0.9	0.95	1.2V	V
VDD_CORE_VM	1.28	1.35	1.42	V
VPH_X_LGA	3.3	3.85	4.2	V

6.2 Power Consumption

Power Consumption	0.95V	1.35V	1.95V	VDDIO1.8V	3.85V
	1.2A	400mA	250mA	30mA	1A

6.3 Interface Circuit time series

6.3.1 power on and power off sequence timing



a VDD09: VDD_PMU_AON_I, VDD095_PMU, VDD09_PMU_RFA_I
b VDD13: VDD13_PMU_RFA_I, VDD13_PMU_PCIE_I
c VDD19: VDD19_PMU_RFA_I, VDD19_PMU_PCIE_I

Symbol	Parameter	Min	MAX	Unit
t1	VDD18_IO/VDD09 avalid to WLAN_EN or BT_EN is asserted	4	-	ms
t2	Sleep Clock (32.768kHz) valid to WLAN_EN or BT_EN is asserted	0	-	μs
t3	VDD13/VDD19 b valid to WLAN_EN or BT_EN is asserted without SW_CTRL usage	0	-	μs
t4	SW_CTRL c is asserted to VDD13/VDD19 d valid	-	350	μs
t5	SW_CTRL valid to TCXO Reference Clock stabilization	-	2	ms
t6	WLAN_EN valid to PCIE_RST_L de-assert	15	-	ms

a Can be in any order.

b Can be in any order.

c It is about 700 μs SW_CTRL becomes asserted after WL_EN/BT_EN valid.

d Can be in any order.

6.3.2 HCI UART interface

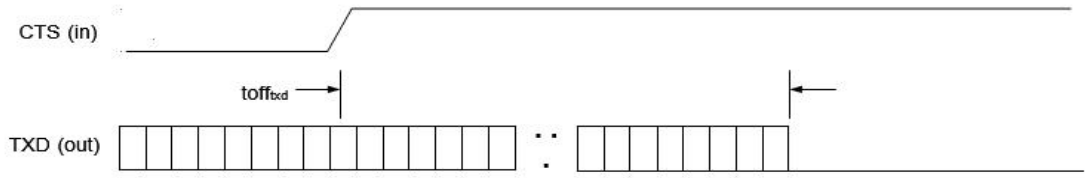
Supports the HCI UART transport layer as defined in the Bluetooth Core Specification, Version 4.0, Volume4, Part A. In addition to communication with the host, the HCI UART interface also supports Bluetooth software (inband) sleep control. The HCI UART interface circuits use digital I/O pins that receive power from the VDD_IO supply. Their I/O performance specifications meet the requirements stated in Section 3.4.

The HCI UART transport layer uses the following settings for RS232.

UART parameter	Value
Number of data bits	Eight
Parity bit	No parity
Stop bit	One stop bit
Flow control	RTS/CTS (hardware)
Flow off response	Two bytes maximum
Supported transport	9.6 K, 19.2 K, 38.4 K, 57.6 K, 115.2 K, 125 K, 230.4 K, 250 K, 460.8 K,
bit rates (bps) a	500 K, 720 K, 921.6 K, 1 M, 1.6 M, 2 M, 3 M, 3.2 M, with an accuracy of +1.5/-2.5%

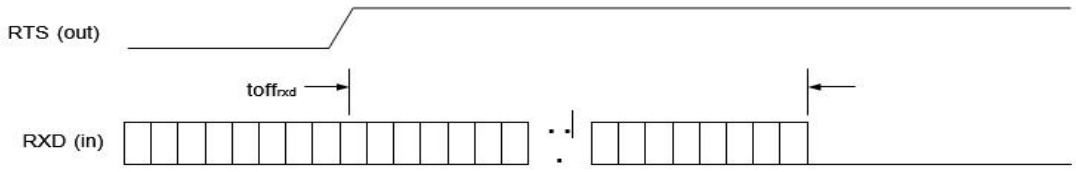
a:UART maximum baud rate is 3.2 Mbps.

The following figure and table show the HCI UART transmit timing:



Parameter	Description	Min	Typ	MAX	Unit
tofftxd	Delay from CTS to TXD stop	-	-	1	byte

The following figure and table show the HCI UART receive timing:



Parameter	Description	Min	Typ	MAX	Unit
$toff_{rxd}$	Delay from RTS to RXD stop	16	-	-	byte

6.3.3 Bluetooth PCM interface

The pulse coded modulation (PCM) interface connects the QCA6696 device to the phone’s audio interface, or to peripheral devices, such as a codec. The PCM interface circuits use digital I/O pins that receive power from the VDD_IO supply. Their I/O performance specifications meet the requirements stated in Section 3.4.

The QCA6696 PCM interface has been designed to minimize audio latency.

The following table lists the typical audio latencies for various packet types:

Packet type	Audio latency
HV3/EV3 TeSCO = 6, WeSCO = 0	4.4 ms
EV3 TeSCO = 6, WeSCO = 2	5.7 ms
EV3 TeSCO = 6, WeSCO = 4	6.9 ms

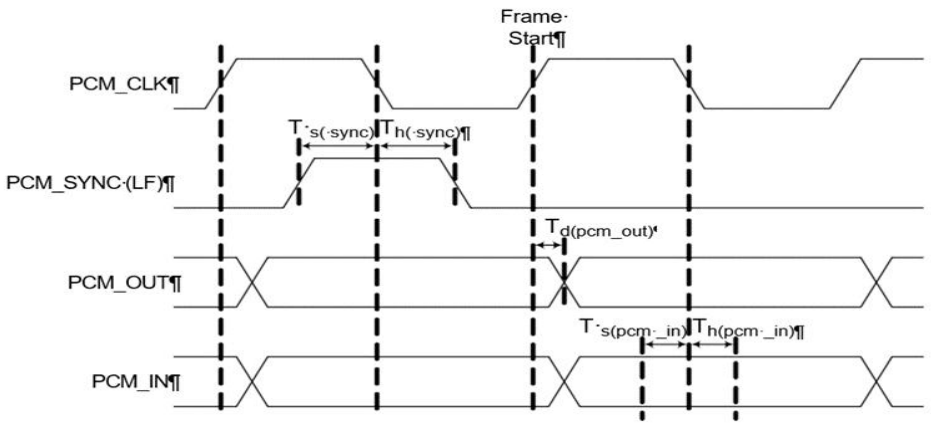
The PCM interface is configured to operate as master or slave. In each case, the PCM_IN pin is the data receive terminal (an input), and the PCM_OUT pin is the data transmit terminal (an output). The clock and sync pins function as inputs or outputs, depending on whether the QCA6696 PCM interface is configured as a master or slave:

- When the QCA6696 PCM interface is the master: PCM_CLK and PCM_SYNC are outputs from the QCA6696 to the PCM bus slave(s).
- When the QCA6696 PCM interface is the slave: PCM_CLK and PCM_SYNC are inputs to the QCA6696 device from the PCM bus master.

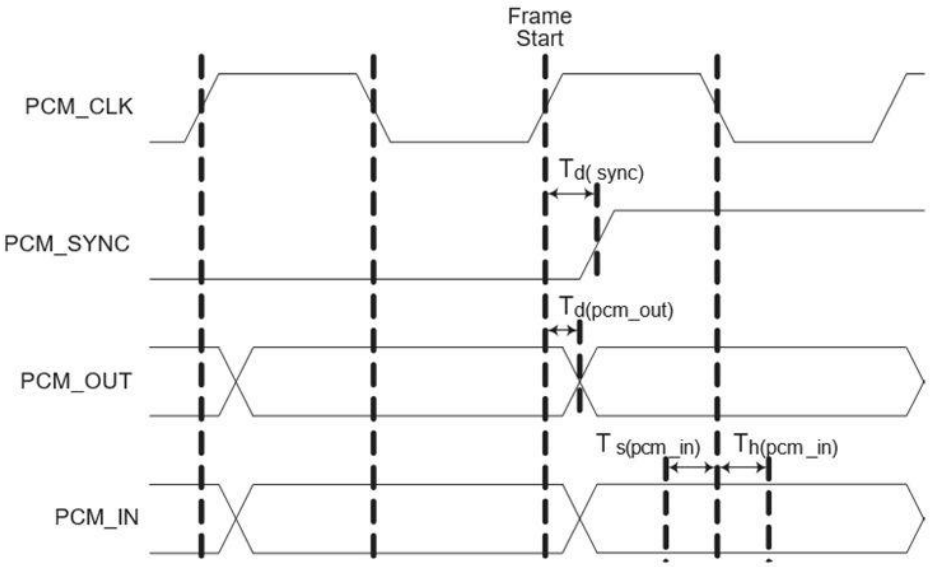
The following table lists the PCM interface specifications:

Parameter	Description	Min	Typ	MAX	Unit
Clock rate (slave)	Determined by the master	64	-	2.048	kHz
Clock rate (master)	(32 MHz * N/4,000), in which N is an integer, 8 ≤ N ≤ 256	64	-	2.048	kHz
Frame size		1	8	256	Bits
Slot size		1	13	16	Bits
Slot size	Number of slots that can be configured per frame	1	-	32	Slots/frame

Example timing diagrams and specifications for slave and master configurations are described in the following figures and tables:



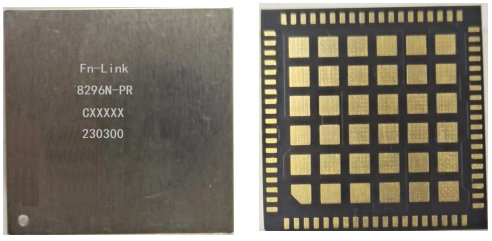
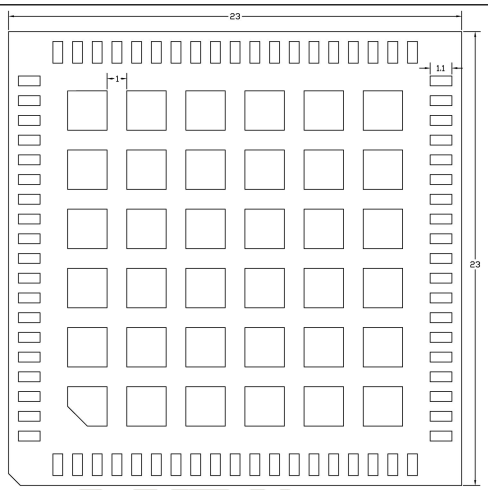
Symbol	Description	Min	Typ	MAX	Unit
F_{pcm_clk}	PCM_CLK frequency	64	-	2.048	kHz
Ts_{pcm_sync}	Setup time PCM_SYNC to PCM_CLK fall	0	-	-	ns
Th_{pcm_sync}	Hold time PCM_CLK fall to PCM_SYNC fall	150	-	-	ns
Td_{pcm_out}	Delay from PCM_CLK rise to PCM_OUT	0	-	150	ns
Ts_{pcm_in}	Setup time PCM_IN to PCM_CLK fall	0	-	-	ns
Th_{pcm_in}	Hold time PCM_IN after PCM_CLK fall	150	-	-	ns



Symbol	Description	Min	Typ	MAX	Unit
$F_{(pcm\_clk)}$	PCM_CLK frequency	64	-	2048	kHz
$Td_{(sync)}$	Delay from PCM_CLK rise to long SYNC	-10	-	50	ns
$Td_{(pcm\_out)}$	Delay from PCM_CLK rise to PCM_OUT	-10	-	50	ns
$Ts_{(pcm\_in)}$	Setup time PCM_IN to PCM_CLK fall	50	-	-	ns
$Th_{(pcm\_in)}$	Hold time PCM_IN after PCM_CLK fall	150	-	-	ns

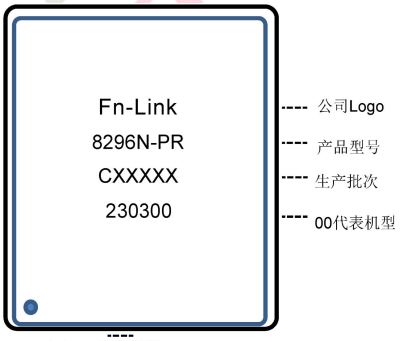
7. Size reference

7.1 Module Picture

L x W : 23 x 23 (+0.3/-0.1) mm 	
H: 5.6 (±0.2) mm	
Weight	3.56g

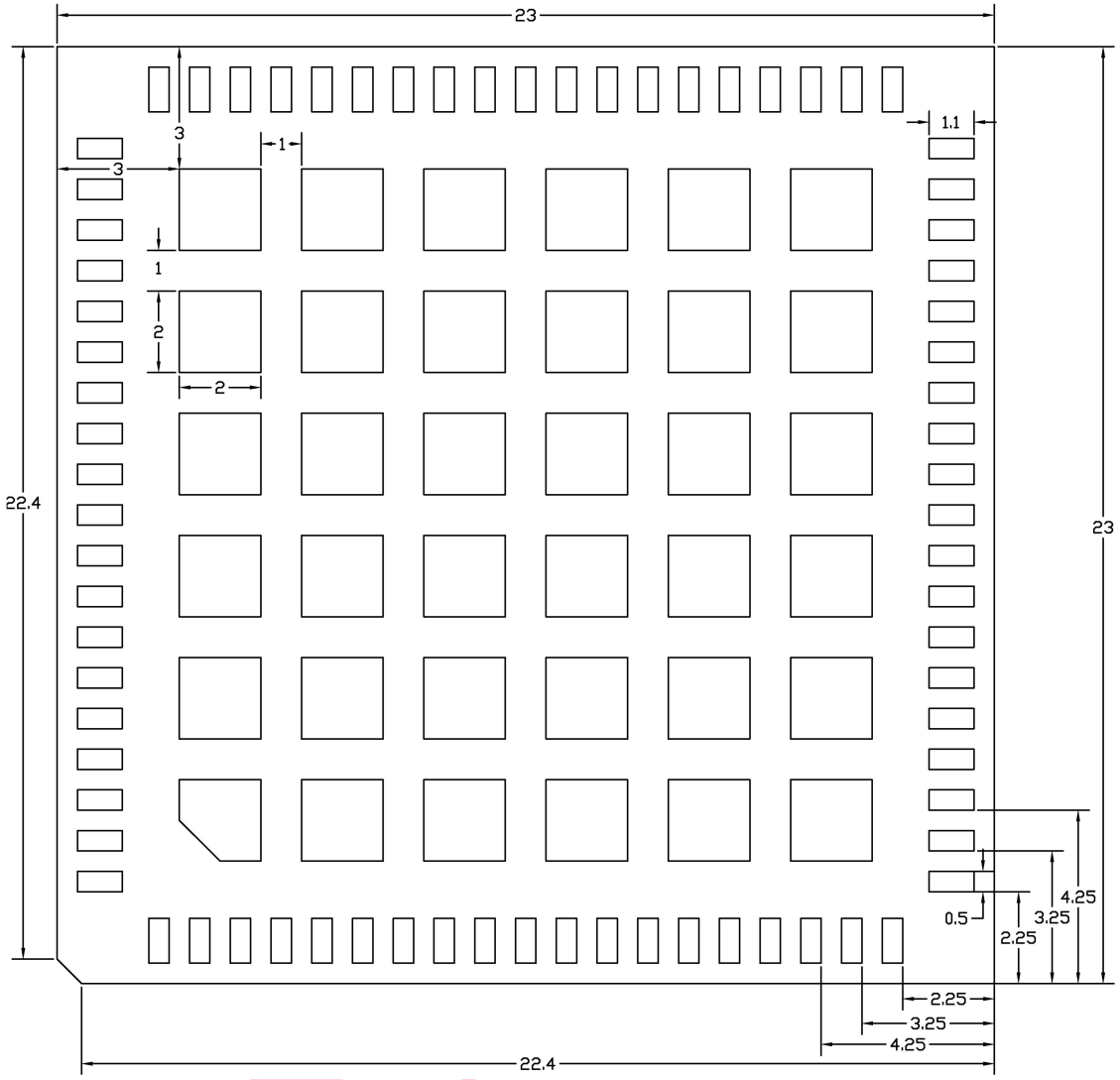
7.2 Marking Description

< TOP VIEW >



7.3 Physical Dimensions

<TOP View>



8. The Key Material List

Item	Part Name	Description	Manufacturer
1	Chipset	QCA-6696-0-NSP265-TR-03-0,265NSP	Qualcomm
2	PCB	8296N-PR IPC 三级 8L,23X23X1.2mm	XY-PCB,Brian-PCB,Truly,Sunlord
3	Crystal	2016 48MHz,9.9pF ±20ppm	TST,HOSONIC,TKD,ECEC,JWT
4	Shielding	8296N-PR shielding	信太,精力通,卓益
5	Diplexer	A-DP1608-R2455Z74771T	ACX, Glead, Walsin, Murata,FTR

9. Reference Design

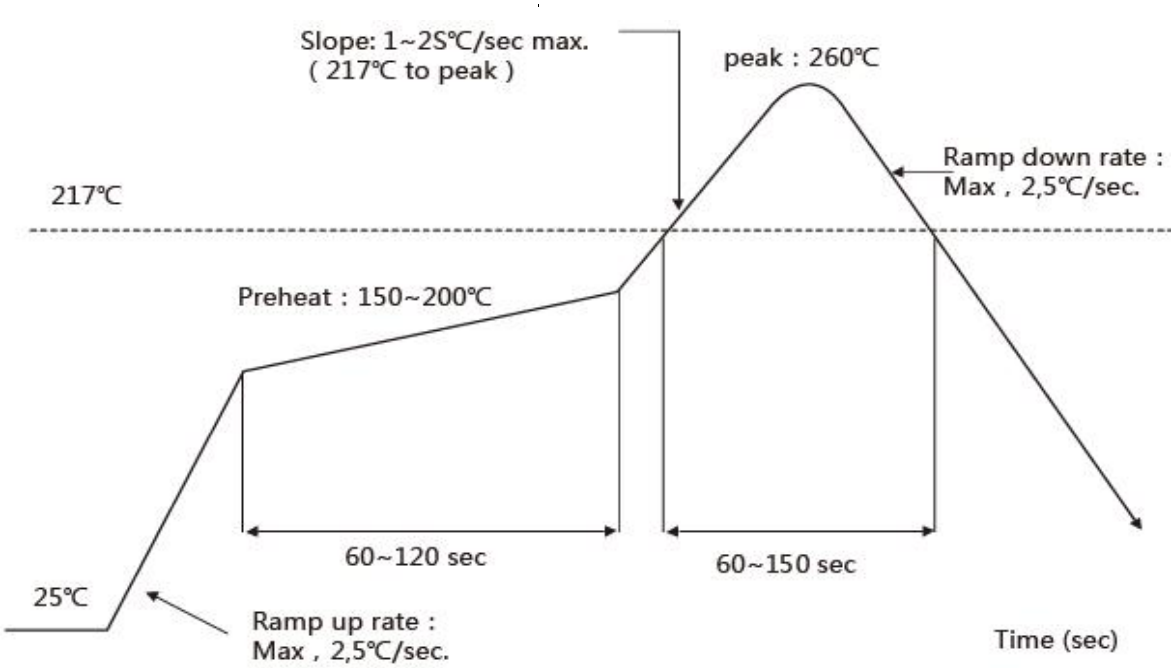
TBD

10. Recommended Reflow Profile

Referred to IPC/JEDEC standard.

Peak Temperature : <260°C

Number of Times : ≤2 times

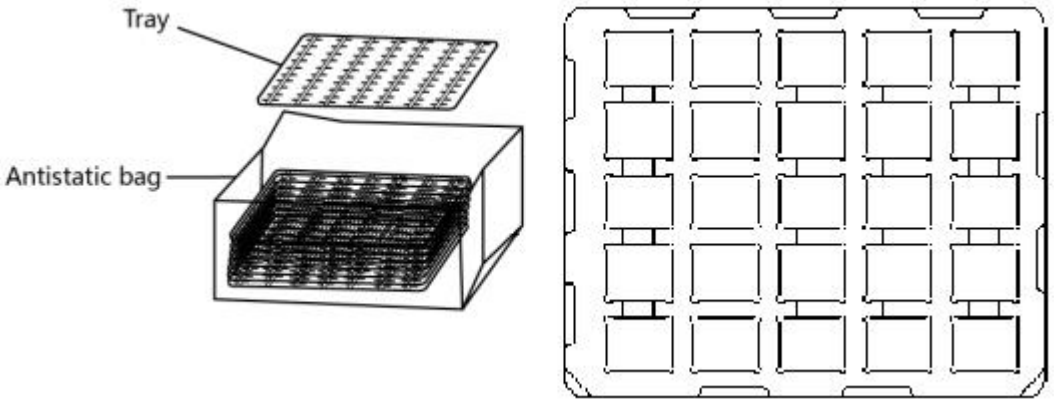


11. RoHS compliance

All hardware components are fully compliant with EU RoHS directive

12. Package

12.1 Tray



13. Moisture sensitivity

The Modules is a Moisture Sensitive Device level 3, in according with standard IPC/JEDEC J-STD-020, take care
all the relatives requirements for using this kind of components.
Moreover, the customer has to take care of the following conditions:

a) Calculated shelf life in sealed bag: 12 months at <40°C and <90% relative humidity (RH)

b) Environmental condition during the production: 30°C / 60% RH according to IPC/JEDEC J-STD-033A paragraph 5

c) The maximum time between the opening of the sealed bag and the reflow process must be 168 hours if condition

b) “IPC/JEDEC J-STD-033A paragraph 5.2” is respected

d) Baking is required if conditions b) or c) are not respected

e) Baking is required if the humidity indicator inside the bag indicates 10% RH or more