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Theory and Practice of Physical Design of VLSI Systems

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Workshop on the Theory and Practice of Physical Design of VLSI

Organizers: T. Lengauer, R. Möhring, B. Preas
September 2 - 6, 1991

The Workshop on the Theory and Practice of Physical Design of VLSI Systems intended to bring together practitioners and theoreticians that work in this important field of design automation. Physical design has experienced impressive development within the last decade. Driven by the explosive growth in the technology for manufacturing integrated circuits, combinatorial methods have been developed that aim at structuring and optimizing the process of physical design. Early on, it has become apparent that sophisticated mathematical techniques would have to be developed and applied in order to handle the range of complexity of the relevant optimization problems. Thus, activities have been spawned in a wide range of communities spanning the entire spectrum from theory to practice.

Driven by the demands of industrial applications, there has been a lot of research aimed at quick but (hopefully) effective solutions to the immediate design problems. Typically, such research involves the development of robust models that capture the characteristics of the application domain and the application of universal and well understood heuristic techniques of optimization. The validation of the research is done by benchmarking or similar experimental evidence of how well the approach fits the application.

Driven by the activities in the practical research communities, more mathematically oriented researchers that are more distant to the application have conducted research on the algorithmic engines that might be at the core of several families of optimization problems in physical design automation (placement, routing, compaction, cell generation etc.).

This workshop intended to enhance the communication between these two research communities. This is important such that practitioners become aware of the new optimization technology at hand and that theoreticians choose models and investigate questions that are relevant to practical applications. To our knowledge, this was the first workshop that was specifically aimed at bringing together theory and practice of physical design.

The lively and sometimes heated discussions and exchanges of ideas during the workshop gave evidence for the fact that both communities have to tell each other a lot and that there is need of more exchange between

them. The list of talks shows that a wide range of subjects and methods was covered. The list of attendees reflects the pluralistic character of the workshop. It was apparent that many attendees got substantially new impulses to motivate and critically evaluate their future research.

The excellent surroundings of the workshop at Schloß Dagstuhl provided an atmosphere that was conducive to frank personal interaction. The organizers wish to thank all those who helped make this workshop an interesting and successful research experience.

Monday, September 2, 1991

Morning Session: (Chair: T. Lengauer)

C. L. Liu:	Performance Driven Placement
J. Cong:	Performance Driven Global Routing
J. Frankle:	Integrating Path Analysis into a Partition, Place and Route System

Afternoon Session: (Chair: B. Preas)

E. Shragowitz:	Timing Constraints on Signal Propagation in VLSI
R. Nair:	Fallacies and Pitfalls in the Design of Performance Driven Layout Techniques

Evening Session:

Discussion:	Performance Driven Physical Design

Tuesday, September 3, 1991

Morning Session: (Chair: R. Otten)

G. Zimmermann:	Hierarchical Chip Planning
B. Preas:	Fully Automatic Layout of General Cell Circuits
I. G. Tollis:	Area Optimization of Slicing Floorplans in Parallel
R. Camposano:	Using Physical Design Information at Higher Levels

Afternoon Session: (Chair: M. Sarrafzadeh)

L. Schrijver:	Homotopic Routing
M. Kaufmann:	On Edge-Disjoint Paths in Planar Graphs
D. Wagner:	A New Approach to Knock-Knee Channel Routing

Evening Session:

Discussion:	The Interface between High-Level Synthesis and Physical Design

Wednesday, September 4, 1991

Morning Session: (Chair: R. Möhring)

B. Korte:	Balanced Clock Trees with Zero Skew
M. Jünger:	Quadratic $0-1$ Optimization and a Decomposition Approach for the Placement of Electrical Circuits
T. Lengauer:	Integer Programming Methods for Placement and Routing
A. Martin:	A Polyhedral Approach for VLSI Routing

Evening Session:

Discussion:	Open Problems

Thursday, September 5, 1991

Morning Session: (Chair: C. L. Liu)

T. C. Hu:	Traveling Salesman Problem from Theory To Practice
M. Sarrafzadeh:	The Crossing Distribution Problem
R. Kolla:	Performance Optimization of Combinational Circuits

Afternoon Session: (Chair: B. Korte)

R. Möhring:	The Mathematics of Gate Matrix Layout and PLA - Folding
D. F. Wong:	Pin Rearrangement Problems for Channel Routing
F. Wagner:	Modeling Hypergraphs by Graphs

Friday, September 6, 1991

Morning Session: (Chair: R. Nair)

G. Hotz:	Optimal Graph Embeddings
R. Rutenbar:	Techniques for Automated Layout of Full-Custom Analog Integrated Circuits
Discussion:	The Role of Models in Physical Design

Using Physical Design Information at Higher Levels

Raul Camposano
GMD, Sankt Augustin and Universität Paderborn, FRG

Although the use of physical design information (size, delay) is essential to take design decisions at higher levels, little is known on how to do this in a systematic way. This talk reviews different approaches that attempt to integrate physical design information into high-level synthesis, i.e. partitioning, estimation design and redesign in a closed loop, the use of module generators and of specialized layout. The shortcomings and achievements of these techniques are presented, stressing the present lack of satisfactory general methods and solutions.

Provably Good Performance Driven Global Routing

Jason Cong
Dept. of Computer Science
University of California, Los Angeles, USA

We propose a provably good performance-driven global routing algorithm based on the bounded-radius minimum spanning/Steiner tree formulation.

For any given value of a parameter ϵ, we can construct a routing tree with longest interconnection path length at most $(1+\epsilon)R$ and with cost at most $(1+2/\epsilon)cost(MST)$, where R is the radius of the net and $cost(MST)$ is the cost of a minimum spanning tree. The method can be generalized to steiner tree routing and routing with variable wire length bounds on different source-sink paths. Extensive simulation confirms that this approach works well for both cell-based and building-block design styles.

This is joint work with A. Kahng, G. Robbins, M. Sarrafzadeh and C.K. Wong.

Integrating Path Analysis with Physical Design

Jon Frankle
USA

Path analysis routines can lead physical design tools toward higher performance layouts. We repeatedly call upon these routines to transform a set of lower bounds $L(c)$ on connection delays into a set of upper bounds $U(c)$, such that meeting all the upper bounds would satisfy overall system timing.

A heuristic based on Youssef and Shragowitz (ICCAD '90) computes $U(c)$ for every connection c. Each $U(c)$ is initialized to $L(c)$. The following steps are then iterated:

Assuming connection delays $U(c)$, compute each $slack(c)$. ("Slack" is the difference between the earliest required and latest actual arrival times at the end of a connection. Slacks are computed by two linear-time waves, one in which actual times propagate forward, and one in which required times propagate backward.) Then increase $U(c)$ by a fraction $f(c)$ times $slack(c)$, where for example $f(c)$ equals 1 divided by the maximum number of connections on a path through c.

A router for Xilinx FPGA's was modified to route connections in order of increasing $U(c)$ and to meet their bounds, the bounds are then relaxed until all nets are routed. For a fixed placement, the system clock period of a standard benchmark, 'primary1', was reduced by 30%. (FPGA's offer greater potential improvement from routing than most technologies, because different routes pass through different numbers of switching elements).

Future work will integrate path analysis with initial min-cut placement and with technology mapping. A recurring goal will be to select upper bounds on connection delays which design tools have the best possible chance of achieving.

Optimal Graph Embeddings

Günter Hotz
Universität des Saarlandes, FRG

Graph embeddings, which in a certain sense are optimal, have to be considered in each system to support chip design. First we give some remarks about the design system in whose context our graph embedding problems have to be seen.

The chip design system CADIC has been developed in a project of "DFG Sonderforschungsbereich 124 VLSI Entwurfsmethoden und Parallelität" The design language is based on an algebraic calculus, whose objects are nets, rectangles with planar graphs hanging on the "pads" of the rectangle. There are two partial abutment operations. The algebra can be considered as a free bi-category ([Ho65,Mo88,KMO89]). Layouts are defined by algebraic expressions or recursive equations in this calculus. The solution of the recursive equations is found by iterating homomorphisms of the algebra into itself. By this the layout is defined up to homotopy. In the next step one has to specify a representative of the homotopy class. This is done in the system by a method based on a work of Leiserson and Pinter [LePi83]. The physical assignment has been described by R. Kolla in a former talk of this conference. By preserving homotopy in all stages of the design process, problems that arise in fulfilling constraints in the lower levels can easily be solved by changing the design in higher levels. One component of the system to compute a starting configuration for an iterative optimization of the placement and compaction will now be considered in more detail.

We generalize the rectangle to a convex region R. On the border of the region there are "pads", that means fixed points on which a planar embedded graph is hanging. Let G be this graph and χ be its embedding. We only consider embeddings such that the knots of G are mapped onto points within R and the edges onto lines. If s is an edge and $\chi(s)$ the embedding of s, then $|\chi(s)|$ is the Euclidean length of $\chi(s)$. We consider mappings $f : R^+ \to R^+$, which are two times differentiable, where $f''(x) > 0$ and $f'(0) = 0$. We define

$$|\chi|_f = \sum_s f(|\chi(s)|)$$

as the cost function of the embedding and wish to minimize χ relative to this measure. Under the assumptions on f there exists exactly one optimal solution χ_f with $|\chi_f|_f \leq |\chi|_f$ for all embeddings χ. It holds the theorem [BeHo87]: If there exists one planar embedding of G, then χ_f is planar, too. This means that, on fixing crossing overs of a not planar embedding, this optimization preserves homotopy. The proof is essential by reduction on a generalization of the monodromy theorem of "folding free covering spaces" [BeHo90]. The efficient computation of χ_f has been considered by H.G. Osthof in his Ph.D. thesis. The case $f(x) = x^p$ and $p \to \infty$ was considered by B. Becker and H.G. Osthof. This case promises especially good initial configurations for placement. The computation of χ_f is done in the manner of multigrid methods. The necessary hierarchical decomposition is given in a natural way by the input specification of the layout. In addition H.G. Osthof

studied the case $p \to 1$. This case led him to a very efficient algorithm to compute min-cuts of graphs with one source, one sink, and positive weights. The capacity in this case is just

$$|\chi|_1 = \lim_{p \to 1} |\chi_{x^p}|.$$

The running time of this algorithm is $e \log e$ where e is the number of edges. The computation starts with an approximation of χ_{x^2}. The result is experimental. It has been tested on 200,000 examples. In each case the result was exact.

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Traveling Salesmans Problem from Theory to Practice

T. C. Hu

Computer Science and Engineering Department

University of CA, San Diego, USA

Given a signal net in the shape of a free tree. The net has to be tested for connections. Normally, we could put one probe at one of the leaves and move the other probe to all other leaves of the tree (A traveling salesmans problem

for $n-1$ cities). But we can do better by moving two probes simultaneously (only $n/2$ moves instead of $n-1$). Many theoretical as well as practical problems arise. This part of the talk is based on

IEEE International ASIC Conference, Sept. 1991, by S.Z. Yao, N.C. Chou, C.K. Cheng and T.C. Hu

Two other topics will also be discussed:

(i) Ancestor Tree for Arbitrary-Function Multi-terminal Cuts. Proceedings on Integer Programming and Combinatorial Optimization edited by R. Kannan and W. R. Pulleyblank, Univ. of Waterloo Press, 1990, pp. 115–128, by C K. Cheng and T. C. Hu. The paper generalized the Gomory-Hu cut tree of 1961 from min-cuts to cuts of arbitrary cost functions.

(ii) Max Folding, a generalization of Max Matching. (Yet to be published) A new class of combinational problem can be formulated as:

Given a red graph with directed and undirected edges, how to add a maximal number of directed green edges such that the in-degree and out-degree of the green graph at every node is at most one, and there exists no alternating cycle formed by the red and green edges. Based on early works by T. C. Hu and S. Kuo. Generalization by T. C. Hu, K. Moerden and David Morgathala.

Quadratic $0-1$ Optimization and a Decomposition Approach for the Placement of Electrical Circuits

Michael Jünger
Universität Köln, FRG

We show how the placement problem can be modeled as a quadratic $0-1$ programming problem with linear constraints. Our complexity analysis shows that various interesting variants of this problem are NP-hard, and there are no ϵ-approximative algorithms for them, unless $P = NP$.

We then present some heuristics inspired by a graph theoretic formulation of the problem. Finally, we point out implementation details and present computational results which show that our approach is competitive

with placement software used in industry. We point out, that this is largely due to a new decomposition approach which overcomes certain problems encountered in min-cut placement.

This talk is based on joint work with A. Martin, G. Reinelt and R. Weismantel.

On Edge-Disjoint Paths in Planar Graphs

Michael Kaufmann
MPI Informatik, Saarbrücken, FRG

An efficient algorithm for the edge-disjoint paths problem in planar graphs is presented in this talk. Using Frederikson's algorithm on decompositions of planar graphs we improve the best bound for the running time of $O(n^2)$ (Becker/Mehlhorn, Matsumoto/Nishizeki/Saito) for the edge-disjoint paths problem to $O(n^{5/3}(\log\log n)^{1/3})$.

Performance Optimization of Combinational Circuits

Rainer Kolla
Universität Bonn, FRG

In this talk we consider the following problem:

"Given a combinational circuit and a set of different cells with different area and delay characteristics. Find an assignment of cells to the gates which minimizes the time performance under an area constraint."

In general this problem is even in the unconstrained case an NP-complete optimization problem. We present efficient pseudopolynomial time algorithms for trees and show how to use them as iterative speed-up heuristics for general combinational logic. To this end we point out the application of these algorithmic techniques for the library mapping problem and we discuss general questions arising from the relation of performance optimization and physical design, in particular placement and routing.

Balanced Clock Trees with Zero Skew

Bernhard Korte
Universität Bonn, FRG

As VLSI-chips get faster and the cycle time gets smaller, the construction of an optimally balanced clock tree plays an ever important role. Performance driven placement tries to maximize the slack at the latches while planning the combinational logic. However, with very fast CMOS or bipolar technology it is even more important to control the travel time of the clock signal itself. The clock signal is generated or enters the chip at a certain point. From this point one has to construct a (clock) tree such that all latches are leaves. The tree should be built up in such a way that the clock signal arrives at each latch exactly at the same time.

We call a tree $T = (V, E)$ with root $r \in V$ balanced if all paths from the root to a leave have the same length. It is called totally balanced if it is balanced and moreover each subtree of the same level has the same total length.

We give different algorithms for constructing totally balanced trees. The most promising one is a bottom-up strategy which uses bottleneck matchings to build up subtrees successively which are combined by further matchings over drivers to a totally balanced tree. We show that our algorithms construct trees of length $O(\sqrt{n})$ or $O(\sqrt{n \log n})$ depending on the matching strategy. Note that an optimal Steiner tree for n points uniformly distributed in the unit square already has length $O(\sqrt{n})$. Even if one takes into consideration node weights (pin capacitance) we prove that our best algorithm generates totally balanced trees of length $O(\sqrt{n})$.

The algorithm has been designed for very large CMOS chips with about 8000 latches and up to twelve different clocks on the same chip. Its results are used in practical chip production.

This is joint work with Karsten Munss.

Integer Programming Methods for Placement and Routing

Thomas Lengauer
Universität Paderborn, FRG

We formulate several of the variants of the global routing problem that occur in practice as integer programs. After a review of previously published techniques, we propose a Lagrangian relaxation of these integer programs

and discuss its merits. Finally, we extend the integer programs to handle the placement and routing problem simultaneously and introduce an appropriate Lagrangian relaxation. This research is aimed at providing a general algorithmic framework based on proven integer programming methods that solves placement and routing problems in a generic level that largely abstracts from details of particular fabrication technologies.

This research is joint with Martin Lügering.

Performance Driven Placement

C. L. Liu
Dept. of Computer Science
University of Illinois at Urbane-Champaign, USA

A new performance driven placement algorithm has been proposed. In the algorithm, we just use a convex programming algorithm to compute a set of upper bounds on the net wire lengths. We then use a modified min-cut algorithm to generate a placement with the objective of minimizing the number of those nets, the wire lengths of which exceed their corresponding bounds. We then address the situation in which the modified min-cut algorithm fails to generate a placement that satisfies the timing requirements. We employ an iterative approach to modify the set of upper bounds making use of the information from previous placements.

A Polyhedral Approach for VLSI Routing

Alexander Martin
ZIB, Berlin, USA

From a graph-theoretical point of view the routing problem in VLSI-Design can be described as the problem of packing Steiner trees in special graphs. We consider this problem from a polyhedral point of view and define a polyhedron P whose vertices are in a one to one correspondence to the solutions in the graph. Next we describe a lot of valid inequalities for P, which define facets if the underlying graph is complete and the terminal sets are disjoint. We develop a cutting plane algorithm which includes separation algorithms for two classes of valid inequalities and a polynomial heuristic which exploits the information given by the LP solutions. Finally, we present preliminary results obtained for switchbox problems.

This is joint work with M. Grötschel and R. Weismantel.

The Mathematics of Gate Matrix Layout and PLA - Folding

Rolf Möhring
Technische Universität Berlin, FRG

We give a survey on mathematical models occurring in linear VLSI layout architectures such as gate matrix layout, folding of programmable logic arrays and Weinberger arrays. These include a variety of mostly independently investigated graph problems such as augmentation of a given graph to an interval graph with small clique size, node search graphs, matching problems with side constraints and other. We discuss implication of graph theoretic results for the VLSI layout problems and survey new research directions. New results presented include NP-hardness of gate matrix layout on chordal graphs, efficient algorithms for trees, cographs and certain chordal graphs, Lagrangian relaxation and approximation algorithms based on on-line interval graph augmentation.

Fallacies and Pitfalls in the Design of Performance-Driven Layout Techniques

Ravi Nair
IBM T. J. Watson Research Center
Yorktown Heights, New York, USA

This talk lists a number of common fallacies and pitfalls in the design of new techniques for performance-driven layout of integrated circuit chips. Chief among them are:

- Relying on placement without adequate consideration of wiring
- Ignoring logic options to overcome performance inadequacies.
- Using path slacks as weights on nets
- Inadequate modeling of net characteristics
- Using simplified cost functions for an optimization problem formulation
- Treating layout as a "minimization" rather than an "allocation" problem

Fully Automatic Layout of General Cell Circuits

Bryan Preas
Xerox Parc, USA

Currently, general cell layout is a heavy weight process. In order to produce good layouts, designers must consider the physical alternatives in the behavioral and logic design stages and must interact closely with the general cell layout programs. In contrast, modern standard cell layout is nearly automatic. This difference arises for two reasons. General cell layout has:

1. much higher topological complexity. Standard cell layout imposes a structure of rows of fixed size, uniform height cells. This structure is exploited in the standard cell layout process.

2. many more degrees of freedom. The general cells within a circuit may have many physical implementations each with different sizes, shapes and pin configurations. These physical alternatives must be considered in the general cell layout process.

This presentation addresses these issues and describes a prototype system that can automaticly lay out general cell circuits.

In order to automate the general cell layout process, we must develop methods to tradeoff the interface characteristics of the cells (size, shape and pin configuration) against the constraints of the composite design.

Our approach uses a bottom up phase to generate shape functions (minimum height of a cell as a function of its width) and wire length functions (wire length as a function of cell area) of the leaf cells and intermediate cells that describe the many layout alternatives. This is followed by a top down planning phase (cast as an A* search) to select the best of the layout alternatives for the cells in combination with the overall layout. This phase incorporates global wiring and pin position constraints. These bottom up and top down phases are repeated until all conflicting constraints have been resolved and the planning errors have been reduced to an acceptable level. The layout can then be generated in the normal bottom up fashion.

Much work remains to be done but early results indicate that it is possible to produce competitive general cell layouts completely automatically.

This is joint work with Massoud Pedram.

Techniques for Automated Layout of Full-Custom Analog Integrated Circuits

Rob A. Rutenbar
Carnegie Mellon University, USA

We describe new algorithms for device-level placement and routing of full-custom analog cells. A block place and route style derived from macrocell digital ICs has recently emerged as a viable layout methodology for custom analog cells. In this "macrocell" style, parameterized module generators produce geometry for individual devices, a placer arranges these devices and a router embeds the nets. Analog layout tools that merely apply known digital macrocell techniques fall far short of achieving the density and performance of hand-crafted cells. Our tools, called KOAN and ANAGRAM-II differ from existing approaches in that they rely on algorithms to find critical device layout optimizations, instead of a large library of fixed-topology device generators.

New algorithms implemented in KOAN handle complex layout symmetries, dynamic merging and abutment of devices, and generation of wells and bulk contacts. New routing algorithms implemented in ANAGRAM II handle fully symmetric wiring of differential signals, crosstalk avoidance, over-the-device wiring, and arbitrary design rules. Several examples of CMOS and BICMOS analog layouts produced by the tools will be presented. Results suggest these layouts are competitive in density and performance with handcrafted layouts.

In the last part of the talk, we describe very recent work in simultaneous device placement and routing that addresses difficulties with our sequential place-then-route style. We introduce a new detailed routing abstraction called a "k-bend net" that limits the complexity of an individual net, but allows both nets and devices to be treated as placeable, malleable objects in a common simulated annealing framework. Layouts in which the critical interacting nets are simultaneously embedded during device placement prove to be superior in terms of performance-limiting crosstalk violations, to sequentially placed and routed nets.

The Crossing Distribution Problem

Majid Sarrafzadeh
Dept. of EE and CS
Northwestern University, Evanston, USA

We study the problem of distributing the set of crossings in a global routing: aim is to minimize the total number of crossings and to ensure at most q_i crossings in the region i. A polynomial time algorithm is presented.

Homotopic Routing

Alexander Schrijver
CWI, Amsterdam, The Netherlands

We describe a polynomial-time algorithm for the local routing of VLSI-wires, given the homotopies of the wires. The method is based on solving a certain system of linear inequalities in integer. The method also gives us, if no solution exists, a cut criterion that determines where the bottleneck is, so that the global routing phase can be adapted. We also give an extension to trees and to the directed case.

Timing Constraints on Signal Propagation in VLSI

Eugene Shragowitz
University of Minnesota, USA

Timing Constraints for all nets are derived from the information on the clock cycles, switching delays of cells and electrical characteristics of circuits. Maximal allowable net delay is determined as a minimum of all delays on this net for each path traversing the net. Distribution of delays on nets for each path is performed in accordance to electrical characteristics. An asymptotically optimal algorithm is proposed for the problem and convergence theorems are proven. A description of the algorithm is accompanied by experimental results, which demonstrate the effect of these constraints on net length.

New characteristic functions are introduced for identification of critical paths and ranking of paths according to their criticality. Methods of computations and experimental data are discussed.

Area Optimization of Slicing Floorplans in Parallel

I. G. Tollis
Computer Science Department, Univ. of Texas at Dallas, USA

We present parallel algorithms for finding the optimal implementations for the modules of a slicing floorplan. The first algorithm runs in $O(n)$ time and requires $O(n)$ processors, where n is the number of modules. It is based on a new $O(n^2)$ sequential algorithm for solving the above problem. The second algorithm runs in $O(n)$ time using $O(\log n)$ processors, if the slicing tree has $O(\log n)$ height. Our algorithms do not need shared memory and can be implemented in a distributed system.

This is joint work with C.-H. Chen

A New Approach to Knock-Knee Channel Routing

Dorothea Wagner
Technische Universität Berlin, FRG

We present a new algorithm for dense two-terminal channel routing problems that determines layouts with the following properties:

- they are area-optimal
- they have minimum total wire length
- they have nearly minimal number of bends.

For a modified version of the algorithm we can prove that the layouts are again area-optimal

- with a nearly minimal number of bends and
- only a nearly minimum total wire length

but in addition are three-layer wirable.

The running time of both algorithms is linear in the number of nets.

Modelling Hypergraphs by Graphs

Frank Wagner
Freie Universität Berlin, FRG

In the most general setting a layout problem is modelled as a hypergraph embedding problem. Then min-cut algorithms are applied as part of a divide-and-conquer strategy.

Typically the min-cut algorithms work better/only for ordinary graphs. So it would be nice to find a (weighted) graph, possibly with additional dummy vertices, that has the same min-cut properties as a hyperedge, i.e. every min-cut should have the same cost. We show that such a perfect simulation does not exist. It is a first step in the direction of proving a conjecture by Lengauer, saying that there is no better simulation than taking an uniformly weighted clique.

Pin Rearrangement Problems for Channel Routing

D.F. Wong
Department of Computer Sciences
University of Texas at Austin, U.S.A.

In this talk we consider the problem of rearranging pins in a channel, subject to various types of constraints, to minimize channel density. We first consider pin rearrangement subject to position constraints, order constraints and separation constraints. The position constraints are given by associating with each pin a set of allowable positions. The order constraints specify the relative orderings of the pins on the top and the bottom of the channel by a pair of partially ordered sets. The separation constraints require the distance between each pair of consecutive pins to be within a certain range. We show that the problem is NP-hard in general and present polynomial optimal algorithms for an important case in which the order constraints are given by a pair of linearly ordered sets (i.e. relative orderings of the pins on the top and the bottom of the channels are fixed). We then extend the algorithm to solve the case where pin rearranging constraints are given by movable modules as well as movable pins within the modules. Finally we also consider the case where each module or submodule can be flipped and present a polynomial time optimal algorithm to solve the problem.

Hierarchical Chip Planning

Gerhard Zimmermann
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The goal of the presented research was the demonstration that very large VLSI chip complexities of more than one million cells can be handled with a hierarchical layout synthesis system. For example, with three levels of a ports hierarchy and 100, 100 and 1000 cells per level respectively, the product of ten million cells is feasible. This is more than current technology can handle and is aimed at the future.

The heart of a top-down design methodology is chip planning. In general, four design styles for the placement and global routes of cells with different shapes are considered. The first is the bottom-up placement of fixed macro cells (general cells). More flexibility is achieved by a set of layout alternatives (multi-macro cells) for each cell type. In contrast to the bottom-up strategies top-down styles require flexible cells that are represented by shape functions with tolerances. This third style offers more flexibility and a larger design space. An intermediate method is a middle-out strategy. First floorplans are generated at an intermediate level that represent semi-flexible cells. These can be incorporated in the floorplanning of the next higher level.

Our chip planning method combines all four design styles because in reality there is always a mixture of fixed and flexible cells and each method has advantages and disadvantages. We try to reduce the disadvantage of the estimation tolerances for the shape functions of flexible cells by 3-phase chip-planning. At each planning level constraints are passed up (after phase 1) in the hierarchy and down (after phase 2). In phase 1, the topology, geometry, and global routing is determined, in phase 2, after receiving new constraints from the level above, the geometry is corrected, and global routing is repeated. In phase 3, after receiving new constraints from below, geometry and global routing are corrected. Thus we go up and down in a yo-yo manner and connect and refine all levels of the hierarchy.

This method has been implemented in our PLAYOUT system and used for a 280, 000 standard cell example with 12 large macro cells. The complete design took about 6 months including high-level synthesis for the structural design and chip assembly to measure the results of chip planning. Two to four "designers" worked in parallel. The result was a 10×10 cm chip layout using a 1.25μ industrial standard cell library.

The results are preliminary, because we found many places where tools or parameter settings have to be improved. But we also found an average of 4% area improvement of 3-phase chip-planning over 1-phase planning using the same set of tools. These results will be verified by more examples. In summary we have shown that very complex VLSI layout problems of the future can be handled using a multi-level top-down design method.

This is joint work with Bernd Schürmann.

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