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Semitracks Monthly Newsletter

Chemical Vapor Deposition—Epitaxy Part 2

By Christopher Henderson

In this section we will continue our discussion on chemical vapor deposition for epitaxial growth.

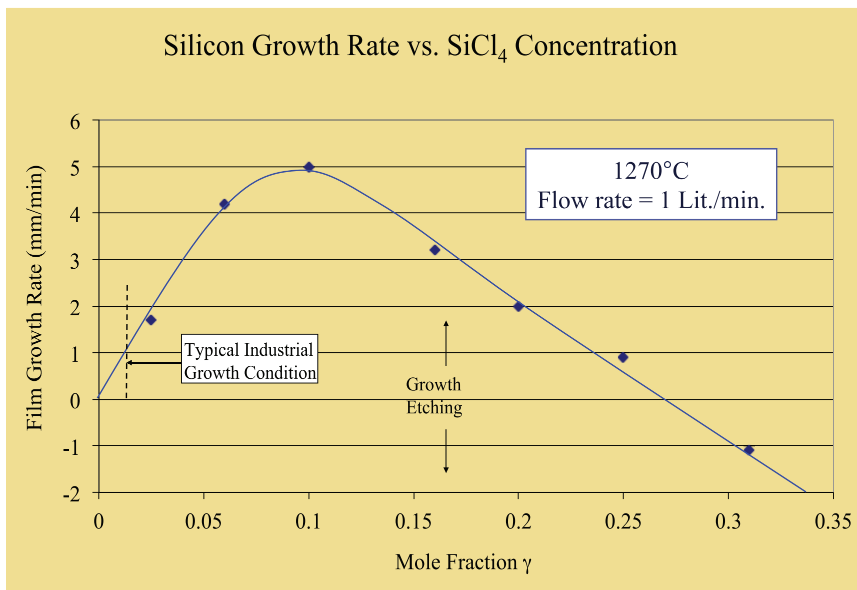

Figure 10. Silicon growth rate as a function of SiCi4 concentration.

The growth rate is also affected by the concentration of the gas. Figure 10 shows the film growth rate as a function of the mole fraction of the gas silicon tetrachloride. At 1270°C and a flow rate of 1 liter per minute, the growth is positive at lower mole fraction

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ratios, while it turns negative at ratios above 0.25. When the growth rate turns negative, etching is occurring.

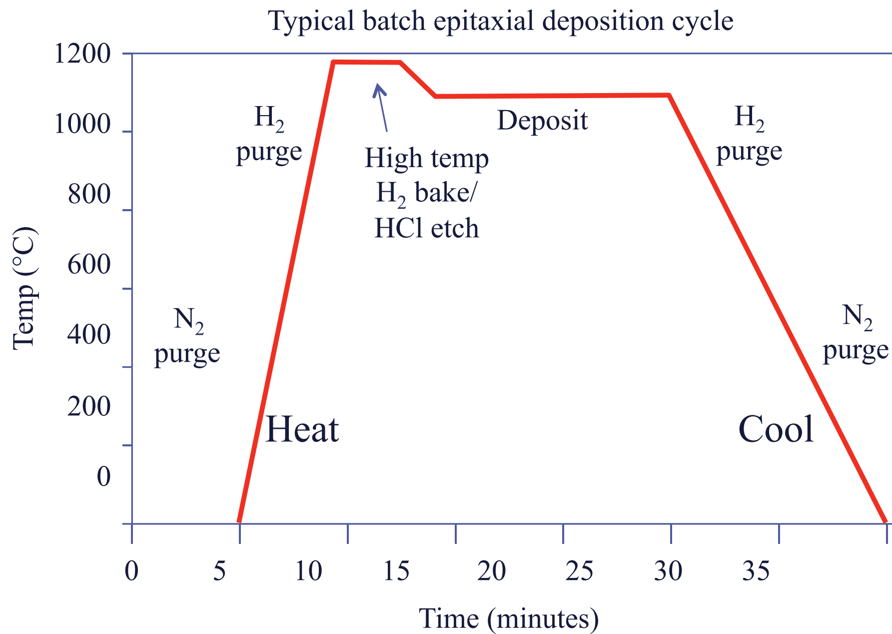


Figure 11. Epi deposition process.

If we look at an overall time-temperature profile for an epitaxial deposition process, it looks something like this graph shown in Figure 11. We begin with a nitrogen purge, followed by a ramp up in the temperature. The high temperature hydrogen bake occurs first, to volatilize the surface oxide layer. We follow this with the deposition process for 10 to 15 minutes. Finally we follow the deposition with a cool-down phase. During this phase we include a hydrogen purge and a nitrogen purge to keep the surface free from defects and a native oxide.

Let's turn our attention now to the doping portion of the process. One can dope the epitaxial layer by introducing gases containing the appropriate impurities. For example, one can use phosphine to add phosphorus doping, arsine to add arsenic doping, or diborane to add boron doping. The doping level is very critical, and process engineers must control this very tightly. For better process control the dopant gases are highly diluted in hydrogen. One must be extremely careful with these gases as they are both toxic and flammable. These gases all require special handling and storage procedures.

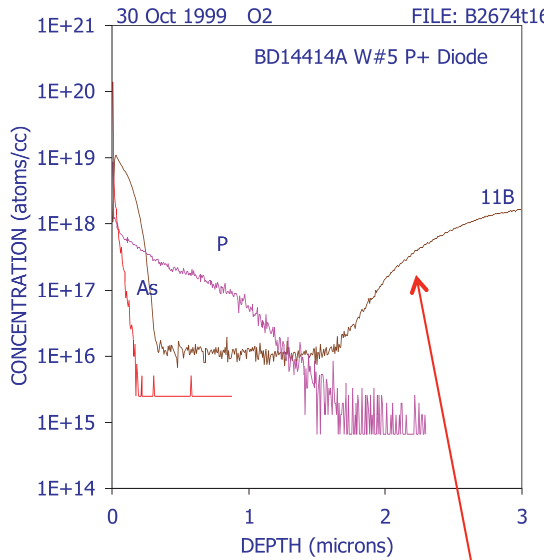


Figure 12. Epi deposition process—doping.

A side effect of the epitaxial process is autodoping. This occurs during the deposition by two methods. One is out-diffusion from the substrate. The high temperatures allow the higher concentration of dopants in the substrate to diffuse into the epitaxial layer. A second, more subtle process occurs when dopants out-diffuse from the back of the wafer, mix into the gas stream and become incorporated into the growing film. Both out-diffusion and vapor phase autodoping will produce a transition layer, as the doping concentration morphs into a gradient at the epi-layer/substrate boundary rather than a step function. Vapor phase autodoping can also produce an autodoping tail, which can be more difficult to detect and characterize.

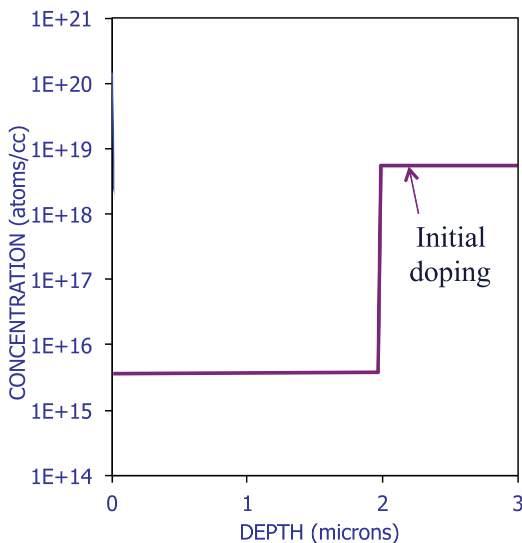


Figure 13.

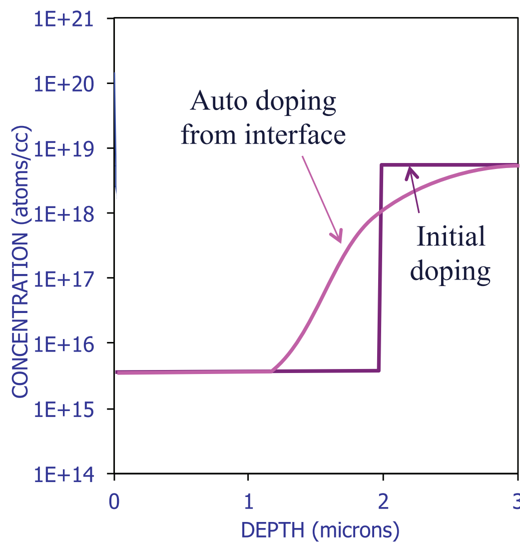


Figure 14.

If we look at the autodoping process from a graphic standpoint, the initial doping might look something like Figure 13. After the epitaxial growth process, the auto-doping from the interface will produce a profile that looks something like Figure 14.

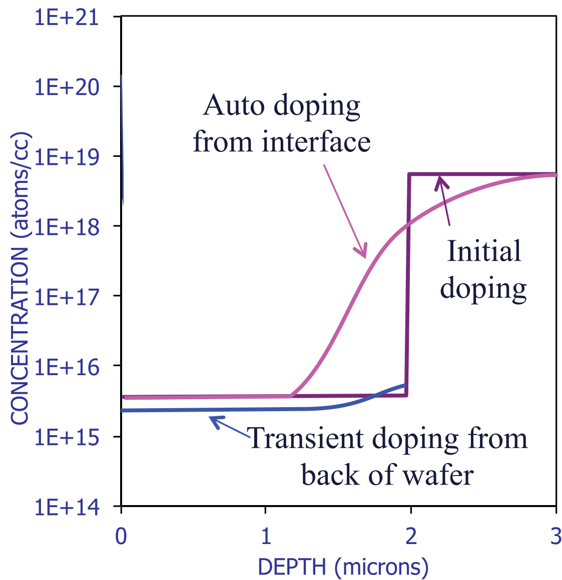


Figure 15.

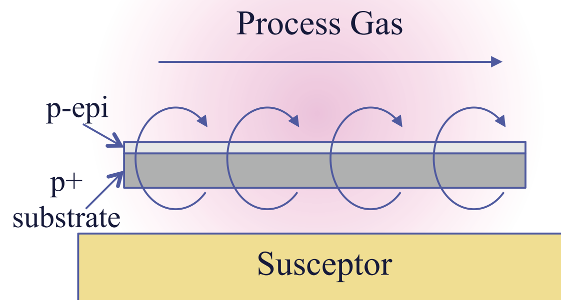
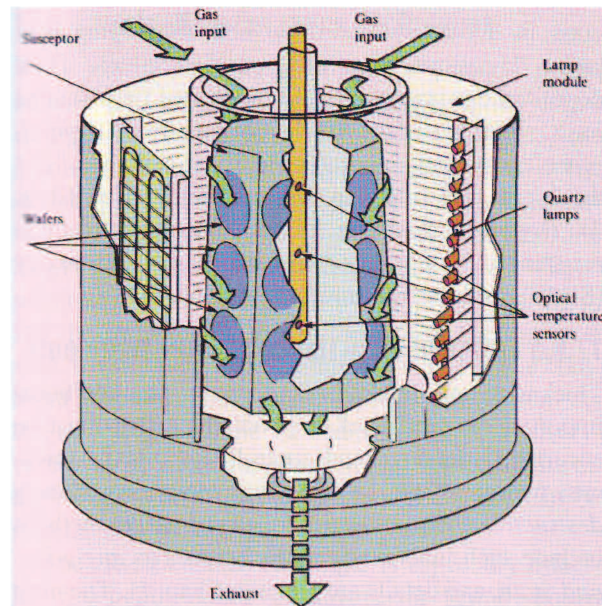


Figure 16.

The transient doping from the back of the wafer will produce a lower concentration gradient that looks something like Figure 15. Figure 16 shows how back surface autodoping can occur.

So how do we control passive doping? There are several methods. One method is to move to single wafer processing. This dramatically reduces backside autodoping issues. Another method is to lower the temperature. This will reduce diffusion effects. For example, one can use silane at a lower temperature instead of Trichlorosilane, which requires a much higher temperature. One can also deposit or grow a capping layer on the backside to help prevent backside autodoping. An edge seal wafer on the susceptor will also help, as it prevents vapor flow from the backside to the frontside. Finally, a modified prebake cycle can help. Using hydrochloric acid and an n-type dopant gas can help limit autodoping effects.

Once we deposit the epitaxial layer, we will want to ensure it conforms to our specifications. There are several methods to characterize these epi films. For film thickness there are two methods: infrared reflectance and Fourier Transform Infrared Spectroscopy. These are two infrared techniques. In the reflectance technique, we analyze the interference between the IR light reflected at the air-epi interface and the epi-substrate interface. This works well if there are large differences in the doping levels, as higher doping levels more strongly absorb the light. FTIR works in a similar manner, although it can also be done in a transmission mode. To detect crystal defects and particles in a non-destructive manner, one can use a wafer surface scanner. One can also perform defect decoration using certain wet chemical etches followed by an inspection. This is destructive, however. One can check resistivity using a four-point probe measurement, and one can check the dopant profile using secondary ion mass spectroscopy, time-of-flight secondary ion mass spectroscopy, and spreading resistance probe measurements.



Schematic of a radiantly-heated, cylindrical-type epitaxial reactor (courtesy Applied Materials)

Figure 17. Batch reactor.

Let's move on and discuss the equipment used for epitaxial deposition. Historically, process engineers used batch reactors to deposit epitaxial layers. This has the advantage of being a higher throughput process, but there are a number of drawbacks. The popular design was the barrel reactor (Figure 17). The susceptor was a silicon carbide-coated graphite with a hexagonal cross-section. The unit then rotated to improve wafer-to-wafer thickness uniformity. The system heated the wafers using an array of water-cooled quartz lamps. The system injected the reactant gases at top of chamber, and exhausted them at the bottom. These systems could operate at atmospheric or reduced pressure, and the system held the wafers in a vertical orientation to minimize particle contamination. These systems have since been replaced by single wafer reactors.

Today, process engineers perform single wafer deposition. These deposition chambers are constructed of fused silica. The system heats the wafer from the front and back by quartz infrared lamps, which is a fast, controlled ramp-up to the process temperature. The pre-mixed gases flow into the chamber, across the wafer, and out the exhaust system. The system continuously rotates the wafer to minimize non-uniformities from temperature and gas flow variations. These systems use extensive cooling to keep the chamber wall temperature below 600°C. One can perform deposition at atmospheric or reduced pressure, and when the deposition process completes, the system cools the wafer to ~750°C, and then moves it into a cool-down chamber to complete the cooling process. There are many advantages over batch processing tools, including: higher growth rates, better uniformity and repeatability for both thickness and dopant concentration, higher reliability, and better economy for large wafers.

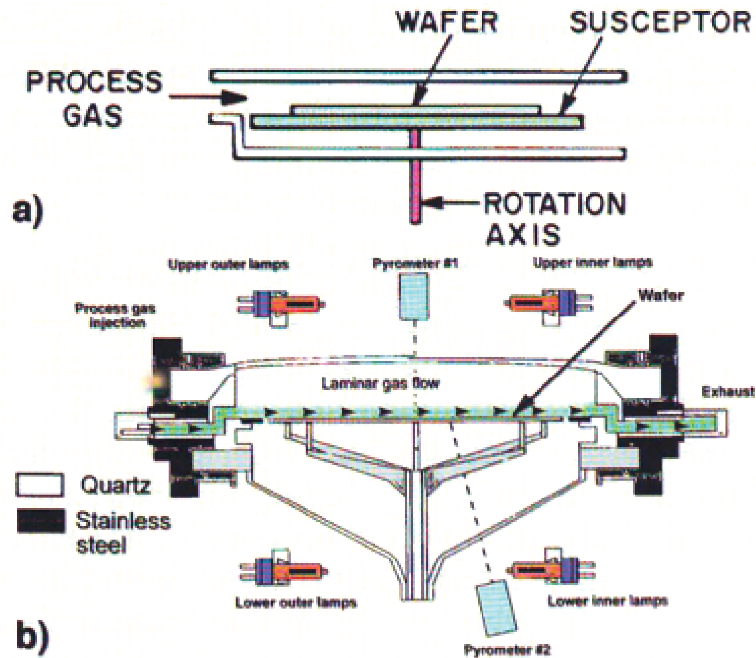
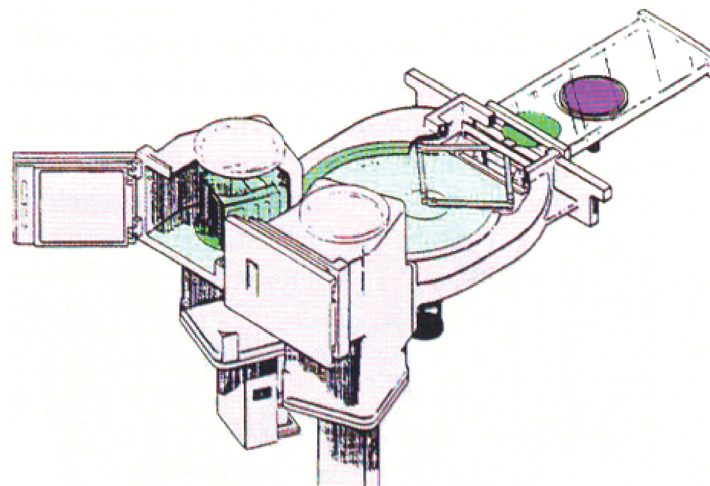


Figure 18

Figure 18 shows cross-sections of a single wafer epitaxial reactor. The wafer sits on the susceptor during the deposition process. Gases flow from left to right in a laminar flow regime in this system. The heating lamps heat up the chamber and wafer, and the two pyrometers measure front and backside temperatures on the wafer.



Perspective drawing of a commercial single-wafer epitaxial reactor (courtesy ASM International)

Figure 19

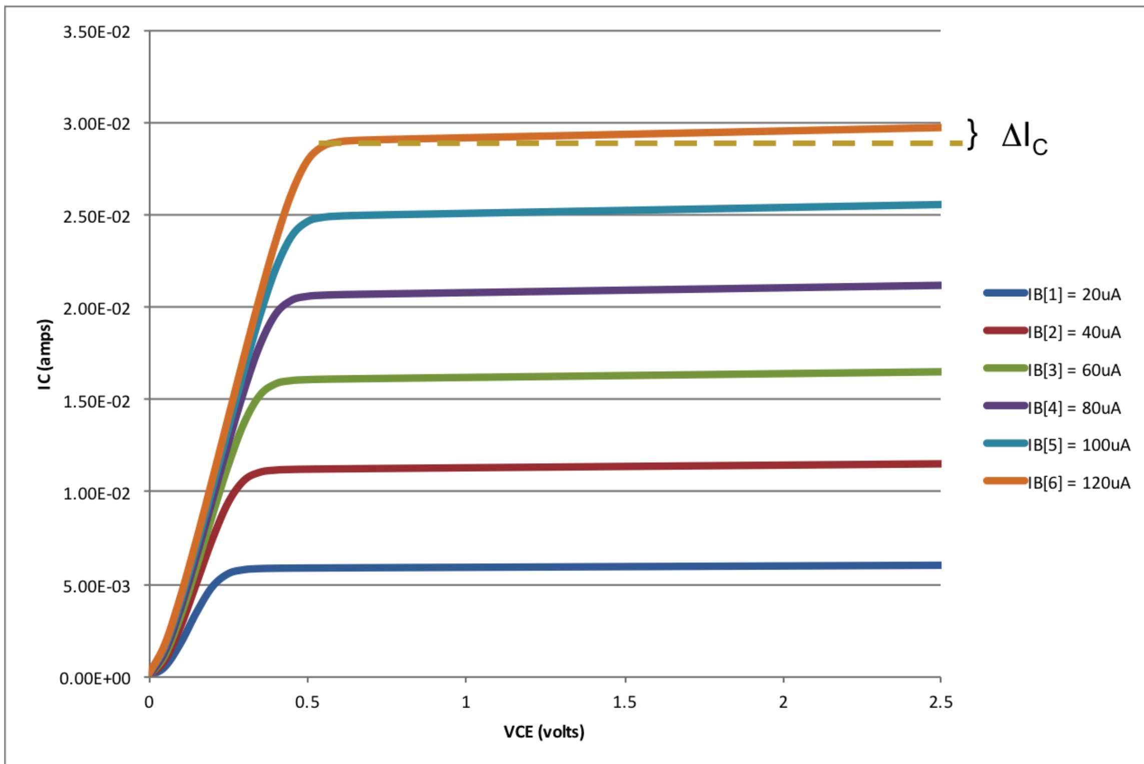
Figure 19 shows a single wafer system from a different perspective. The load lock appears at the upper right, and the input and exhaust systems appear at the left in this image.

In conclusion, chemical vapor deposition is a common process for epitaxial growth on wafers. Process engineers use CVD for both CMOS and Bipolar/BiCMOS processes. We described the basic reaction process, which follows the Deal-Grove model. The basic sequence for epitaxial growth is a nitrogen purge, followed by a heat cycle, a pre-bake in hydrogen to remove the native oxide layer, the deposition itself, a cool down step, and a final purge in nitrogen. Last, we described the two equipment configurations. There are both batch and single wafer configurations. Process engineers use single wafer systems today, as they provide better control and uniformity.

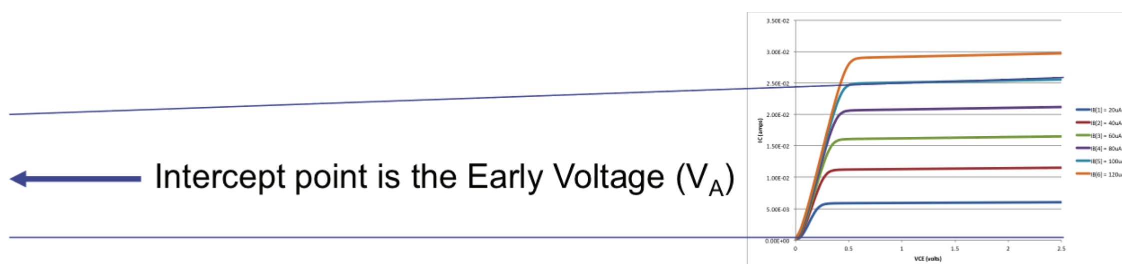
Technical Tidbit

Early Voltage (Early Effect)

The Early Voltage , or Early Effect, is named for James Early, who discovered the phenomenon in 1952.



In an NPN on PNP bipolar junction transistor, the collector-base depletion region widens as the collector-base voltage increases. Although the base region is usually somewhat more heavily doped than the collector, it is also very thin. Therefore as the depletion region widens, it shortens the undepleted (or “quasineutral”) base width. A shorter base reduces the time carriers require to cross, thus reducing recombination. This reduces base current and in turn increases beta. This phenomenon is called the Early Effect. Most Bipolar Junction Transistors use VA to define the Early voltage (typically 15 V to 150 V; smaller for smaller devices).



While this effect is not usually a significant issue for logic circuits, it can be a large issue for analog circuits. In an analog circuit, one requires consistent and stable values, sometimes over a voltage range. The Early voltage introduces an error that must be either accounted for, or removed using additional circuitry.

Ask the Experts

Q: I recently saw a diagram for a DECMOS process where the silicide was blocked on a portion of the gate. Why would this be the case?

A: While silicide on the gate is normally useful for lowering the gate resistance, in an ESD protection structure or in a power device, using a non-silicides gate structure can allow the transistor to handle higher levels of current. By partially blocking the silicide on the gate, one can tune the transistors for either better over-voltage protection (gate not solicited) or better standard operating performance (gate silicided).

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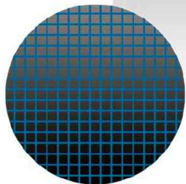

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Spotlight: Semiconductor Reliability and Qualification

OVERVIEW

Package reliability and qualification continues to evolve with the electronics industry. New electronics applications require new approaches to reliability and qualification. In the past, reliability meant discovering, characterizing and modeling failure mechanisms and determining their impact on the reliability of the circuit. Today, reliability can involve tradeoffs between performance and reliability, assessing the impact of new materials, dealing with limited margins, etc. in particular, the proliferation of new package types. This requires information on subjects like: statistics, testing, technology, processing, materials science, chemistry, and customer expectations. While customers expect high reliability levels, incorrect testing, calculations, and qualification procedures can severely impact reliability. Your company needs competent engineers and scientists to help solve these problems. ***Semiconductor Reliability and Qualification*** is a four-day course that offers detailed instruction on a variety of subjects pertaining to semiconductor reliability and qualification. This course is designed for every manager, engineer, and technician concerned with reliability in the semiconductor field, qualifying semiconductor components, or supplying tools to the industry.

What Will I Learn By Taking This Class?

Participants learn to develop the skills to determine what failure mechanisms might occur, and how to test for them, develop models for them, and eliminate them from the product.

1. **Overview of Reliability and Statistics.** Participants learn the fundamentals of statistics, sample sizes, distributions and their parameters.
2. **Failure Mechanisms.** Participants learn the nature and manifestation of a variety of failure mechanisms that can occur both at the die and at the package level. These include: time-dependent dielectric breakdown, hot carrier degradation, electromigration, stress-induced voiding, moisture, corrosion, contamination, thermomechanical effects, interfacial fatigue, etc.
3. **Qualification Principles.** Participants learn how test structures can be designed to help test for a particular failure mechanism.
4. **Test Strategies.** Participants learn about the JEDEC test standards, how to design screening tests, and how to perform burn-in testing effectively.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of the failure mechanisms, test structures, equipment, and testing methods used to achieve today's high reliability components.
2. Participants will be able to gather data, determine how best to plot the data and make inferences from that data.
3. The seminar will identify the major failure mechanisms, explain how they are observed, how they are modeled, and how they are eliminated.
4. The seminar offers a variety of video demonstrations of analysis techniques, so the participants can get an understanding of the types of results they might expect to see with their equipment.

5. Participants will be able to identify the steps and create a basic qualification process for semiconductor devices.
6. Participants will be able to knowledgeably implement screens that are appropriate to assure the reliability of a component.
7. Participants will be able to identify appropriate tools to purchase when starting or expanding a laboratory.

COURSE OUTLINE

Day 1 (Lecture Time 8 Hours)

1. Introduction to Reliability
    1. Basic Concepts
    2. Definitions
    3. Historical Information
2. Statistics and Distributions
    1. Basic Statistics
    2. Distributions (Normal, Lognormal, Exponent, Weibull)
    3. Which Distribution Should I Use?
    4. Acceleration
    5. Number of Failures

Day 2 (Lecture Time 8 Hours)

1. Overview of Die-Level Failure Mechanisms
    1. Time Dependent Dielectric Breakdown
    2. Hot Carrier Damage
    3. Negative Bias Temperature Instability
    4. Electromigration
    5. Stress Induced Voiding
2. Package Level Mechanisms
    1. Ionic Contamination
    2. Moisture/Corrosion
        1. Failure Mechanisms
        2. Models for Humidity
        3. Tja Considerations
        4. Static and Periodic stresses
        5. Exercises
    3. Thermo-Mechanical Stress
        1. Models
        2. Failure Mechanisms
    4. Interfacial Fatigue
        1. Low-K fracture
    5. Thermal Degradation/Oxidation

Day 3 (Lecture Time 8 Hours)

1. Package Attach (Solder) Reliability
    1. Creep/Sheer/Strain
    2. Lead-Free Issues
    3. Electromigration/Thermomigration
    4. MSL Testing
    5. Exercises
2. TSV Reliability Overview
3. Board Level Reliability Mechanisms
    1. Interposer
    2. Substrate
4. Electrical Overstress/ESD
5. Test Structures and Test Equipment
6. Developing Screens, Stress Tests, and Life Tests
    1. Burn-In
    2. Life Testing
    3. HAST
    4. JEDEC-based Tests
    5. Exercises

Day 4 (Lecture Time 8 Hours)

1. Calculating Chip and System Level Reliability
2. Developing a Qualification Program
    1. Process
    2. Standards-Based Qualification
    3. Knowledge-Based Qualification
    4. MIL-STD Qualification
    5. JEDEC Documents (JESD47H, JESD94, JEP148)
    6. AEC-Q100 Qualification
    7. When do I deviate? How do I handle additional requirements?
    8. Exercises and Discussion

INSTRUCTIONAL STRATEGY

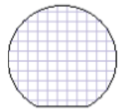
By using a combination of instruction by lecture, video, problem solving and question/answer sessions, participants will learn practical approaches to the failure analysis process. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field. The handbook offers hundreds of pages of additional reference material the participants can use back at their daily activities.

The Semitracks Analysis Instructional Videos™

One unique feature of this workshop is the video segments used to help train the students. Reliability Analysis is a visual discipline. The ability to identify nuances and subtleties in graphical data is critical to locating and understanding the defect. Some tools output video images that must be interpreted by engineers and scientists. No other course of this type uses this medium to help train the participants. These videos allow the analysts to directly compare material they learn in this course with real analysis work they do in their daily activities.

You may want to stress some aspects more than others or conduct a simple one-day overview course. Many of our clients seek ongoing just-in-time training that builds in-depth, advanced levels of reliability expertise. We'll work with you to determine the best course of action and create a statement of work that emulates the very best practices of semiconductor reliability analysis.

Our instructors are active in the field and they practice the disciplines daily. Please give us a call (505) 858-0454 or drop us an e-mail (info@semitracks.com).



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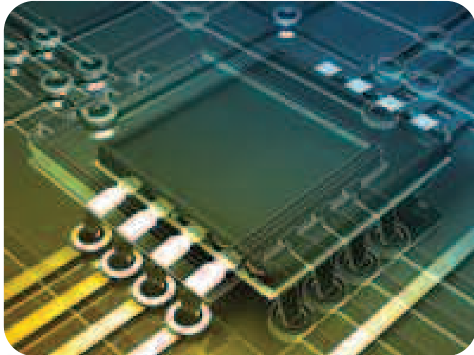
Chris Henderson, IRPS Board

Chris would be happy to meet with you and discuss any training needs you have. Contact him at henderson@semitracks.com during the symposium!



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(Click on each item for details)

Defect Based Testing
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Failure and Yield Analysis
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Munich, Germany

Semiconductor Reliability and Qualification
May 15 – 18, 2017 (Mon – Thur)
Munich, Germany

Semiconductor Statistics
May 22 – 23, 2017 (Mon – Tue)
Munich, Germany

Wafer Fab Processing
June 5 – 8, 2017 (Mon – Thur)
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