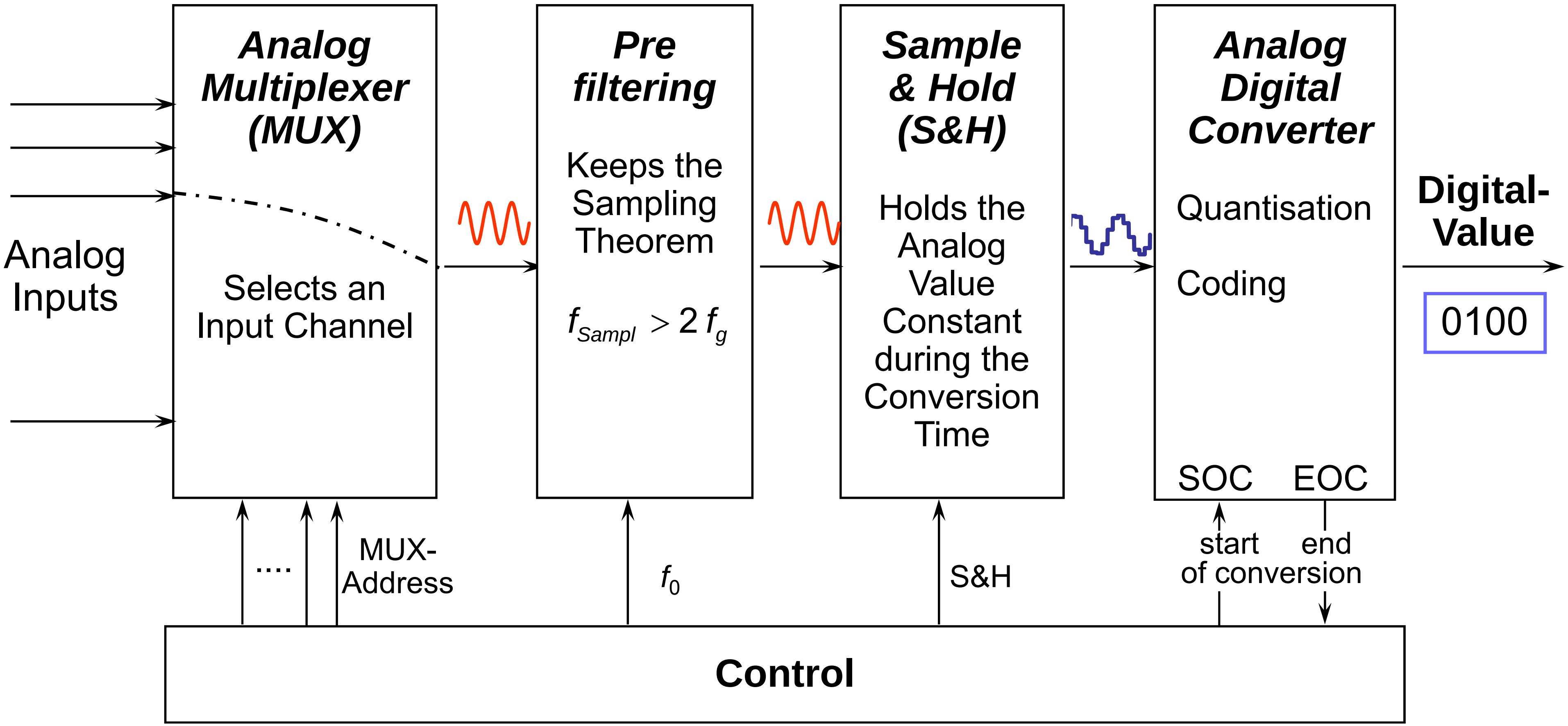
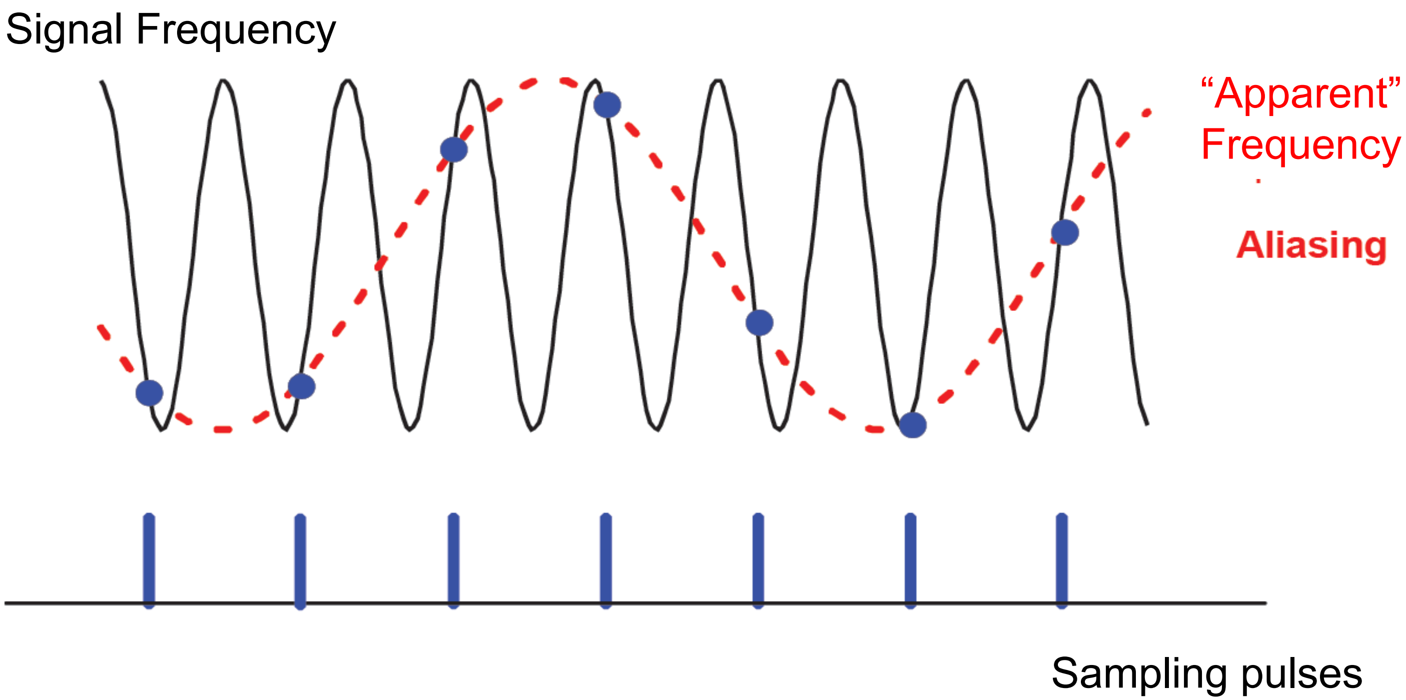
7 Analog-Digital-Conversion

7.1 Components of A/D-Converters

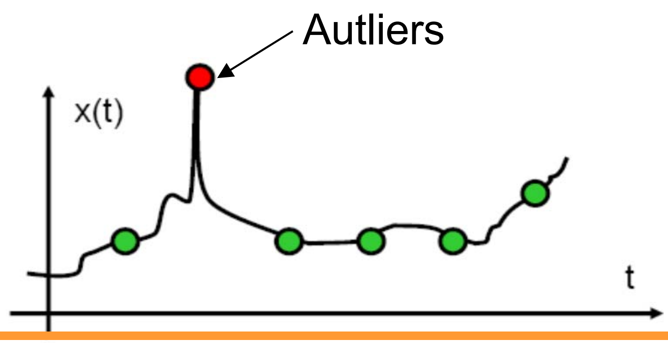


7.1 Components of A/D-Converters

Sampling



Autliers



Earlier or later sampling gives a different result

7.1 Components of A/D-Converters

Sampling

$$x_a(t) = x_e(t) \sum_{k=-\infty}^{+\infty} \delta(t - kT_0)$$

Sampling Periode $T_0 = \frac{1}{f_{Sampl}}$

Fourier Transformation

$$x_e(t) \circ\!\!-\!\!\bullet\; X_e(\omega) = \int_{-\infty}^{\infty} x_e(t) e^{-j\omega t}\, dt$$

Inverse Fourier Transformation

$$x_e(t) = \frac{1}{2\pi} \int_{-\infty}^{\infty} X_e(\omega) e^{j\omega t}\, dt$$

Multiplication in Time Domain → Convolution in Frequency Domain

$$x(t)u(t) \circ\!\!-\!\!\bullet\; X(\omega) * U(\omega) = \int_{-\infty}^{\infty} X(\omega')\,U(\omega - \omega')\,d\omega'$$

7.1 Components of A/D-Converters

Sampling

$$x_e(t) \circ\!\!-\!\!\bullet X_e(\omega)$$

$$\sum_{k=-\infty}^{+\infty} \delta(t - kT_0) \circ\!\!-\!\!\bullet \frac{1}{T_0} \sum_{n=-\infty}^{\infty} \delta\left(f - \frac{n}{T_0}\right)$$

T_0 : Sampling Periode

$$x_a(t) = x_e(t) \sum_{k=-\infty}^{+\infty} \delta(t - kT_0) \circ\!\!-\!\!\bullet X_a(f) = X_e(f) * \frac{1}{T_0} \sum_{n=-\infty}^{\infty} \delta\left[f - \frac{n}{T_0}\right]$$

$$= \int_{-\infty}^{\infty} \left\{ \frac{1}{T_0} \sum_{n=-\infty}^{\infty} \delta\left[u - \frac{n}{T_0}\right] \right\} X_e(f-u)\,du$$

(Changing Summation and Integral) $$= \frac{1}{T_0} \sum_{n=-\infty}^{\infty} \int_{-\infty}^{\infty} \delta\left[u - \frac{n}{T_0}\right] X_e(f-u)\,du$$

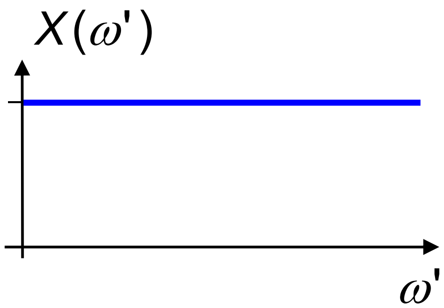
(Dirac-Function) $$= \frac{1}{T_0} \sum_{n=-\infty}^{\infty} X_e\left(f - \frac{n}{T_0}\right)$$

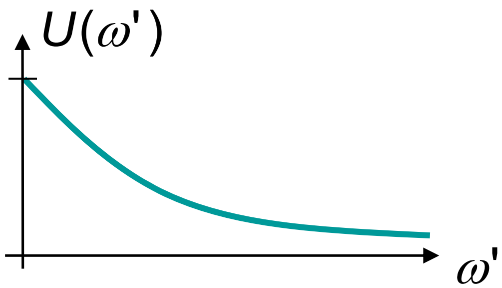
7.1 Components of A/D-Converters

Sampling

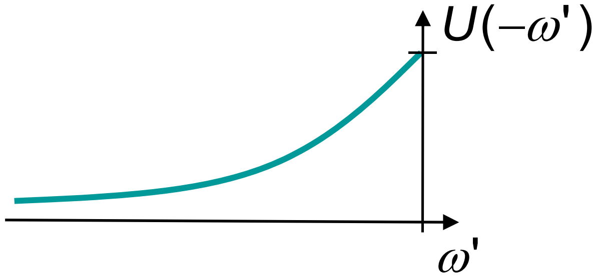
Example Convolution

$$X(\omega) * U(\omega) = \int_{-\infty}^{\infty} X(\omega')\,U(\omega-\omega')\,d\omega'$$

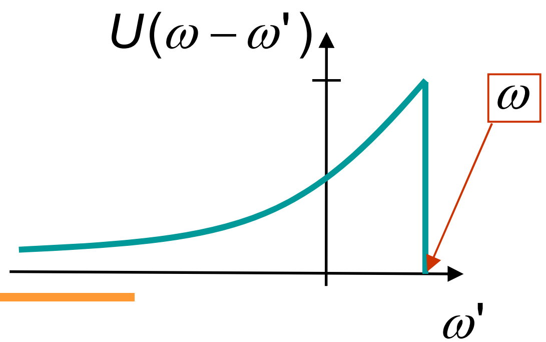




Mirroring



Translation



Sampling

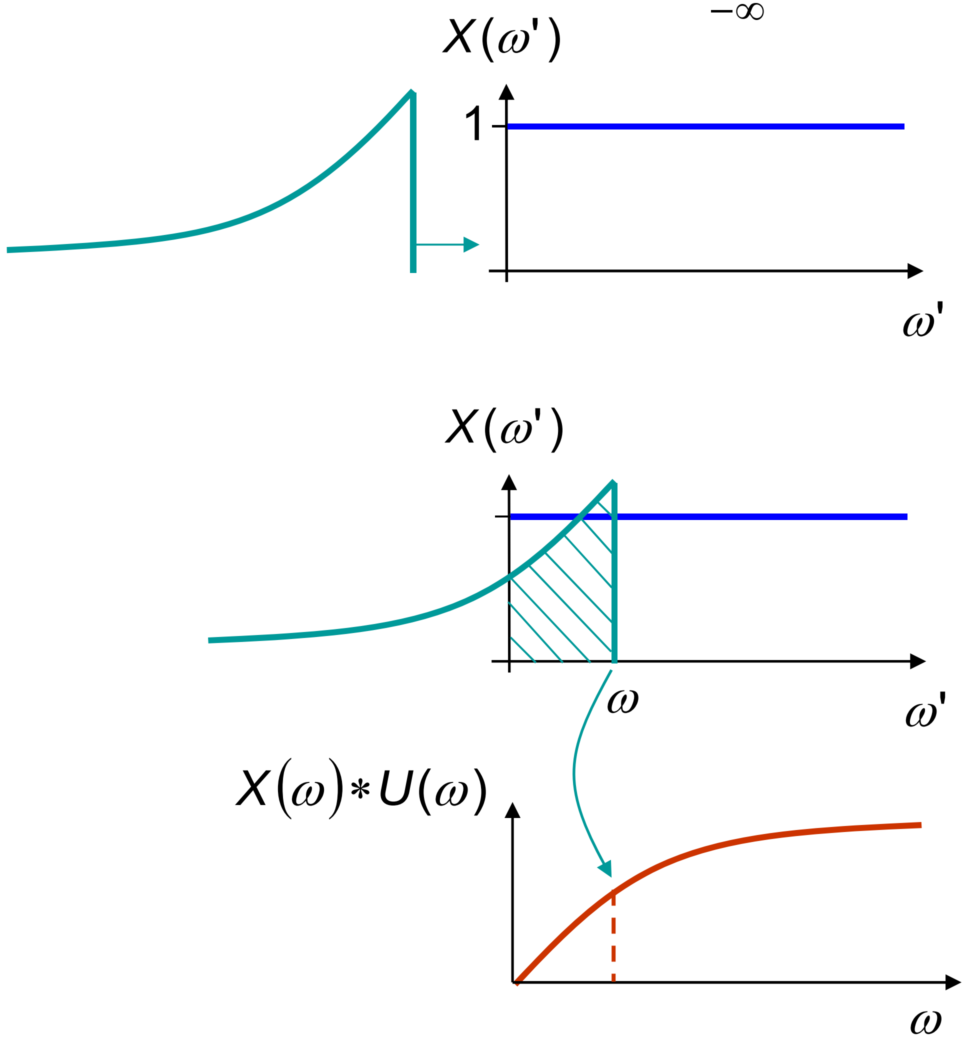
Example Convolution

$$X(\omega) * U(\omega) = \int_{-\infty}^{\infty} X(\omega')\,U(\omega-\omega')\,d\omega'$$

Translation

Multiplication

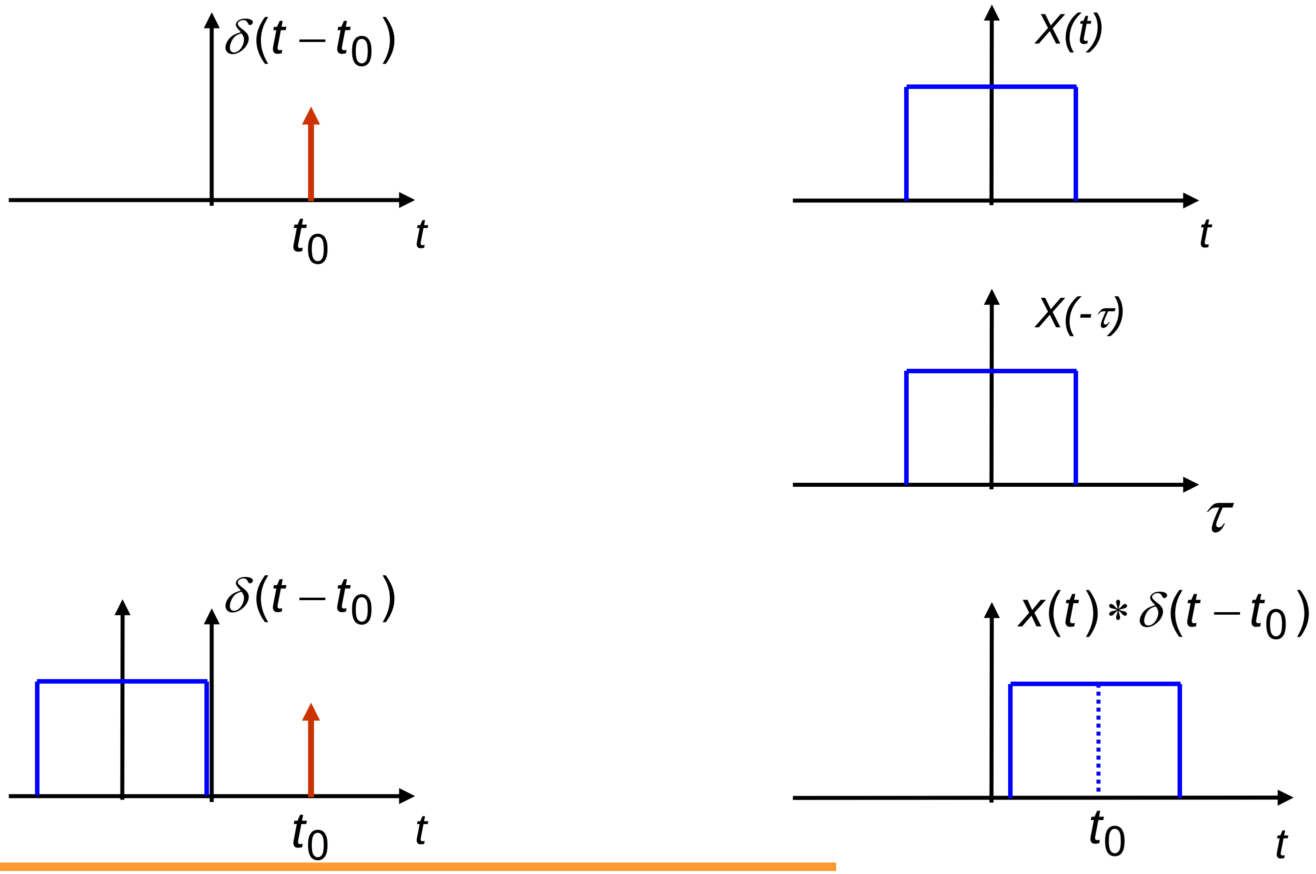
Integration



7.1 Components of A/D-Converters
Sampling

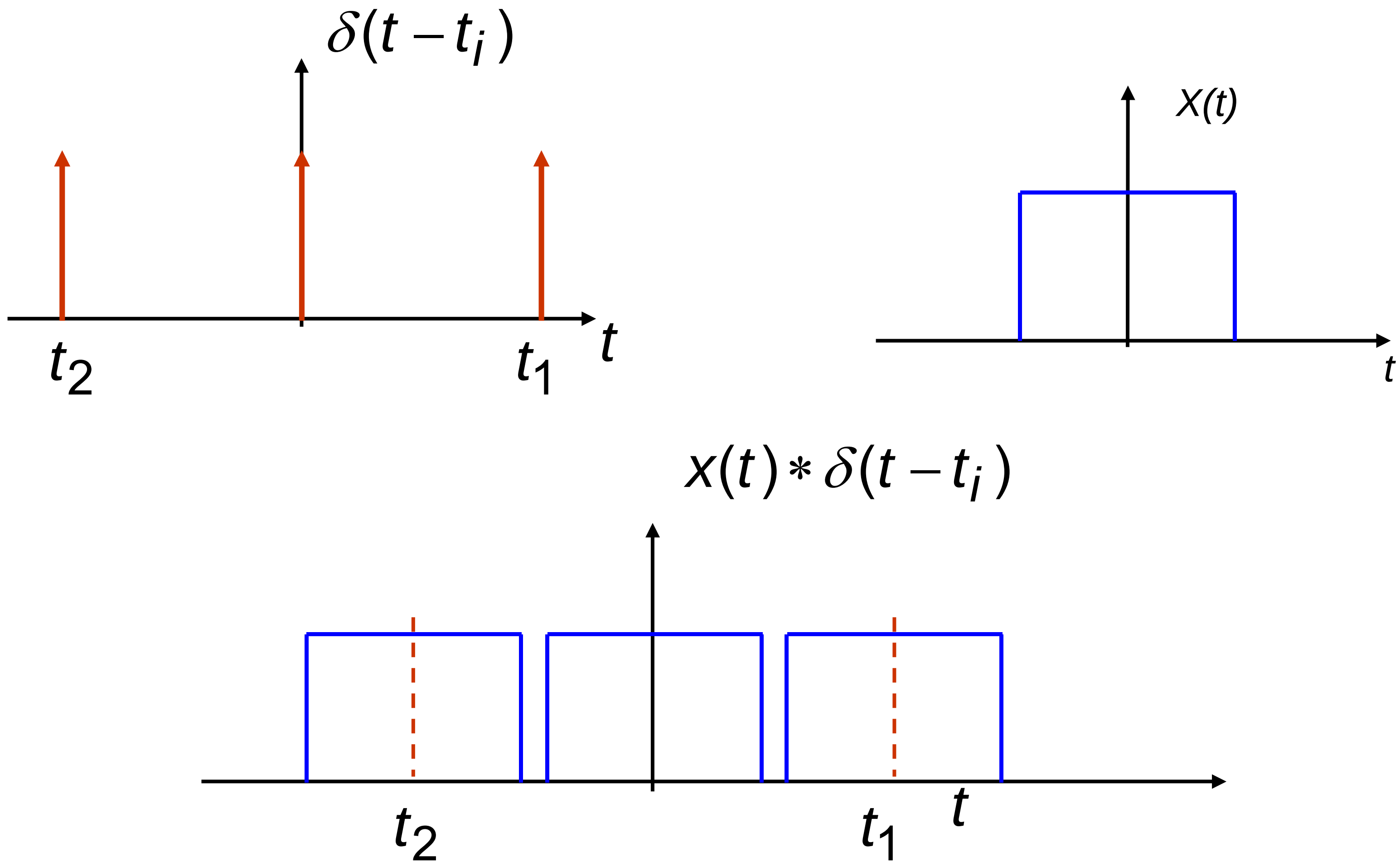
Example Convolution with a Dirac Pulse

$$X(t) * \delta(t - t_0) = \int_{-\infty}^{\infty} \delta(t - t_0) \cdot X(t - \tau) d\tau = X(t - t_0)$$



Sampling

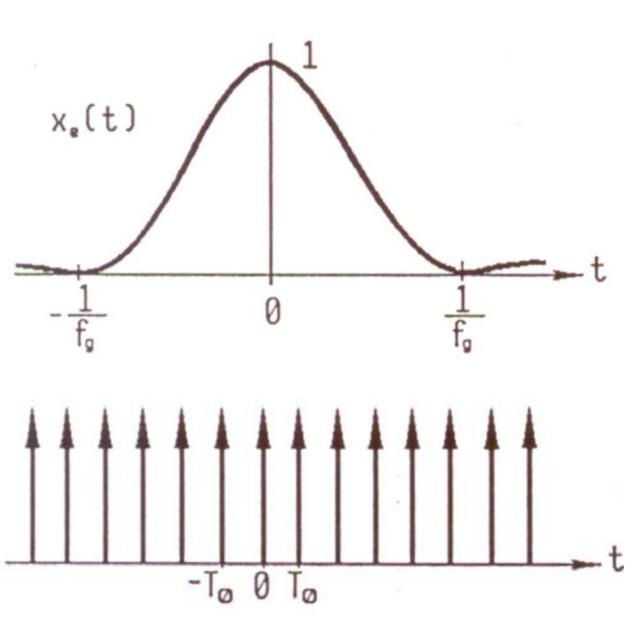
Example Convolution with a Dirac Pulse



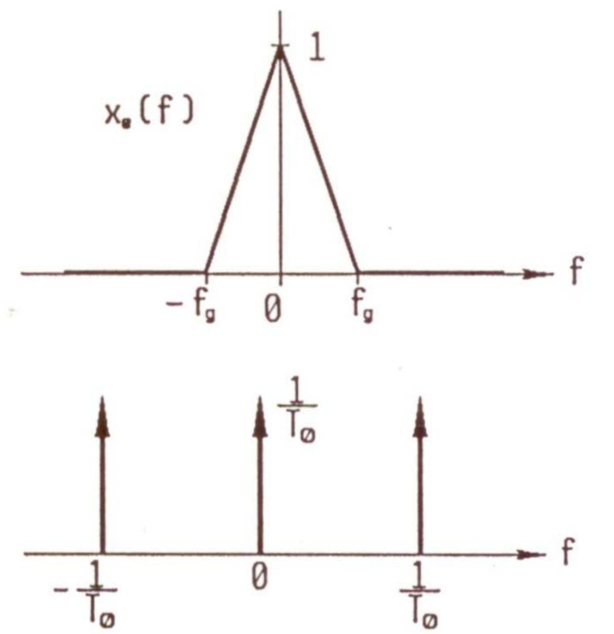
7.1 Components of A/D-Converters

Sampling

Time Domain

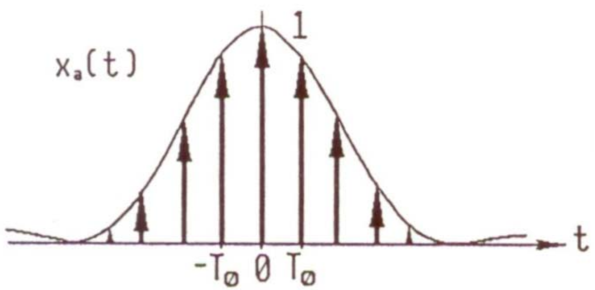


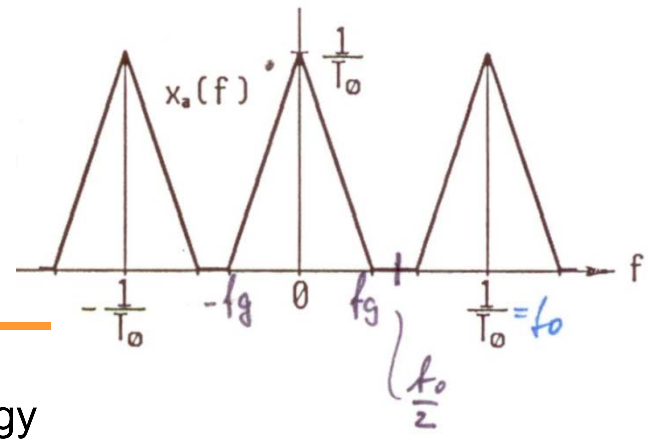
Frequency Domain



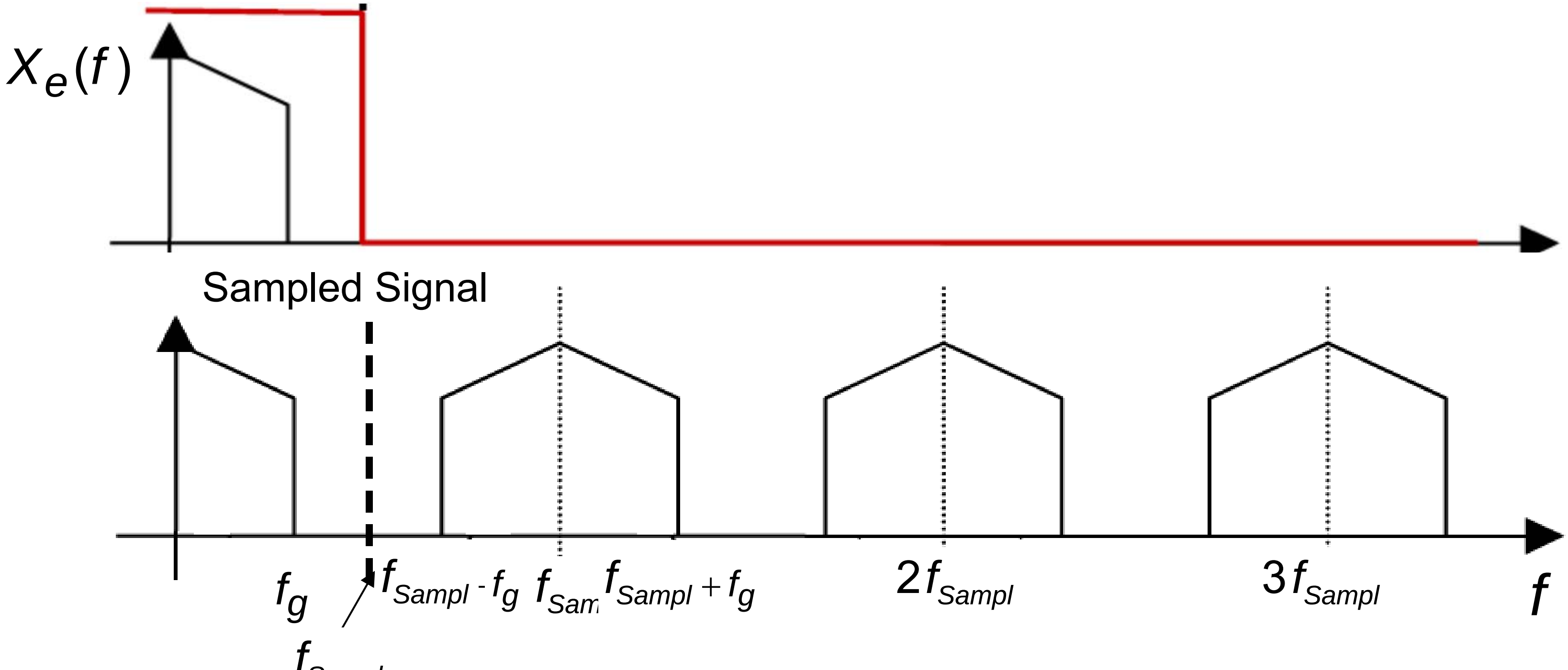
Multication

Convolution





Sampling



$\frac{f_{Sampl}}{2} < f_g$ ▷ Overlapping ▷ Signal can not be reconstructed

Sampling theorem by Shannon or Nyquist-Criterion

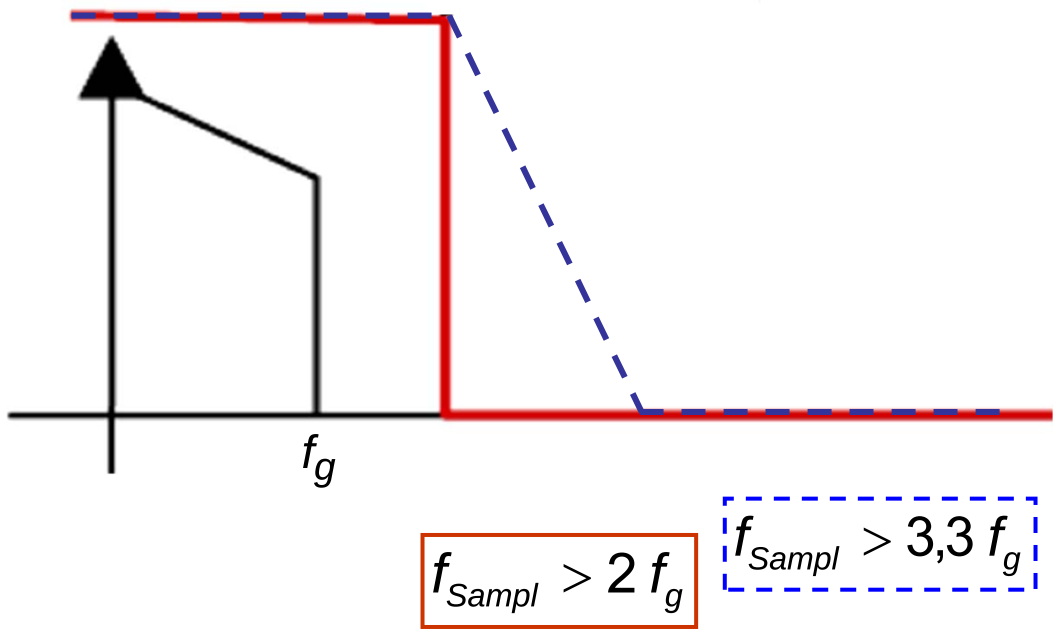
$f_{Sampl} > 2\,f_g$ or more general $f_{Sampl} > 2\,(f_{max} - f_{min})$

7.1 Components of A/D-Converters

Anti-aliasing-Filter

$f > \frac{f_{Sampl}}{2}$ Pre-filtering ▷ no overlapping!

The slow rate of the Filter should be considered!

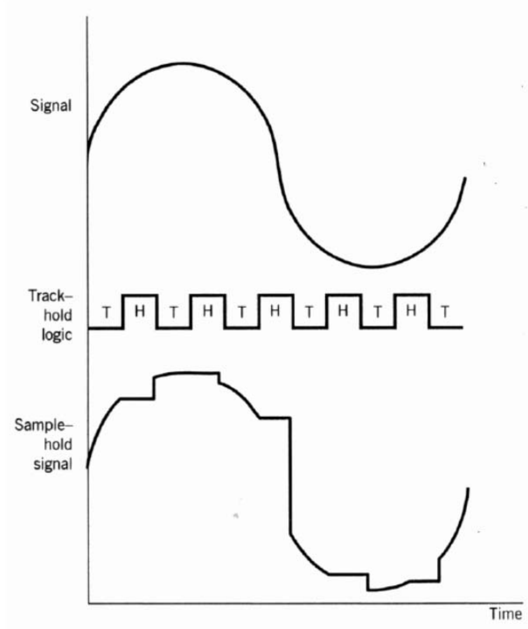


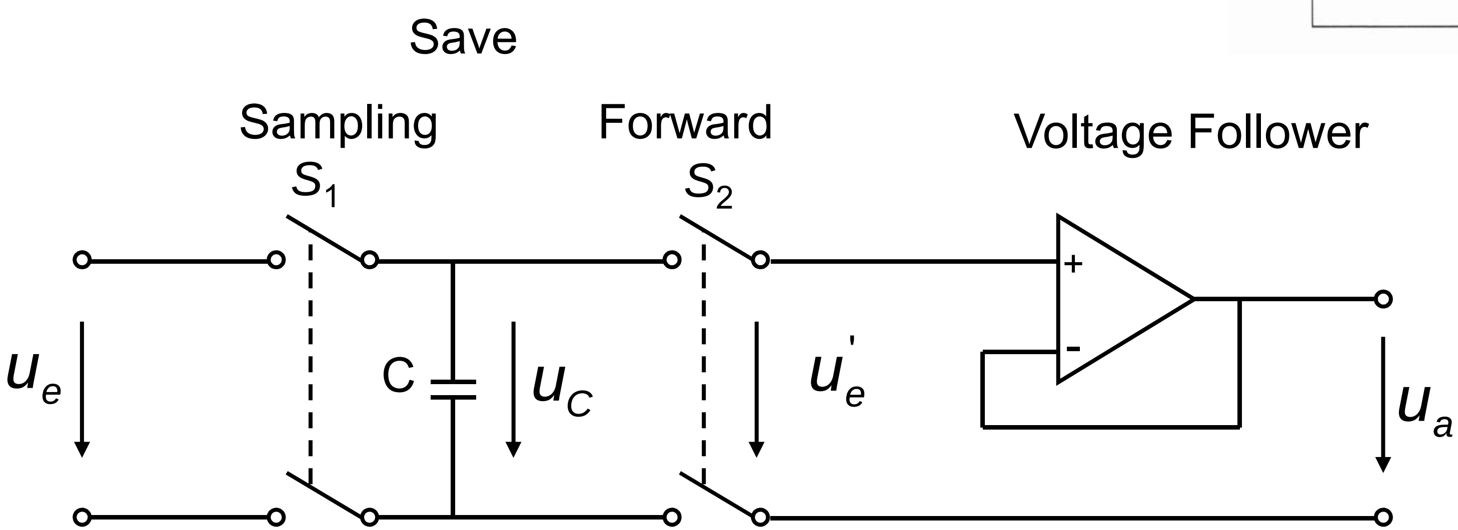
7.1 Components of A/D-Converters

Sample & Hold Circuit

→ Signal amplitude is hold constant during A/D-Conversion

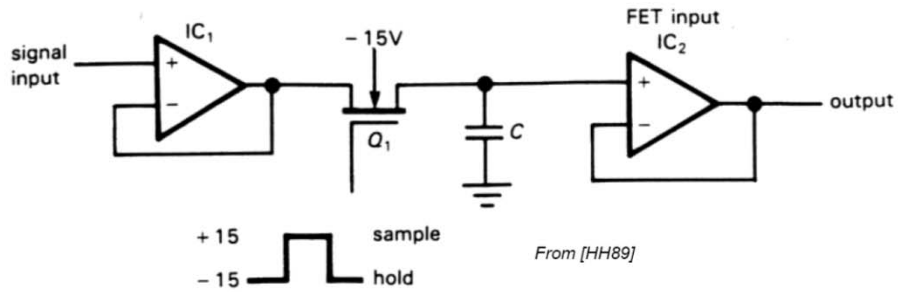
	S_1	S_2
Step 1: Sample	closed	opened
Step 2: Hold	opened	closed





No galvanic Connection to the input u_e

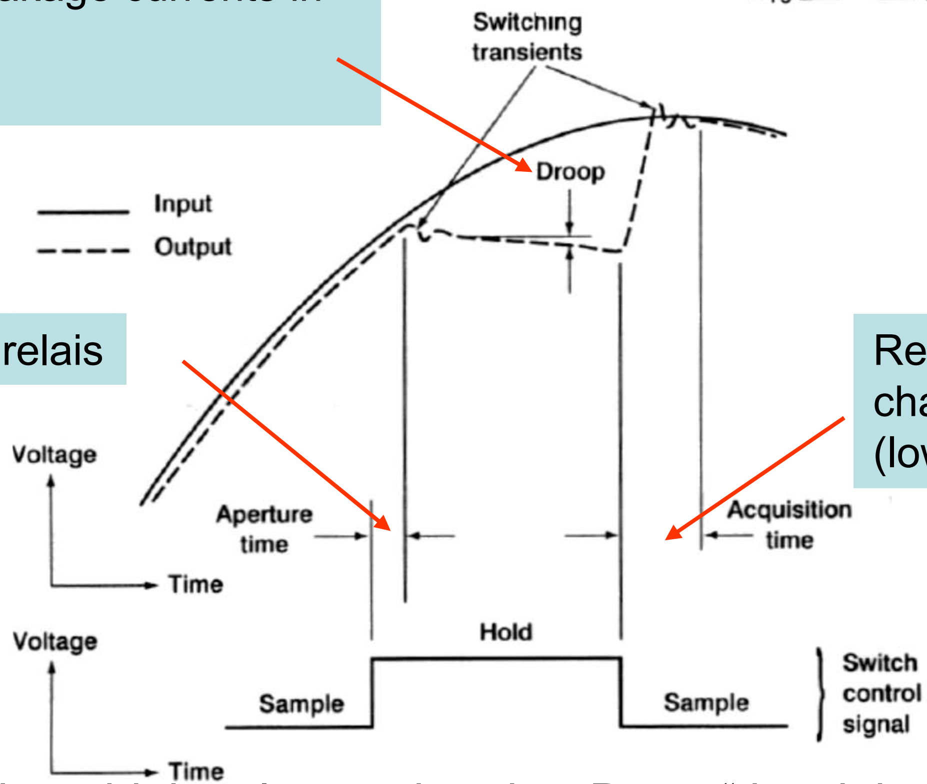
Sample & Hold Circuit



Droop (Regeldifferenz):
Discharge of the Capacitance because of leakage currents in Q1 und IC2
(~1mV/ms)

Opening the relais

Response time and charging the Capacitance (low pass from Q1 and C)



C should habe a high value so that the „Droop“ is minimized

C should have a low value, so that fast changing signals can be followed

7.1 Components of A/D-Converters

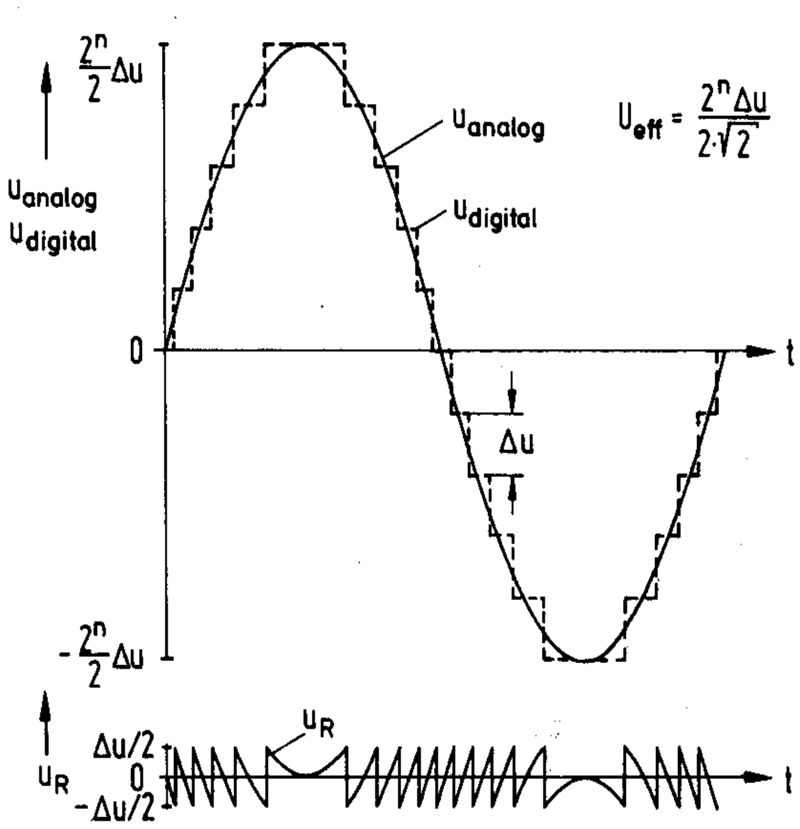
N-Digits digital number

	2-digits number	N-digits number
	$\overline{Z_1 Z_0}$	$\overline{Z_{N-1} \cdots Z_1 Z_0}$
Number of Digits	2	N
Number of Output Stages	$4=2^2$	$n= 2^N$
Number of counting steps	$3 = 2^2-1$	2^N-1
Quantisation step	$U_q = \frac{U_{e,\max}}{2^2 - 1}$	$U_q = \frac{U_{e,\max}}{2^N - 1}$
Shift Thresholds at	$U_{Um} = \frac{1}{2} \cdot \frac{U_{e,\max}}{2^2 - 1} + U_q + \cdots + U_q$	$U_{Um} = \frac{1}{2} \cdot \frac{U_{e,\max}}{2^N - 1} + U_q + \cdots + U_q$
Quantisation noise	$\frac{U_{e,\max}}{6} = \frac{1}{2} \cdot \frac{U_{e,\max}}{2^2 - 1}$	$\frac{1}{2} \cdot \frac{U_{e,\max}}{2^N - 1}$

7.1 Components of A/D-Converters
Quantisierungsfehler

$$\left|error_{quantisieung}\right| = \frac{\Delta X_{LSB}}{2} = \frac{1}{2} \cdot \frac{X_{max} - X_{min}}{Output\,Steps}$$

$$= \frac{1}{2} \frac{X_{max} - X_{min}}{2^N - 1}$$



$X_{\max} - X_{\min}$: Analog values sector

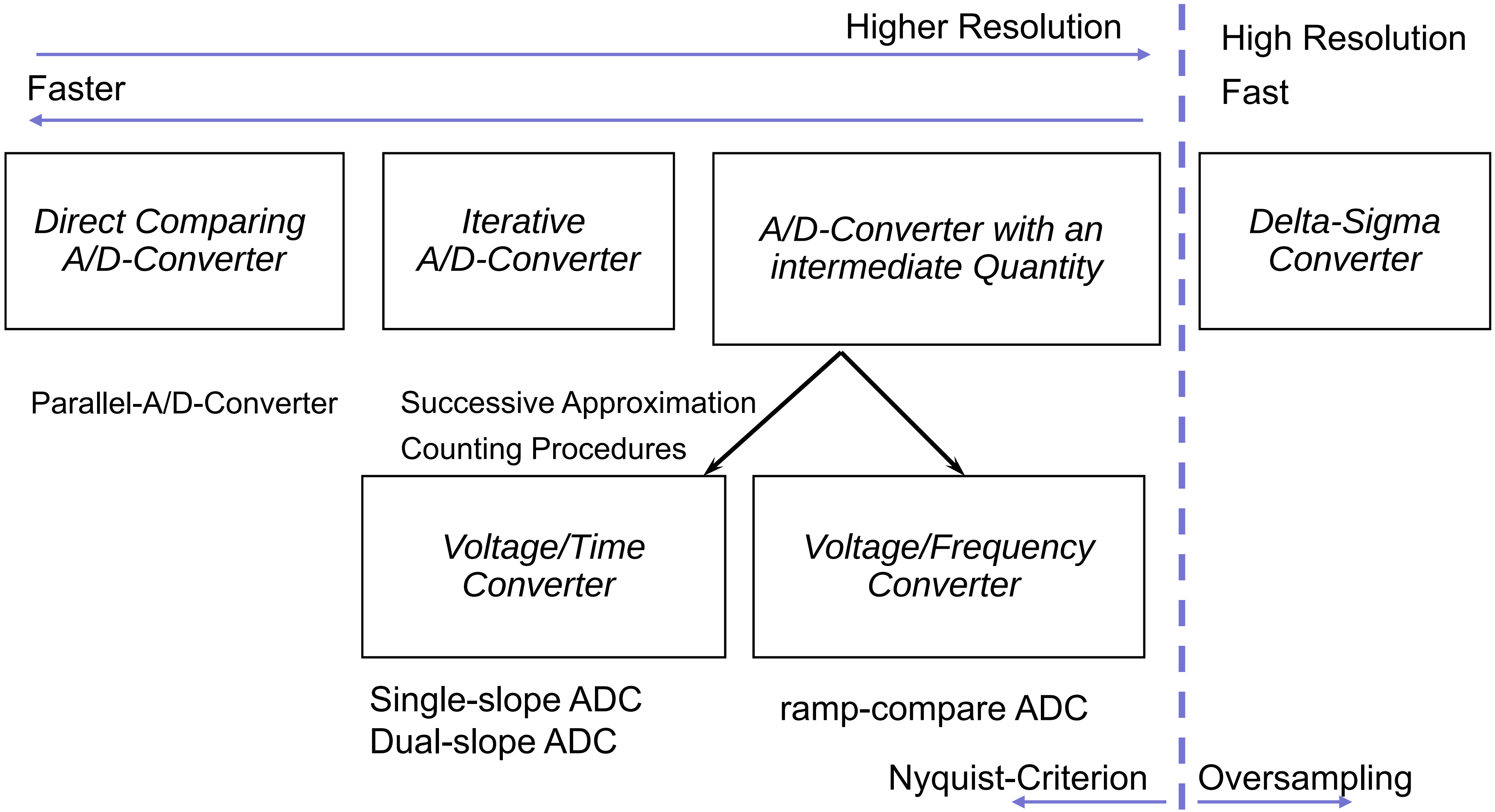
N: Number of Digits

Signal-Noise-ratio

$$\frac{S}{N}[dB] = 20\lg\left(\frac{U_{signal,eff}}{U_{noise,eff}}\right)$$

$$U_{noise,eff} = \sqrt{\frac{1}{T}\int_{-\frac{T}{2}}^{\frac{T}{2}}\left(U_{LSB}\frac{t}{T}\right)^2 dt} = \frac{U_{LSB}}{\sqrt{12}}$$

Classification of Analog/Digital-Converters



See: http://groups.uni-paderborn.de/cc/arbeitsgebiete/messtech/simulationen/ad/index.html

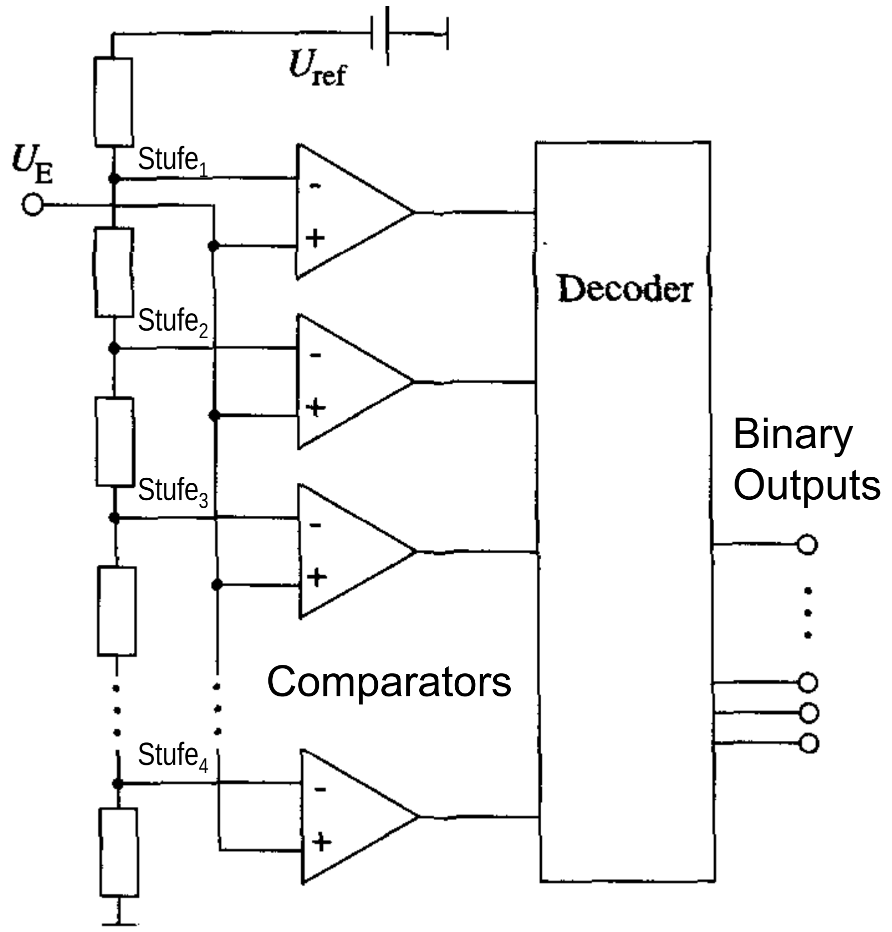
7.2 Flash A/D-Converter

Principle

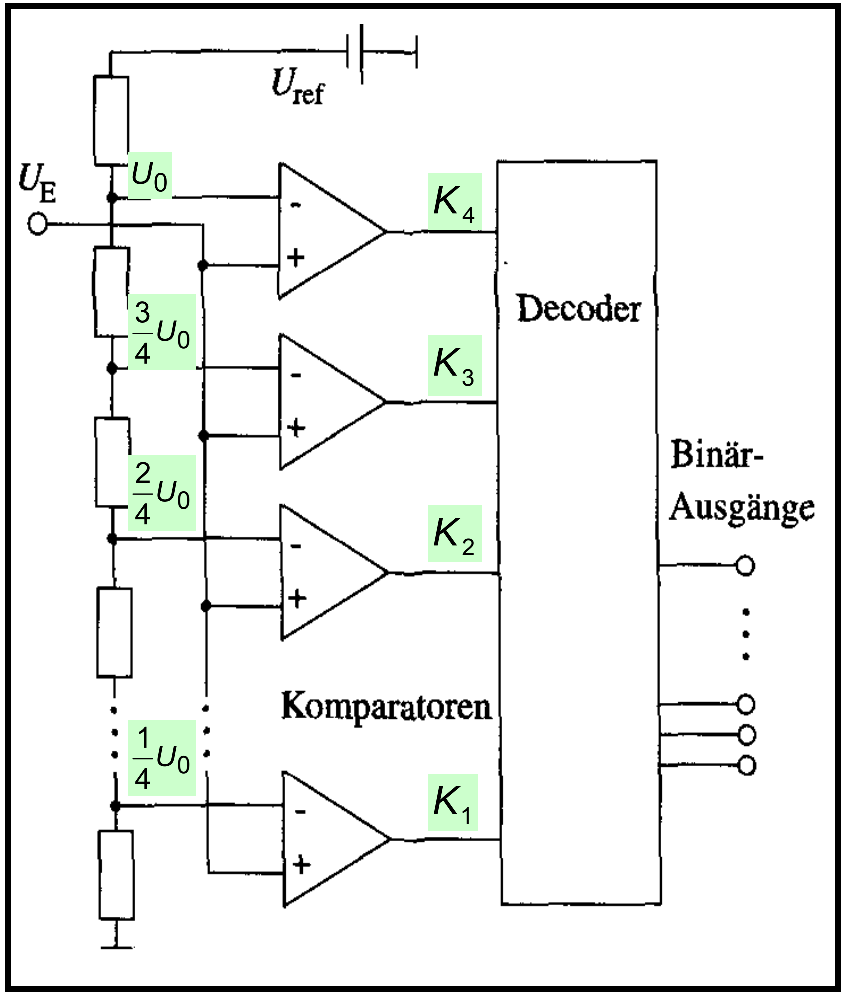
Comparison of the voltage to be converted with well known graduated reference voltages

Properties

- *Resolution 4 to 12 Bit*
- *Suitable for a high signal dynamic*



7.2 Flash A/D-Converter



Example: Parallel-A/D-Converter with 4-Comparators

Voltage	Comparator Signals $K_1\ K_2\ K_3\ K_4$	Digital Number $\overline{Z_2 Z_1 Z_0}$	Output U_E/U_{ref}
$0 \le U_E < \frac{1}{4}U_0$	0 0 0 0	000	0
$\frac{1}{4}U_0 \le U_E < \frac{2}{4}U_0$	1 0 0 0	001	0,25
$\frac{2}{4}U_0 \le U_E < \frac{3}{4}U_0$	1 1 0 0	010	0,5
$\frac{3}{4}U_0 \le U_E < \frac{4}{4}U_0$	1 1 1 0	011	0,75
$U_E \ge U_0$	1 1 1 1	100	1

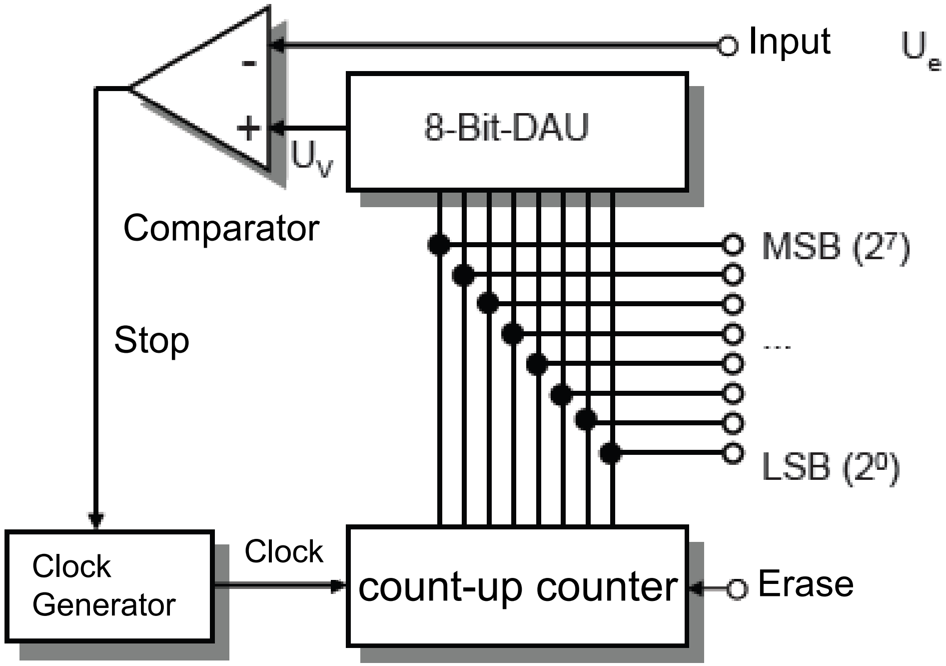
Decoder

Conversion Time dependent on switching speed of the comparators and the coder

– 10^8 Values/sec
– high expenditure, 8-Bit ADU necessitates $2^8 - 1$ comparators!

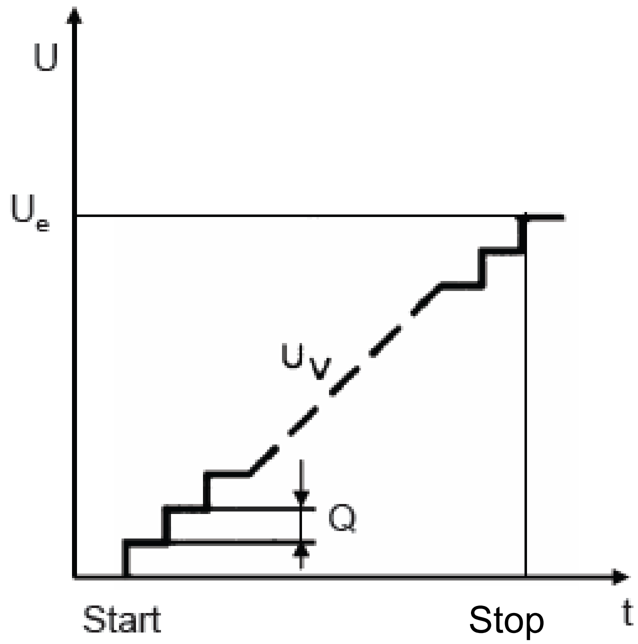
7.3 Iterative AD-Converter
Counting Procedure→ Use of D/A-Converter

Advantage: better resolution through more adjustable steps



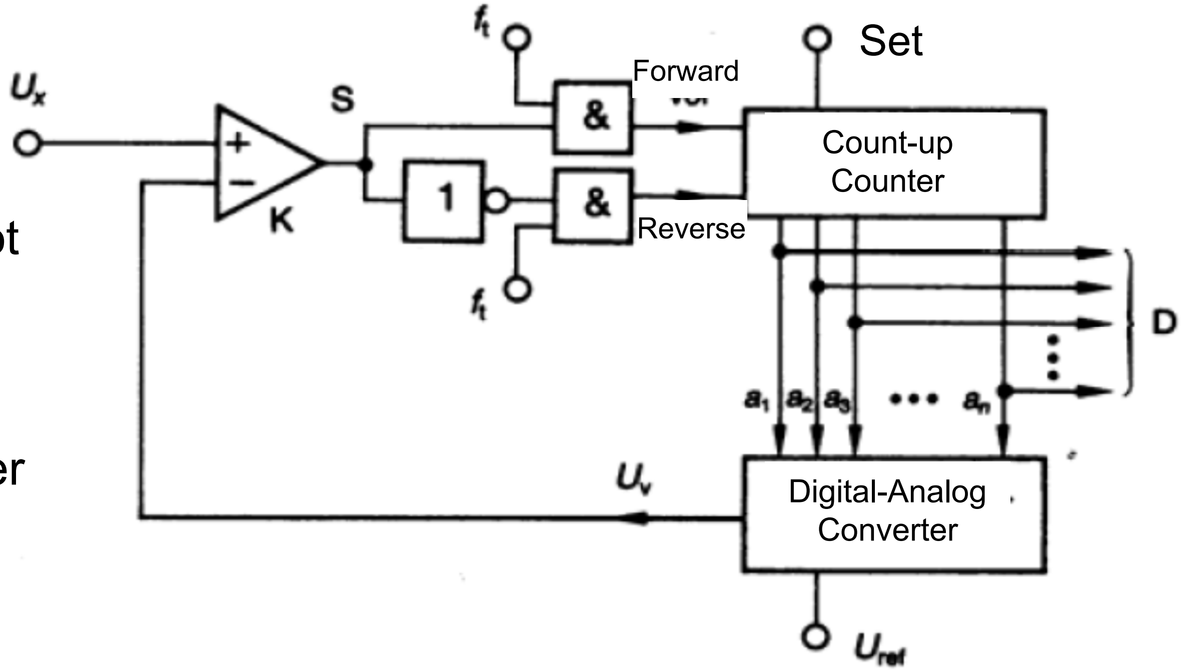
- Count increases by 1→ U_V increases by Q=ΔU
- Reference voltage U_V at the output of the DAU
- Compare with U_e
- Equality → stop counting
- otherwise the counter increased (at clock)
- new counter signal is D/A-converted
- Procedure is repeated until $U_V > U_e$

Convesion time is dependent on :
- Transient behavior of D/A-Converter
- Switching speed of comparators
- Input value
- Number of digits n of output(max. $2n$ steps)
- Clock Frequency f

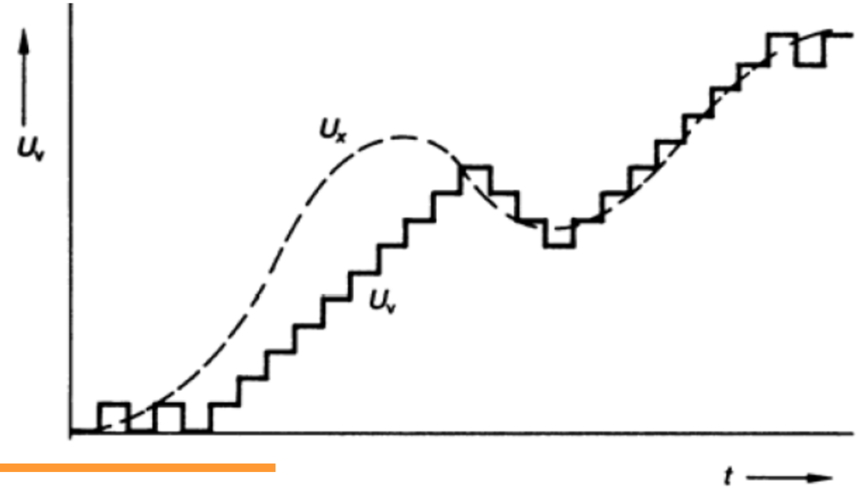


Incremental Follow-Up-Converter

- forward and reverse counter
- By a new conversion U_v is not reset to „0“
- Saves time in comparison with the incremental converter



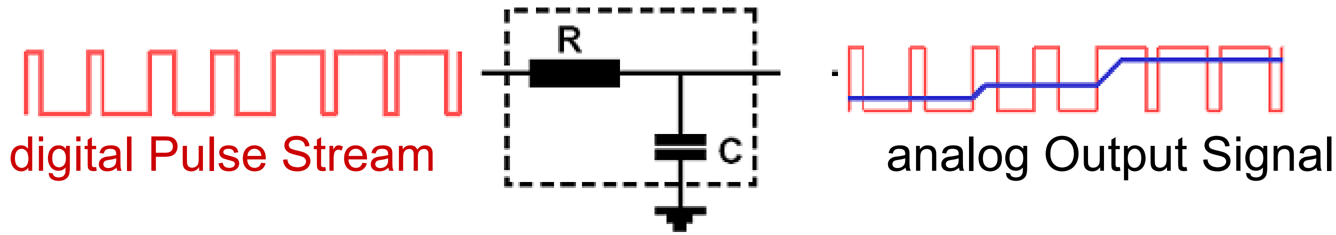
The conversion is terminated, when U_v is alternating increased and decreased by ΔU



Digital- Analog-Converter by Pulse Wide Modulation

Basic Coponents

- Digital stream
- RC-low pass filter

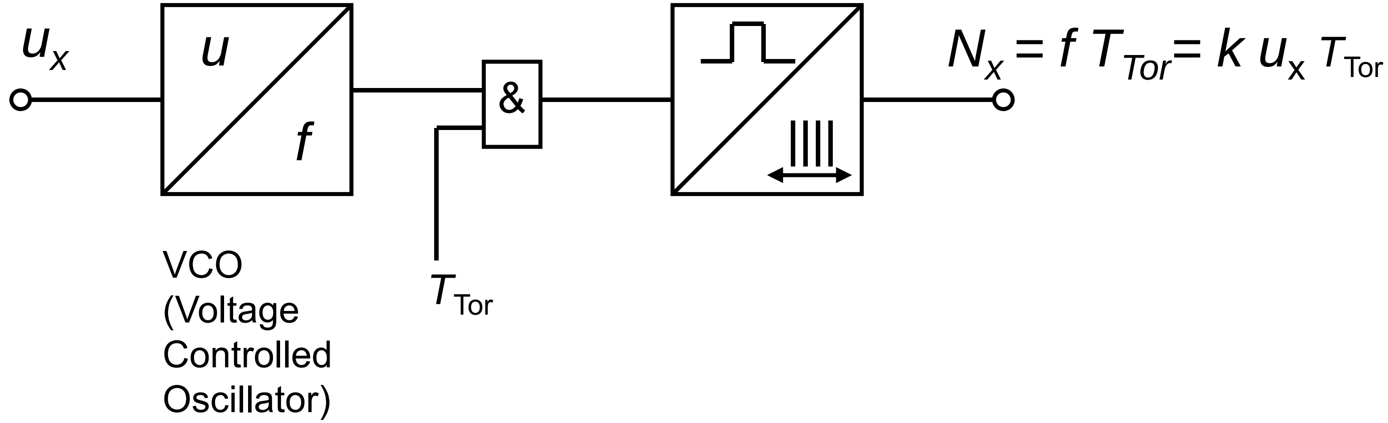


Function

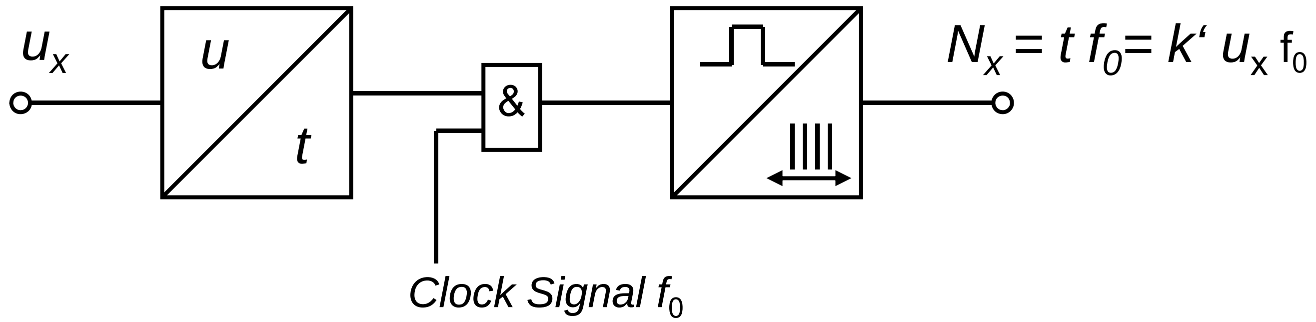
- The digital pulses have the same frequency
- The pulse wide („High“-Duration) is proportional to the output voltage
- The digital pulse stream is low pass filtered
- The analog output voltage of the low pass filter is proportional to the mean duration of the „High“-level

7.4 A/D-Converter with an Intermediate Quantity

u/f-Converter

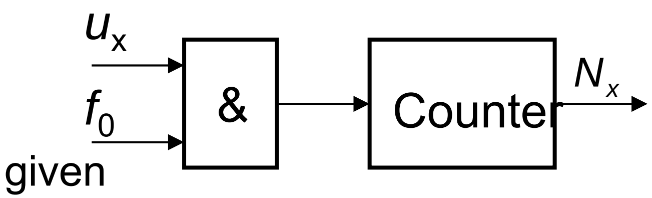


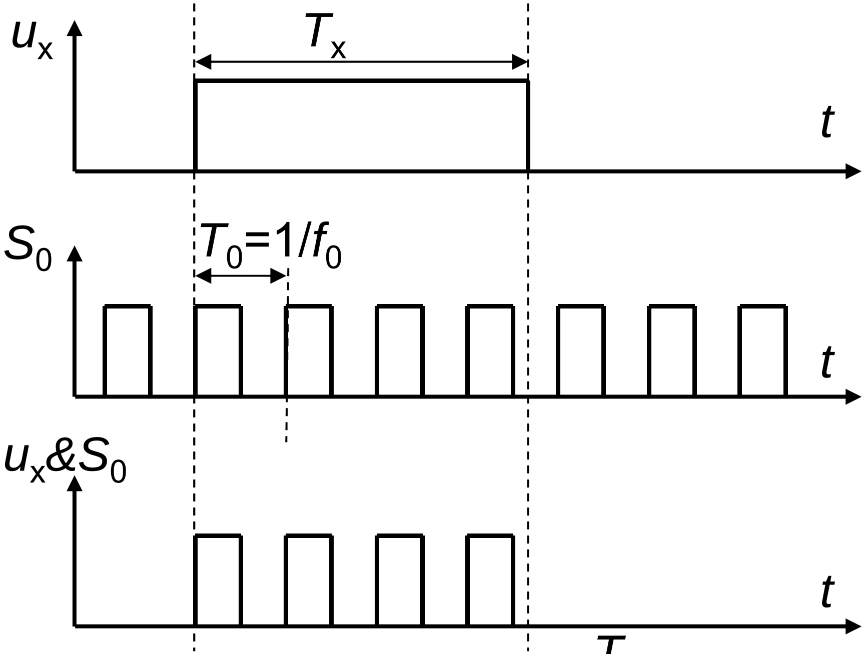
u/t-Converter



7.4 A/D-Converter with an Intermediate Quantity

Periode Duration Measurement



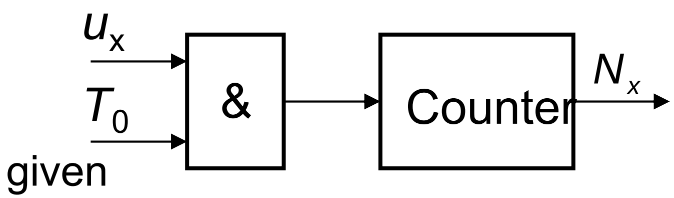


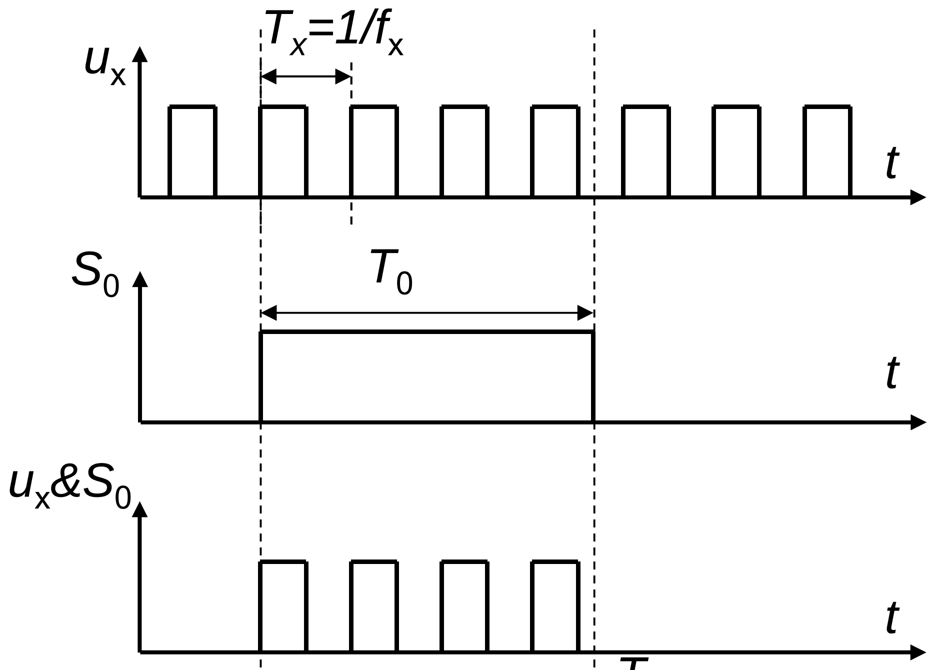
$$N_x = \frac{T_x}{T_0} = f_0 \cdot T_x$$

$$T_x = \frac{N_x}{f_0}$$

$$\left|\frac{\Delta T_x}{T_x}\right| = \left|\frac{\Delta N_x}{N_x}\right| + \left|\frac{\Delta f_0}{f_0}\right| \approx \left|\frac{1}{N_x}\right|$$

Frequency Measurement





$$N_x = \frac{T_0}{T_x} = f_x \cdot T_0$$

$$f_x = \frac{N_x}{T_0}$$

$$\left|\frac{\Delta f_x}{f_x}\right| = \left|\frac{\Delta N_x}{N_x}\right| + \left|\frac{\Delta T_0}{T_0}\right| \approx \left|\frac{1}{N_x}\right|$$

7.4 A/D-Converter with an Intermediate Quantity
u/f- Sawtooth-Converter

$t_1 < t < t_x$

$$U_a(t) = U_o - \frac{1}{C}\int_{t1}^{tx} \frac{U_x}{R}\, dt = U_o - \frac{1}{RC}\int_{t1}^{tx} U_x\, dt$$

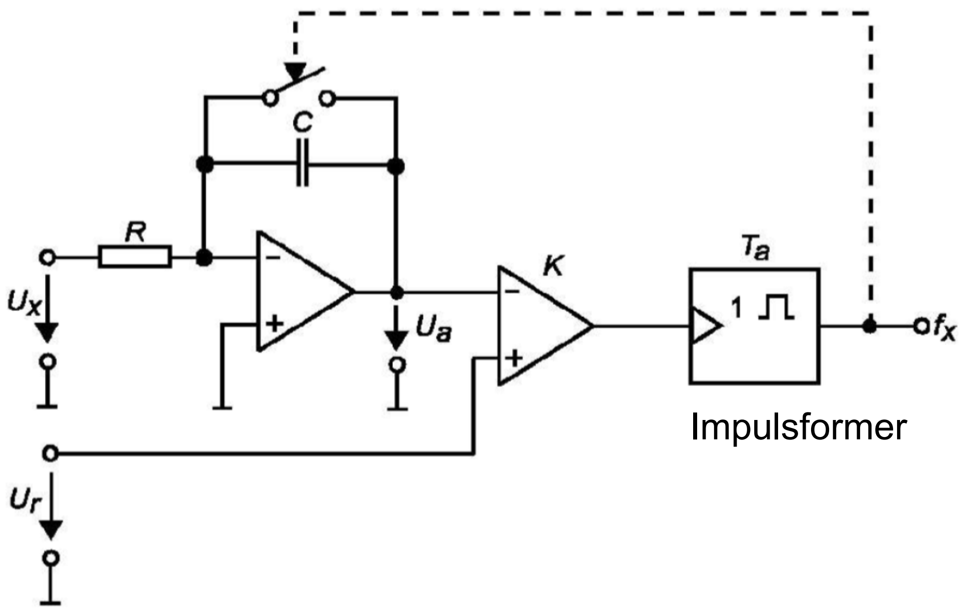
If U_a reaches U_r → the relais is closed during T_a

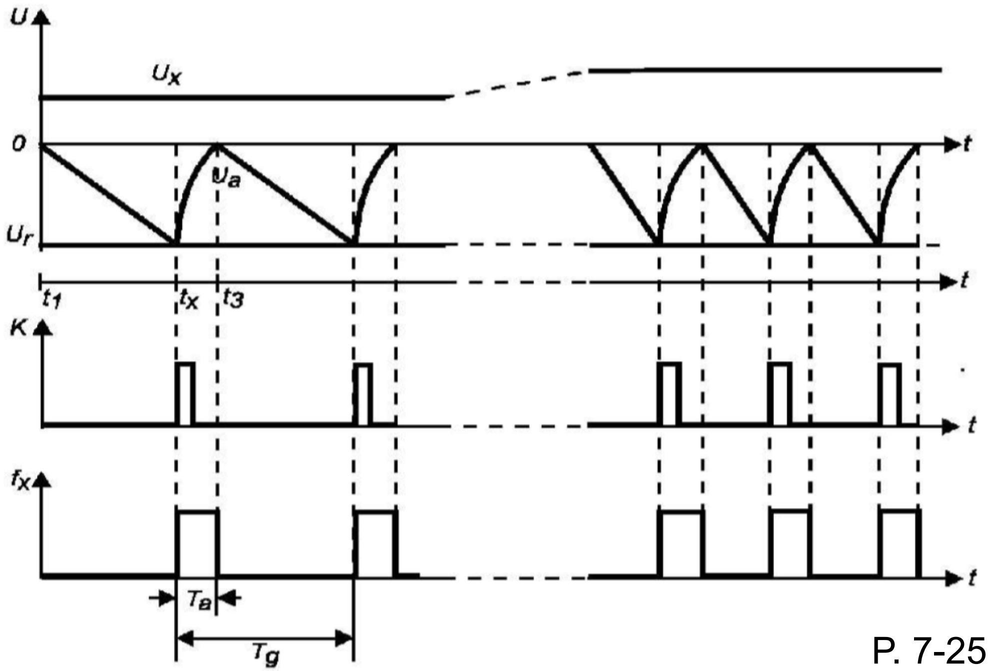
The capacitance is discharged during the constant time T_a

$$f_x = \frac{1}{(t_x - t_1) + T_a}$$

The frequency of occurence of the pulses is dependent on the Integration time (t_x-t_1)

- Relative slow, sampling time can be until $2n / f_{ref}$ long
- Sensitive to noise-peaks





u/f- Converter by the charge balancing method

I_0: Constant current source

$t < t_0$ ▷ u_x is integrated
Integration time is dependent on u_x

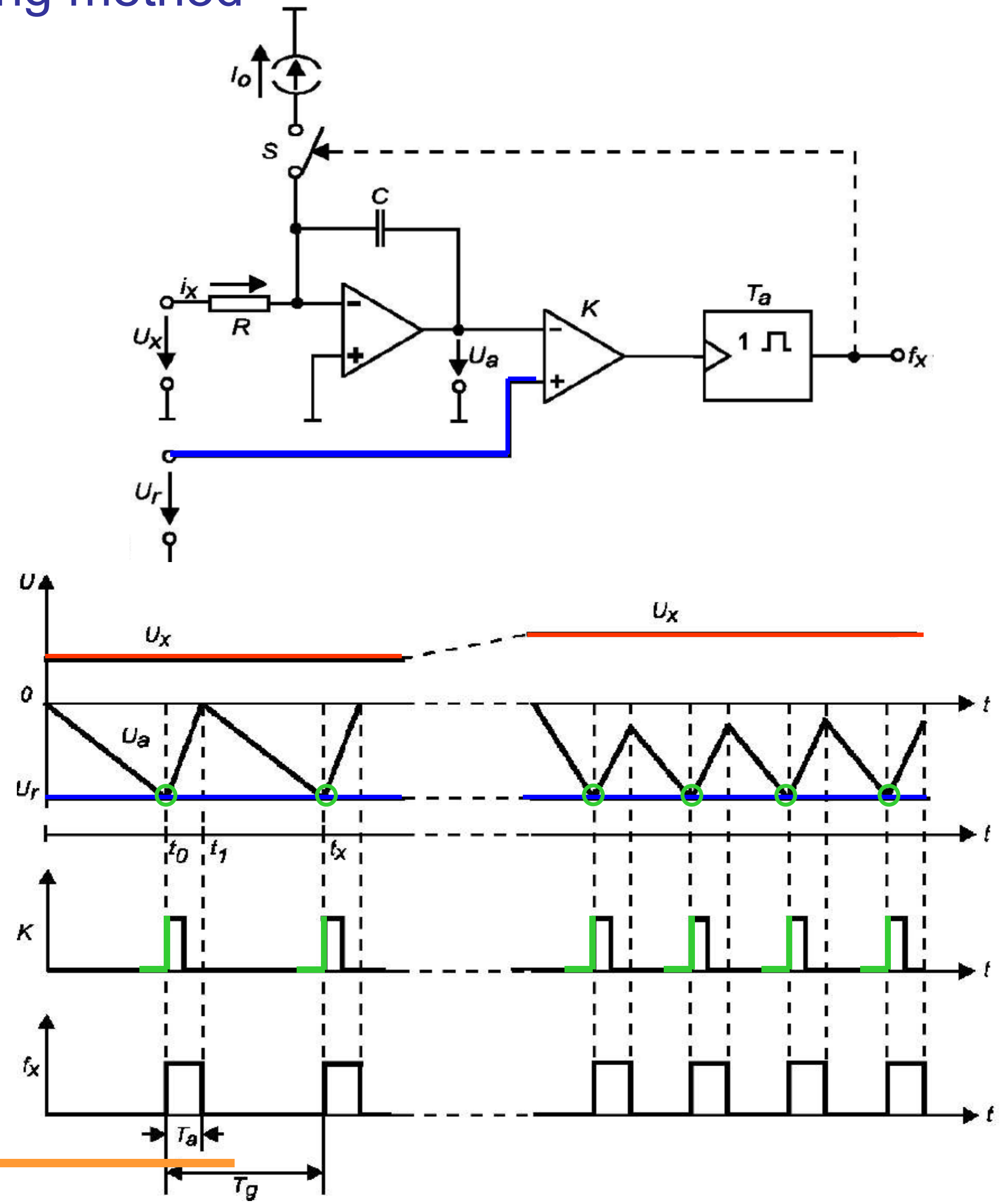
$t = t_0$ ▷ $U_a = U_r$

▷ mono-stable trigger circuit changes ist input during T_a

▷ Integration during T_a *(constant time intervall)*

T_g and f_g are the maesure for the voltage U_x

Discharging during current source is connected
→ Faster conversion



7.4 A/D-Converter with an Intermediate Quantity

u/t- Pulse Wide Converter

$$U_a = U_{a,\max} - \frac{1}{RC}\int_0^t U_0 \cdot dt = U_{a,\max} - \frac{U_0 \cdot t}{RC}$$

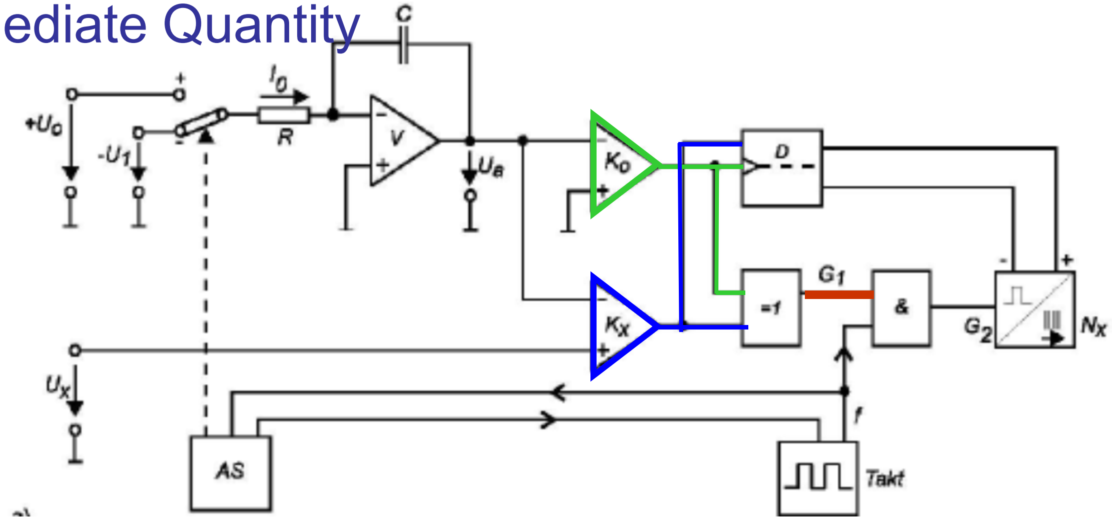
$$U_a(t_3) = 0$$

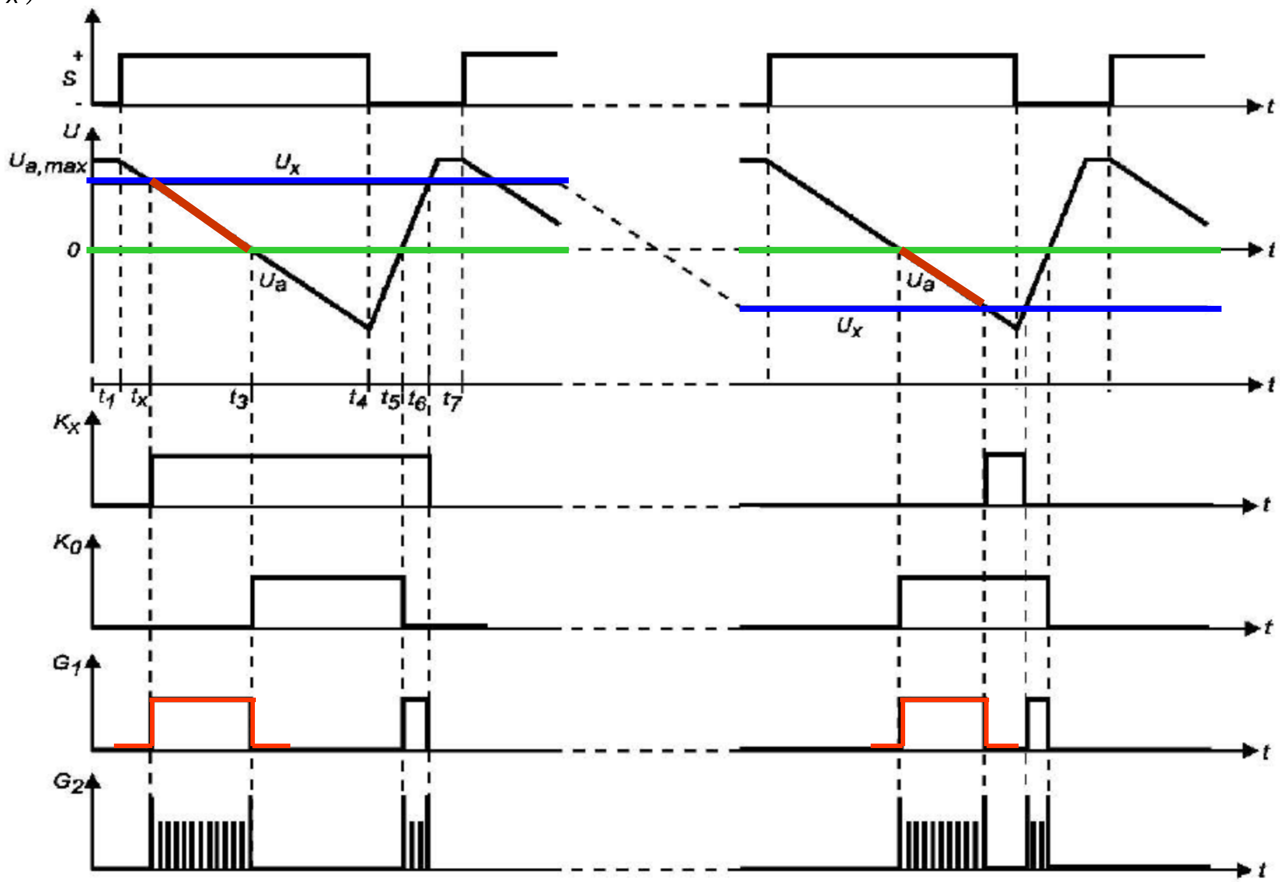
$$U_a(t_x) = U_x$$

$$= U_{a,\max} - \frac{U_0 \cdot t_x}{RC} = \frac{U_0}{RC}(t_3 - t_x)$$

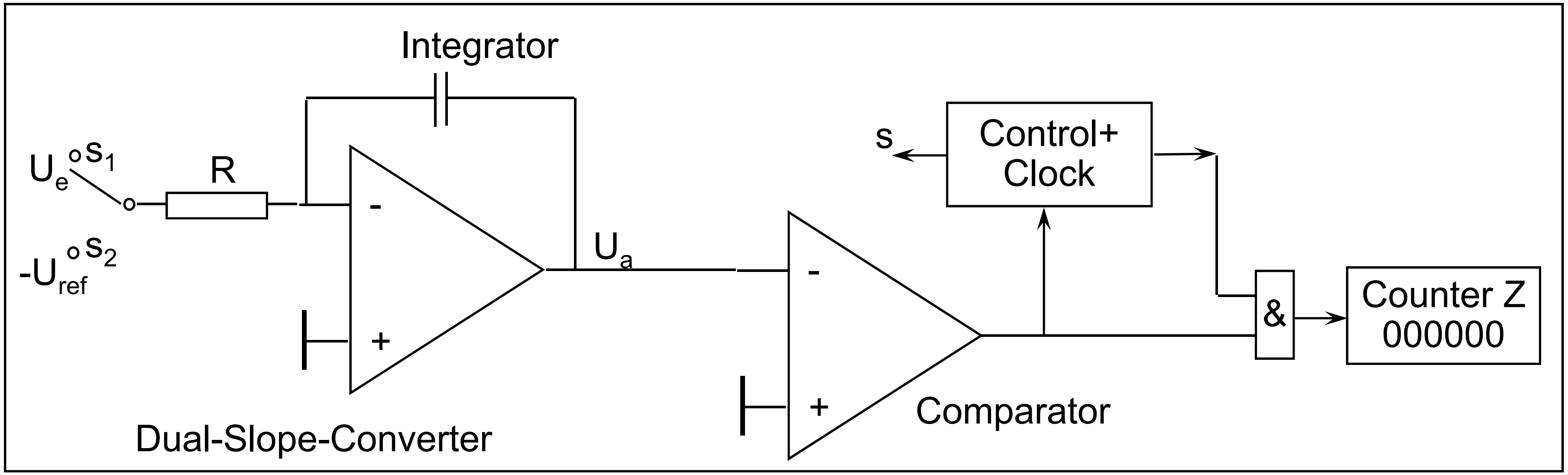
$$(t_3 - t_x) = \frac{U_x \cdot RC}{U_0} = \frac{N_x}{f}$$

$$\boxed{U_x = \frac{U_0}{RC}\frac{N_x}{f}}$$



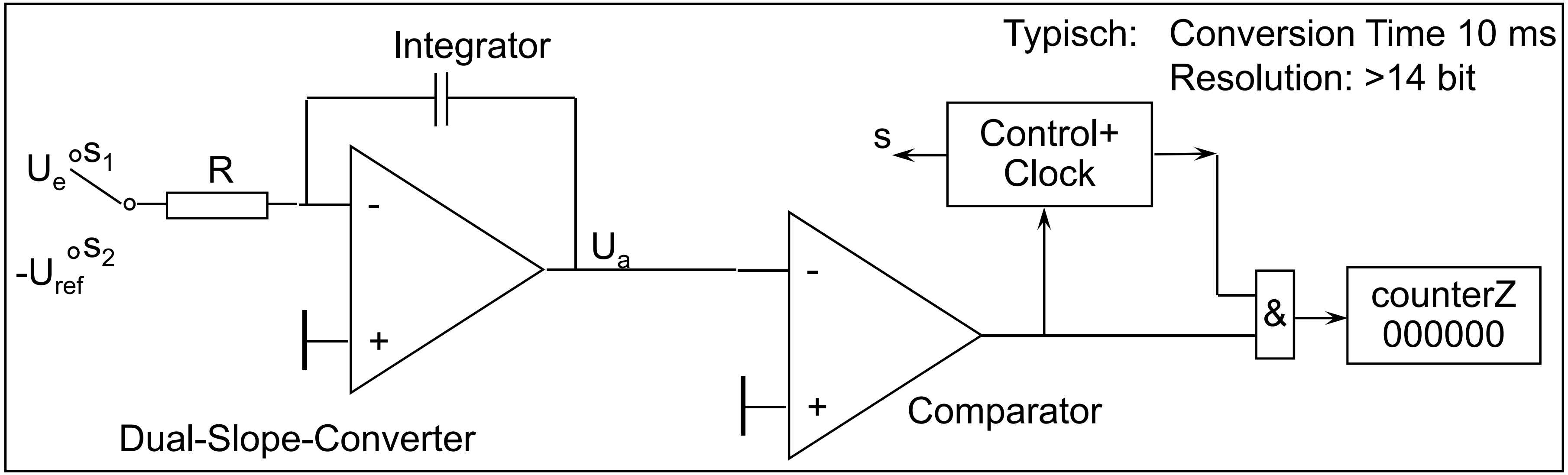


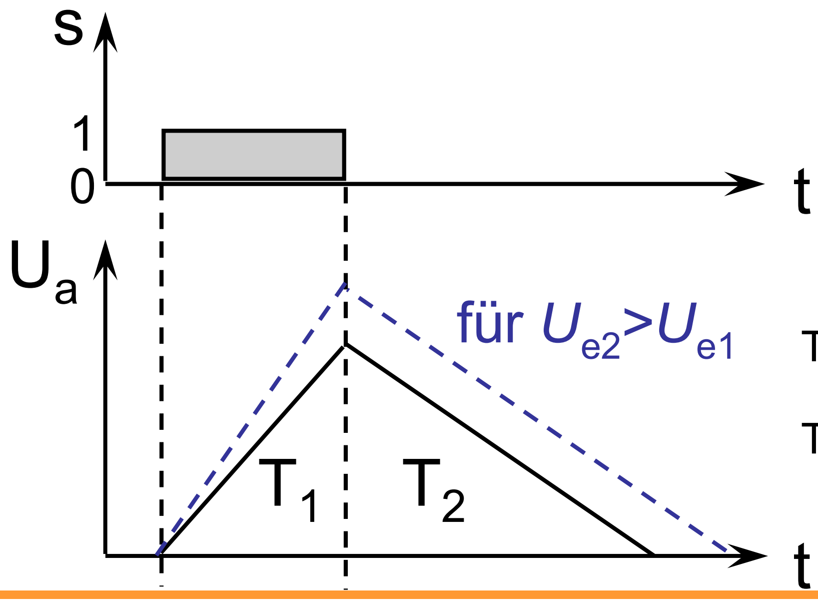
7.4 A/D-Converter with an Intermediate Quantity
Dual Slope Voltage-Time -Converter



- First, U_e is integrated during the given Time intervall T_1, than U_a is desintgrated through Integration of $-U_{ref}$ by 0
- Is U_a=0 reached, the counting is stopped
- The time intervall T1 is well known but independent on U_e
- The time intervall T_2 of the desintegration is proportional to U_e

7.4 A/D-Converter with an Intermediate Quantity
Dual Slope Voltage-Time -Converter

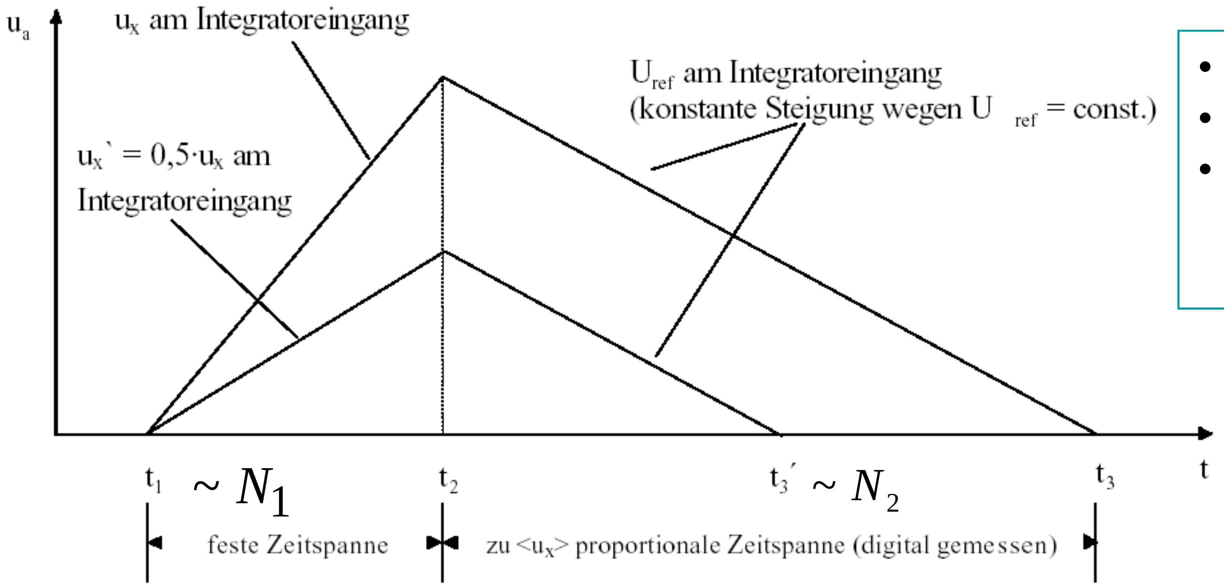




T_1(given):
Integrator charges the capacitance (counter N_1)

T_2(whilst $U_a>0$) :
Integrator discharges capacitance; (counter N_2)

7.4 A/D-Converter with an Intermediate Quantity
Dual Slope Voltage Time Converter



- Very high resolution
- Slow (typ. f_{Tast} a few10 Hz)
- Not sensitive to drift (clock, RC,...) and to noise (because of integration)

$$U_a(t_3) = -\frac{1}{RC}\left[\int_{t_1}^{t_2} u_x \, dt - \int_{t_2}^{t_3} U_{ref} \, dt\right] = 0$$

$$\Rightarrow u_x(t_2 - t_1) - U_{ref}(t_3 - t_2) = 0$$

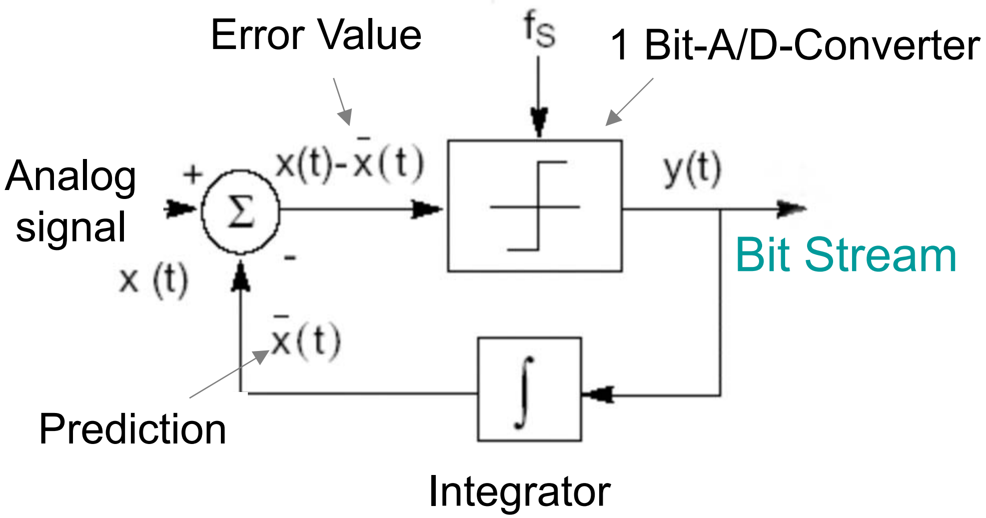
$$\Rightarrow u_x N_1 - U_{ref} N_2 = 0$$

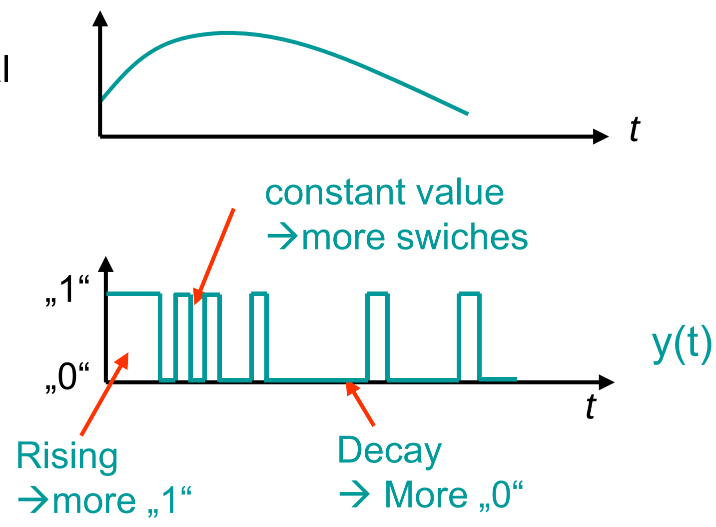
$$u_x = U_{ref} \frac{N_2}{N_1}$$

The precision is only dependent on U_{ref}!

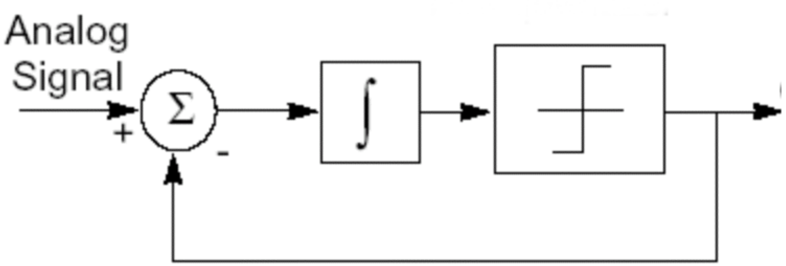
7.5 Sigma-Delta-Converter

1 Bit-Delta-Modulator



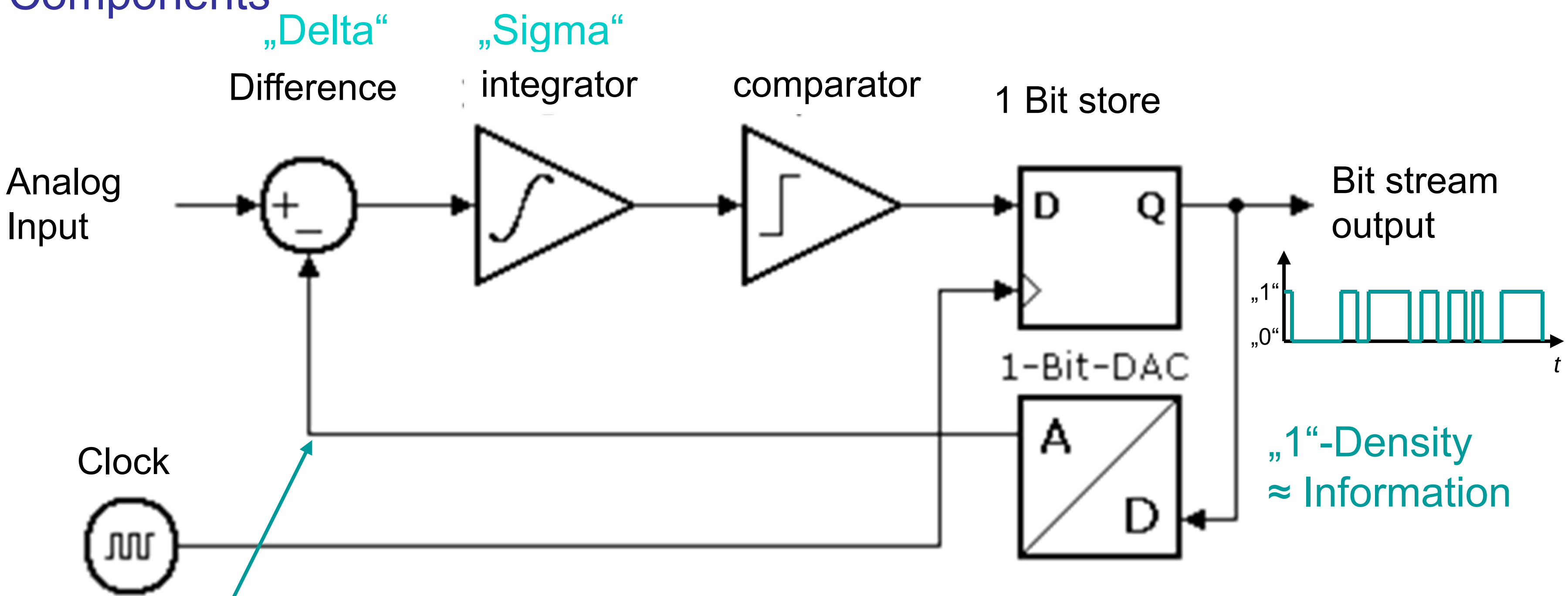


1 Bit-Sigma-Delta-Modulator (Smoothed Version of the Delta-Modulator)



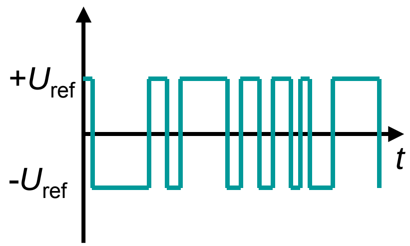
7.5 Sigma-Delta-Converter

Components



Mean value (Bit stream) = Mean Value (Signal) = Mean Value (Feed Back)

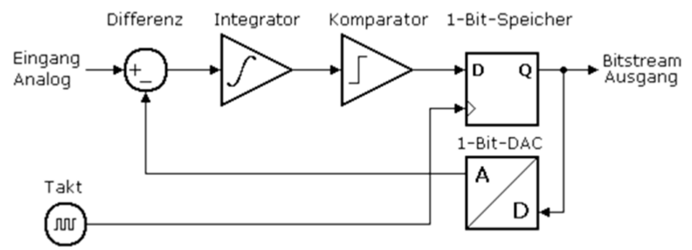
$$2U_{ref} \cdot Bitstream - U_{ref}$$



Properties

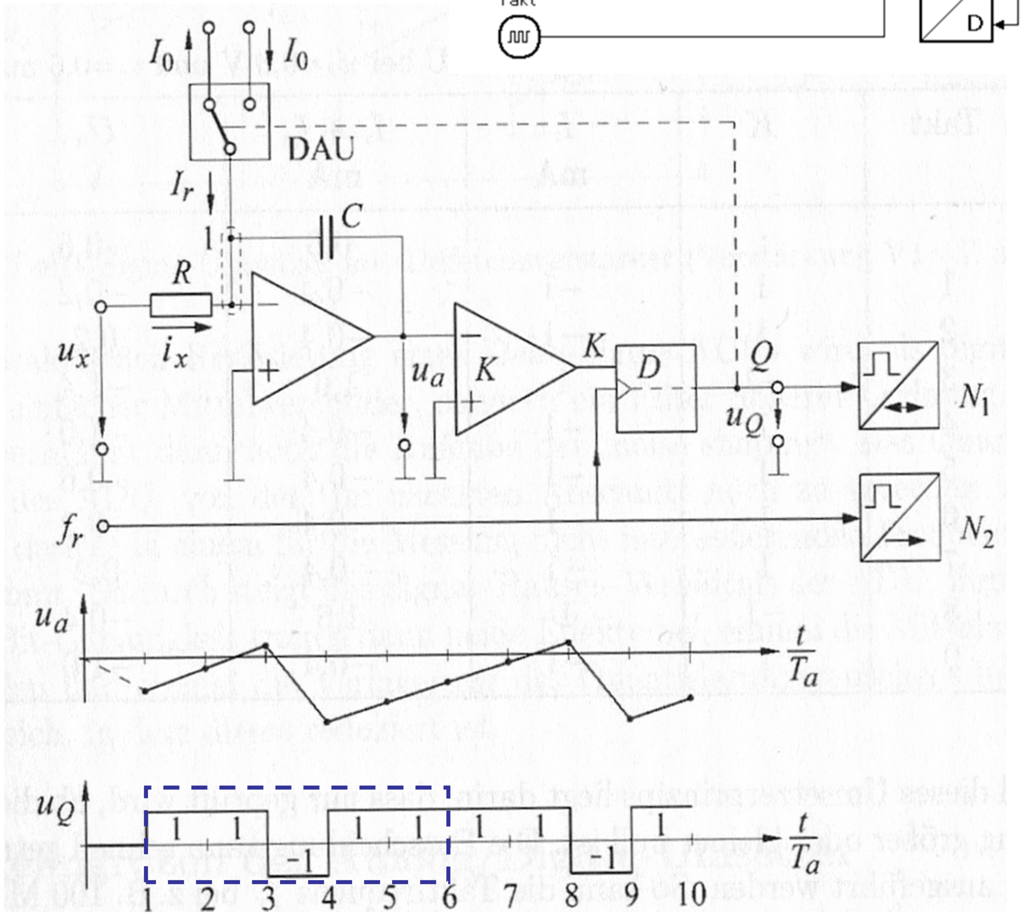
- Sampling frequency typ. 100 kHz
  Oversampling: $f_a >> f_{smax}$
- Typ. 10-24 Bit resolution
- Application in audio technology

7.5 Sigma-Delta-Converter
Possible Realisation



$U_a > 0 \quad K = -1 \quad I_r = +I_0$

$U_a \leq 0 \quad K = +1 \quad I_r = -I_0$



1 Word

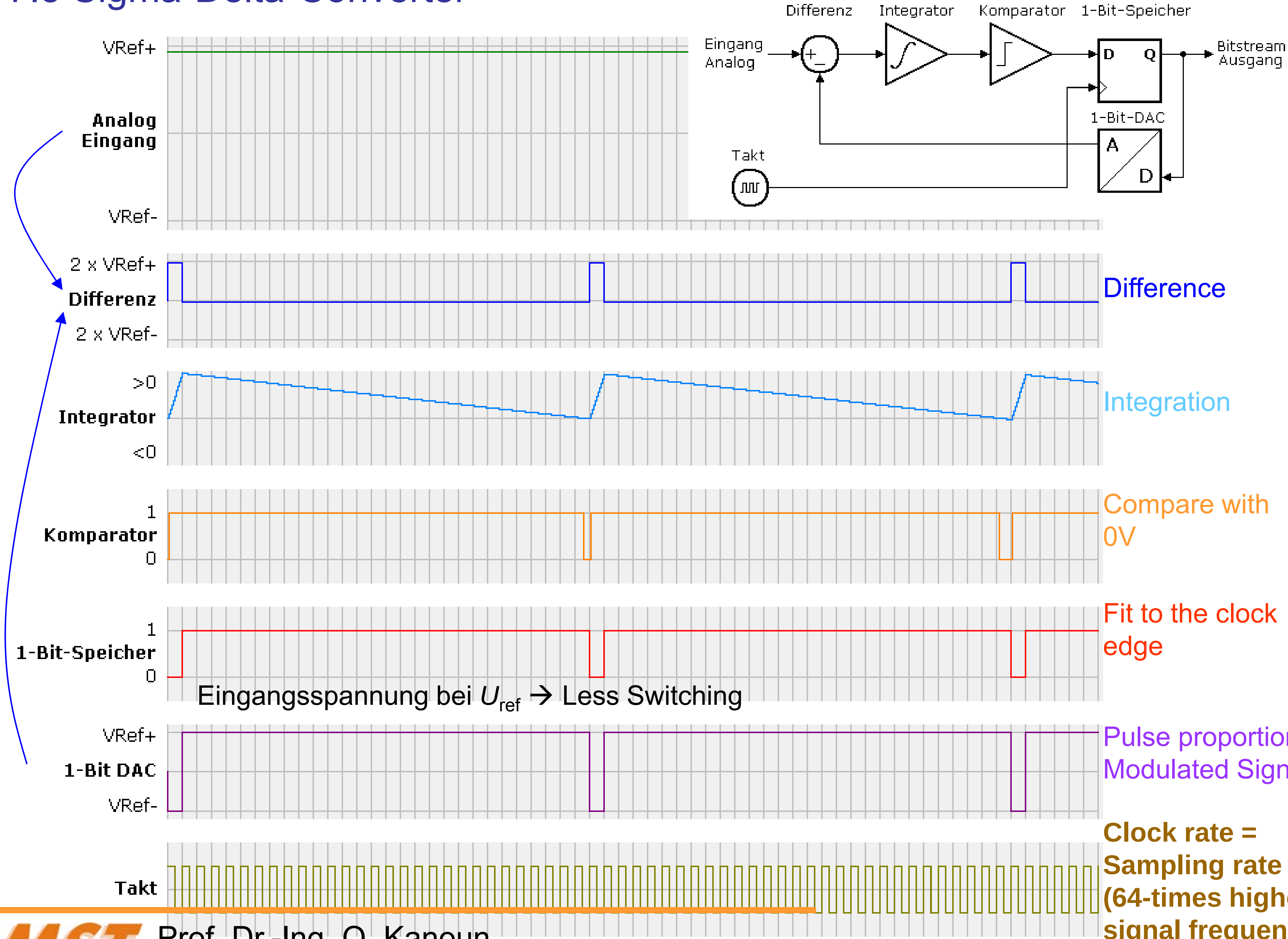
$$U_a = -\frac{1}{C}\left(i_x + i_r\right)\cdot T_0$$

$$U_x = \frac{N_1}{N_2} U_M = \frac{4}{5}\cdot 1V = 0{,}8\,V$$

[Schrüfer]

Typical: Conversion Time 1 ms
Resolution: >16 bit

7.5 Sigma-Delta-Converter



Eingangsspannung bei U_{ref} → Less Switching

Difference

Integration

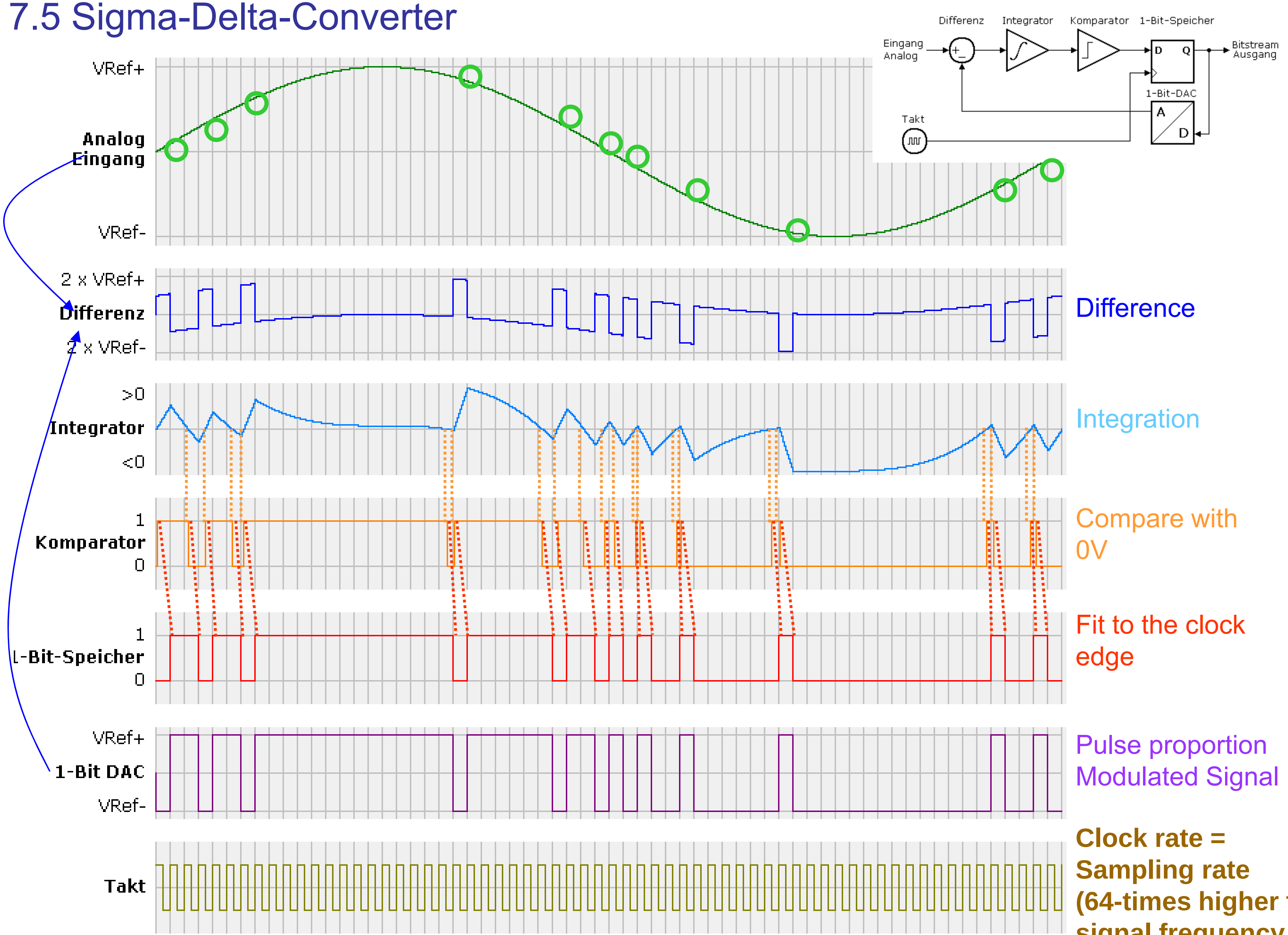
Compare with 0V

Fit to the clock edge

Pulse proportion Modulated Signal

Clock rate = Sampling rate (64-times higher than signal frequency

7.5 Sigma-Delta-Converter



Difference

Integration

Compare with 0V

Fit to the clock edge

Pulse proportion Modulated Signal

Clock rate = Sampling rate (64-times higher than signal frequency

http://www.beis.de/Elektronik/DeltaSigma/DeltaSigma_D.html

Digital Decimation from Bit Stream

(Down Sampling, reducing the number of samples in a discrete-time signal)

1
0
1
0
0
1
0
1
1
0
0
0
1
0
1

Input:16 1Bit-Values

Reducing the sampling points
➔ increasing resolution

$$\xrightarrow[\text{decimation}]{16:1} \frac{7}{16} = 0{,}4375 = 0111$$

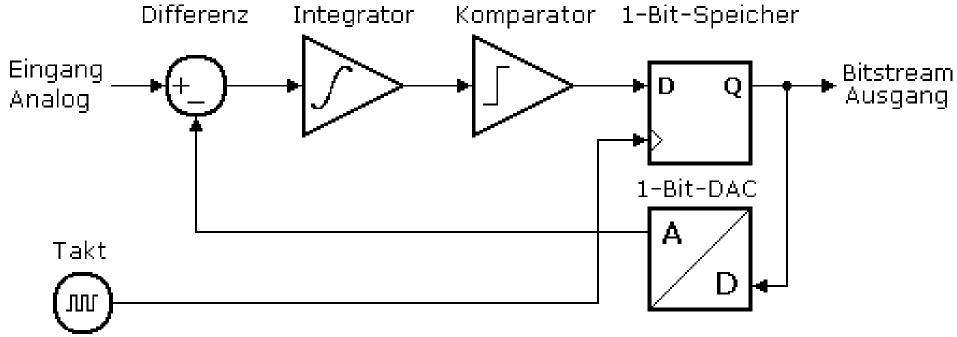
Mean value

Output : 4Bit-Value

Mean Value of the bit stream corresponds to:
Input signal overlapped with disturbing signals

The more bit stream pulses are used the more precise is the mean value
→ Oversampling is necessary

7.5 Sigma-Delta-Converter

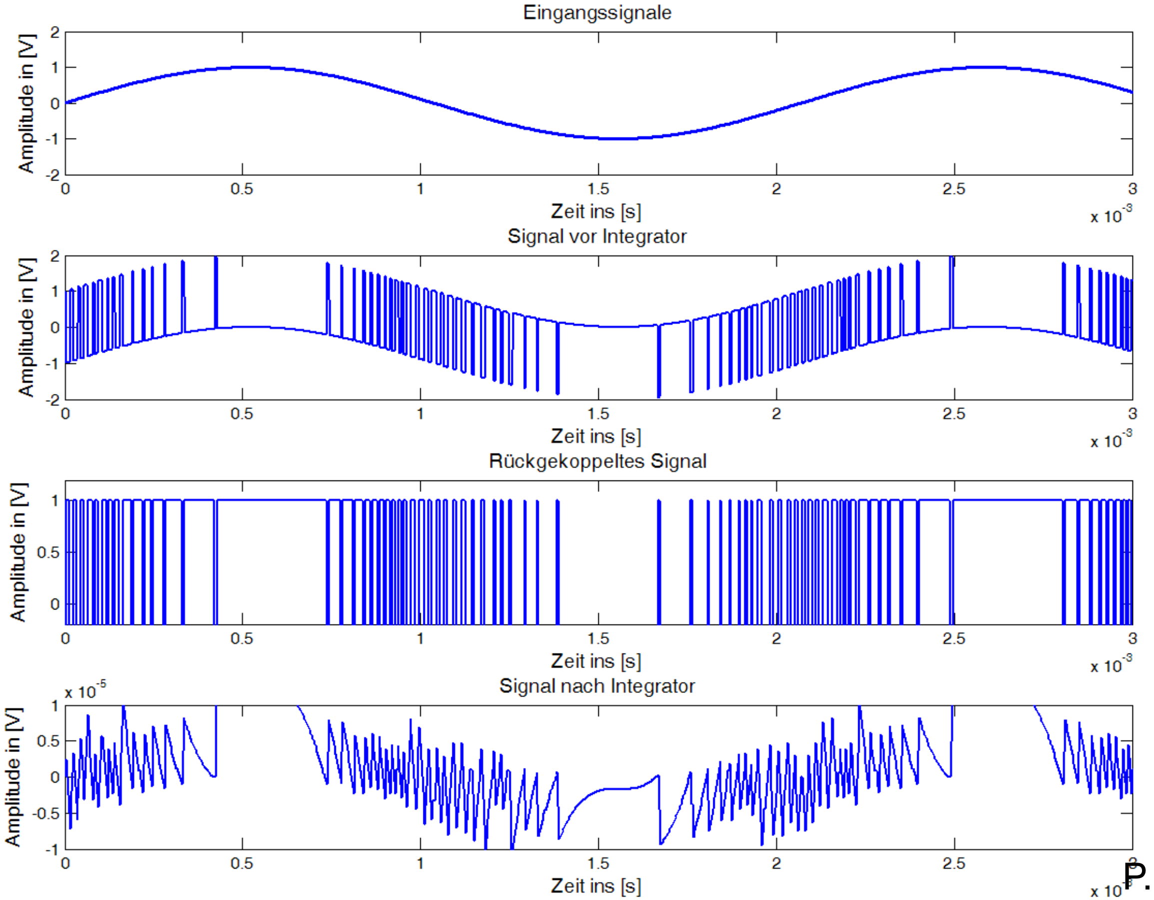


Input Signal

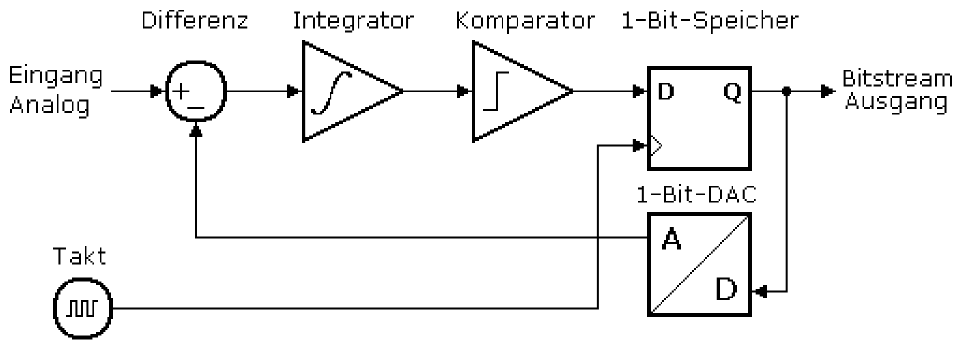
Input Signal –
Feedback Signal

Feedback Signal

Integrator Output Signal



7.5 Sigma-Delta-Converter



Comparator

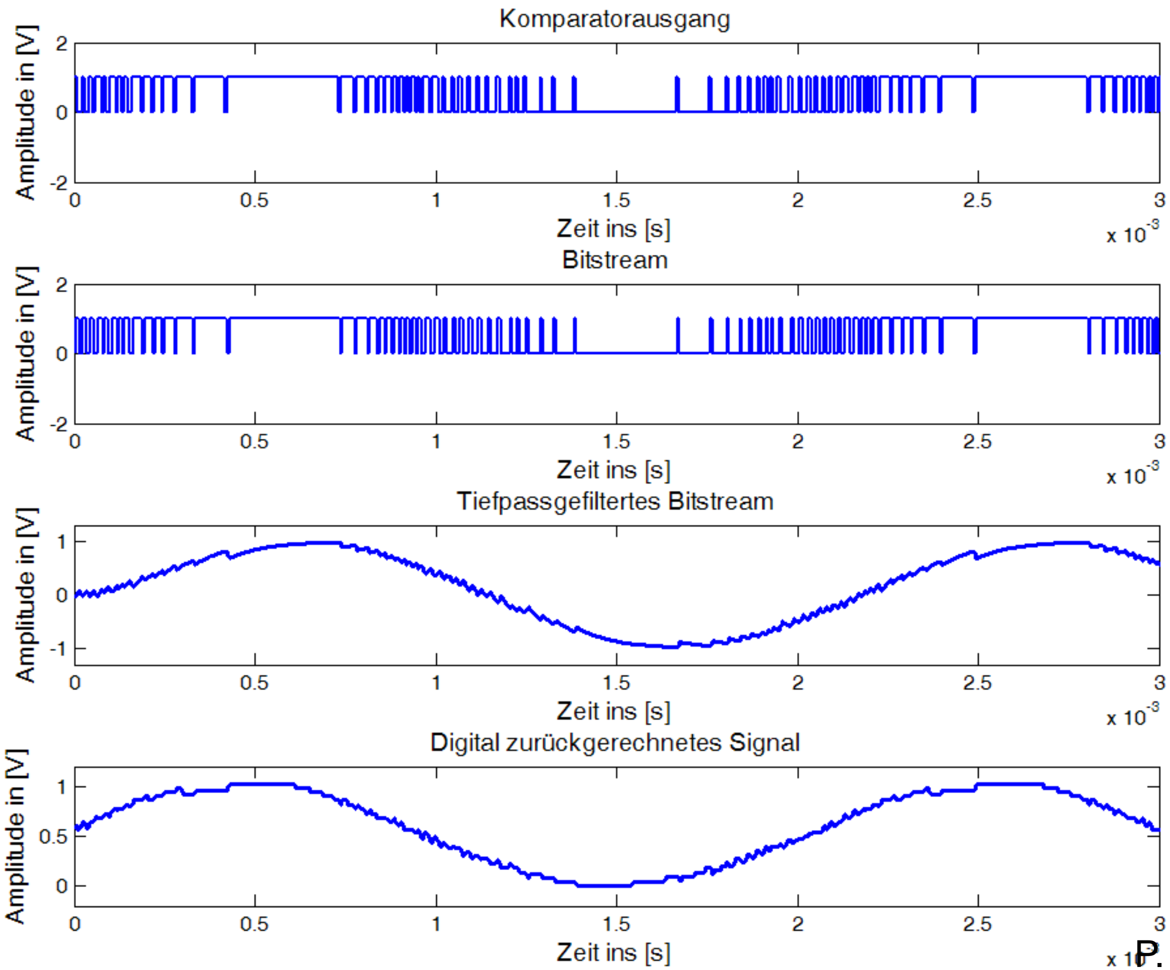
Bit Stream

Low Pass Filtered Signal

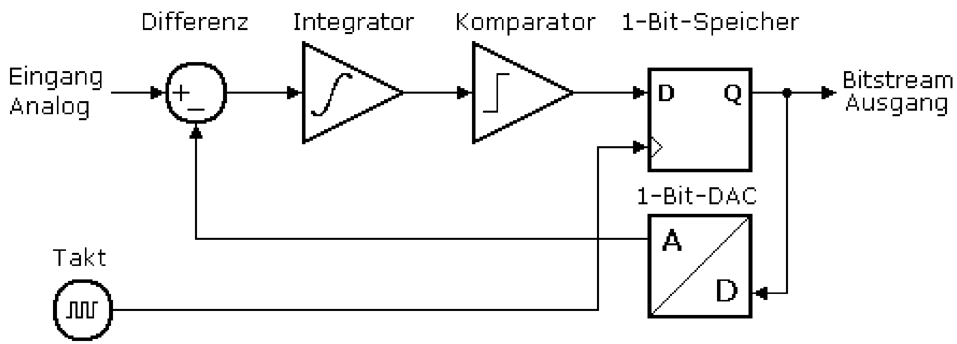
$$F(s) = \frac{\omega_g}{s + \omega_g}$$

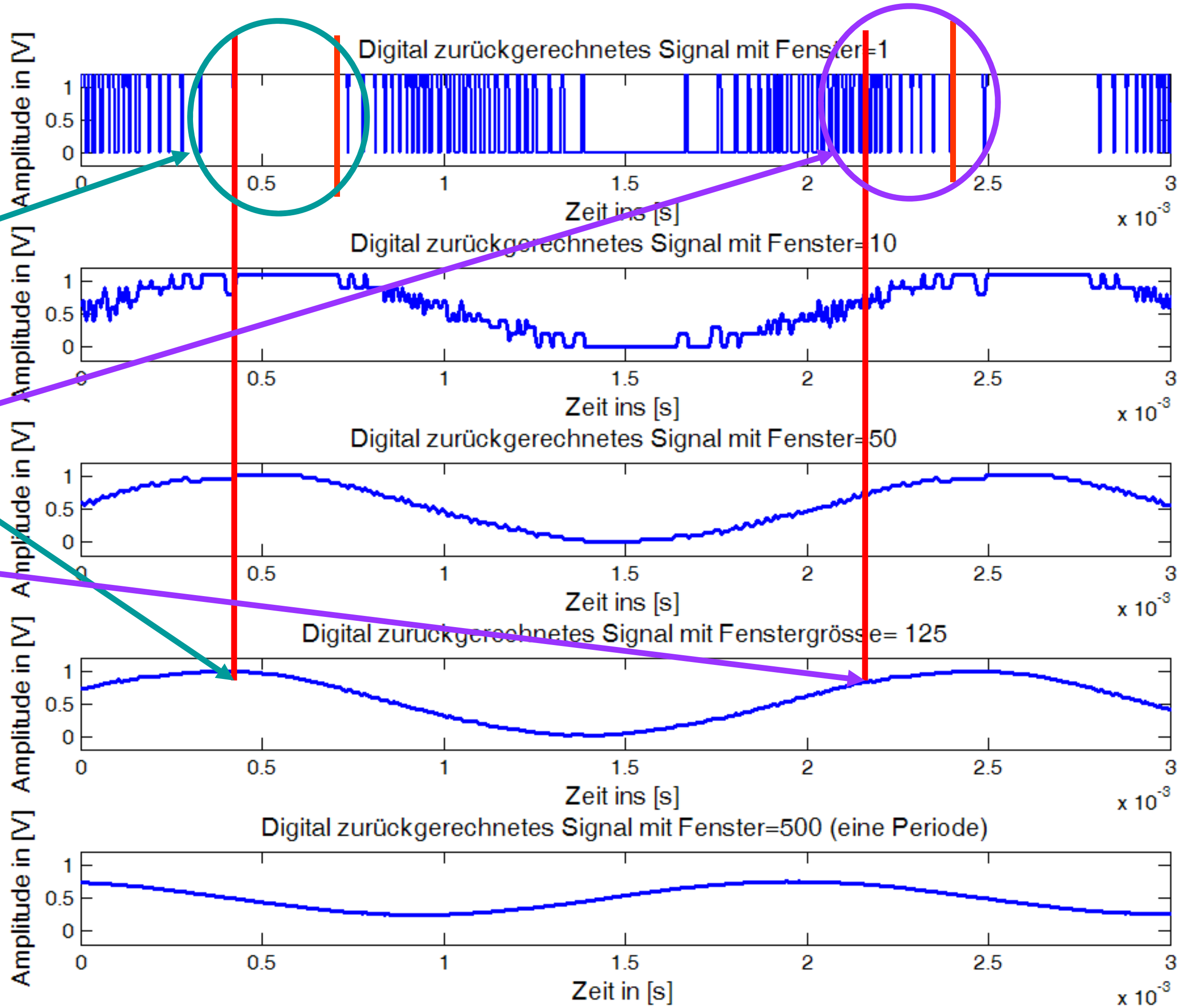
Digital Low Pass Filter:

$$U(t) = U_{ref} \cdot \frac{N_1}{N_{gesamt}}$$



7.5 Sigma-Delta-Converter





Example. Window 1

$$0.96 = 1 \cdot \frac{120}{125}$$

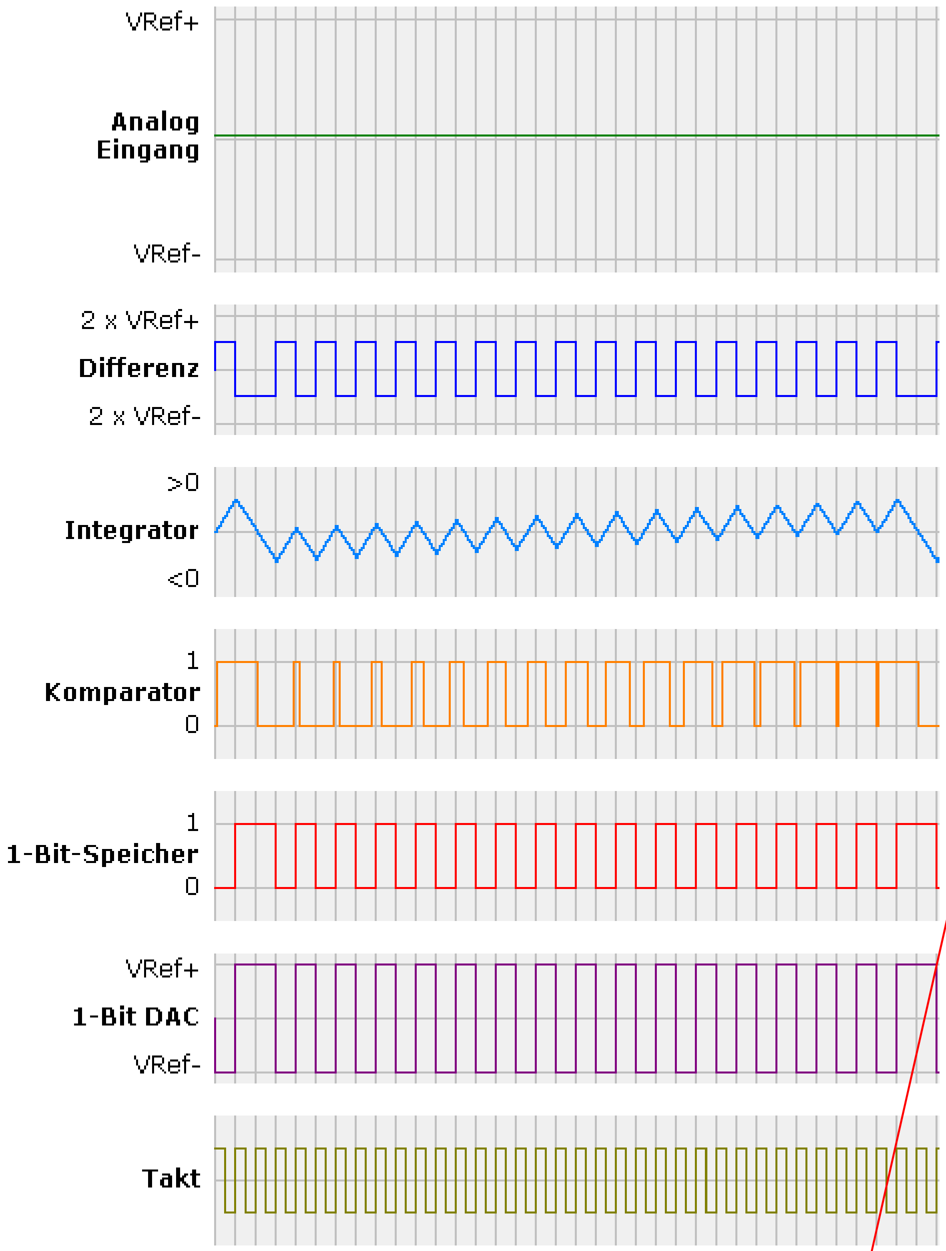
Example. Window 2

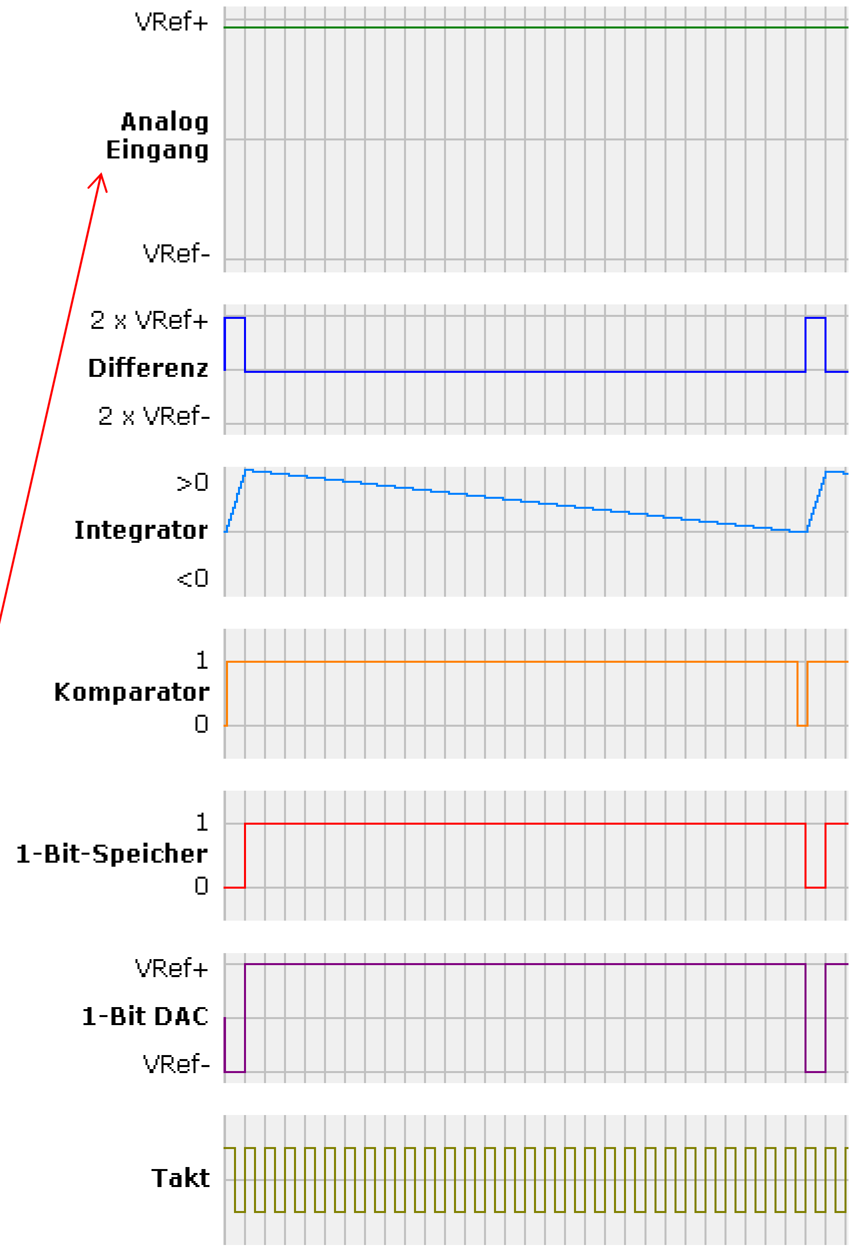
$$0.75 = 1 \cdot \frac{94}{125}$$

The bigger the window is, the smaller the limit frequency of the digital Low Pass

→ Mean Value

→ Phase Shift



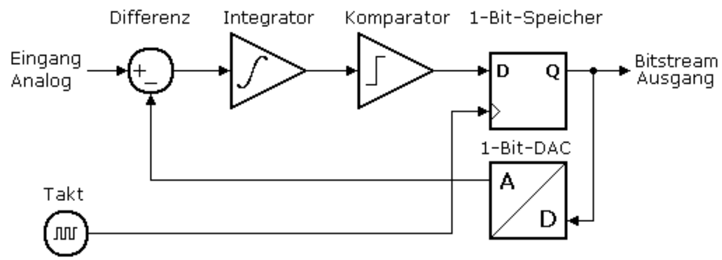


High Signal Value

Frequency of the disturbing signals in the neighborhood of the signal frequency

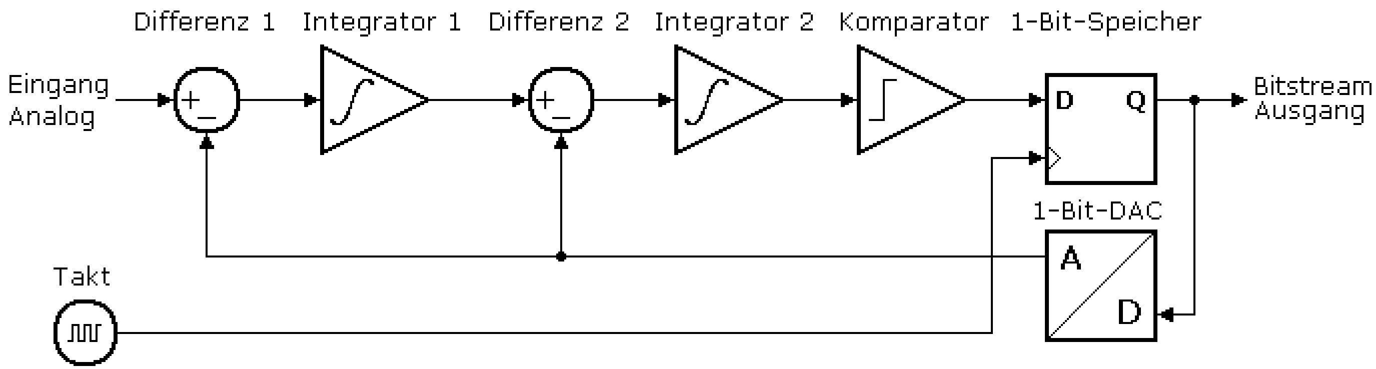
7.5 Sigma-Delta-Converter

1. Ordnung



Sigma-Delta-Converter 2. Order → Reducing disturbing signals

Not one after the other!



→ Signal band width can be higher
→ Clock rate kann be smaller
→ Accuracy of the output signal can be higher (less conversion noise)

http://www.beis.de/Elektronik/DeltaSigma/DeltaSigma_D.html

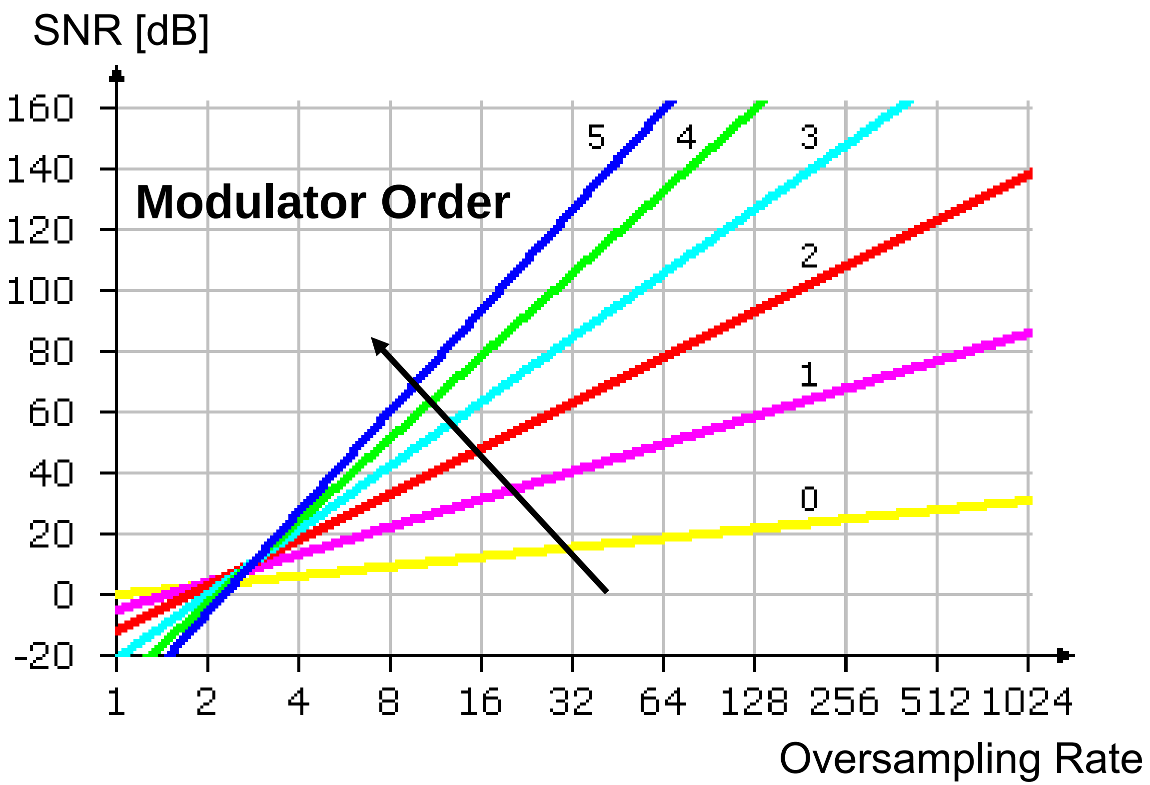
7.5 Sigma-Delta-Converter

Structure

Two Disturbations

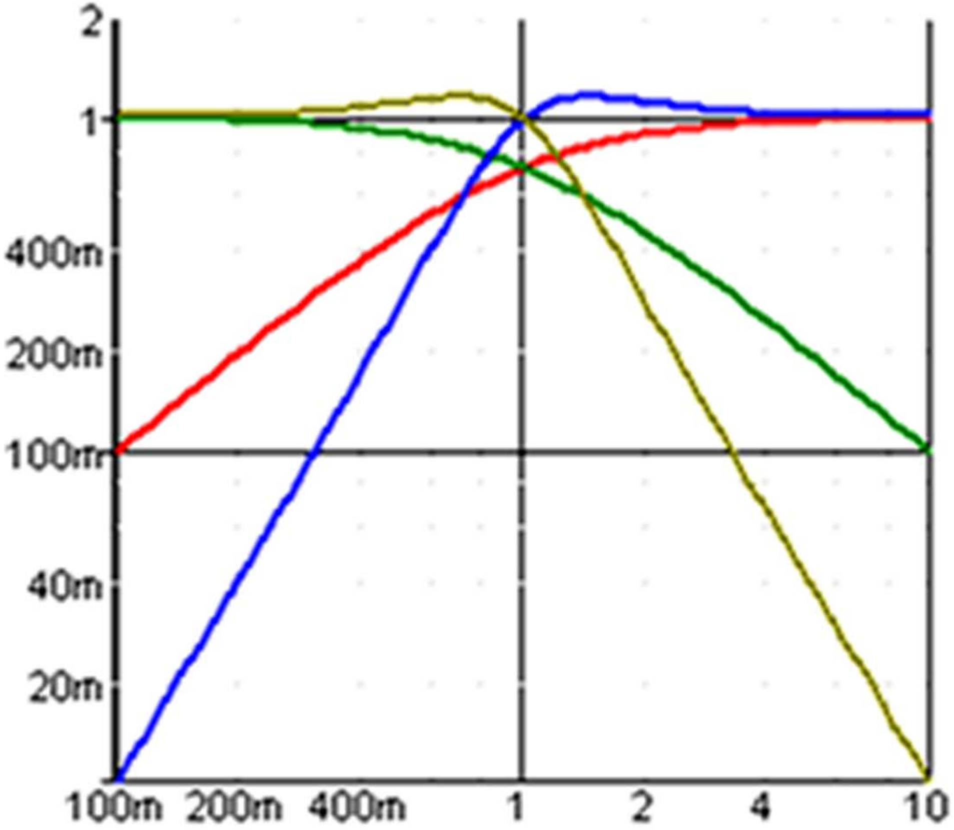
- Quantisation noise (Digitalisation)
- Conversion Noise (within the Bitstream) dependent on:
  - Order of the Sigma-Delta-Converter
  - Oversampling rate

7.5 Sigma-Delta-Converter
Conversion Noise



Typical:
24 Bit, Modulator third order with 64-Times Oversampling
(-160 dB Conversion Noise and -147 dB Quantisation Noise)

7.5 Sigma-Delta-Converter



First Order

- Disturbing Signal
- Usefull Signal

Second Order

- Disturbing Signal
- Usefull Signal

Lower Frequency Band

→ Desired input signals are transmitted

→ Disturbing signals are significantly reduced

→ For Modulators of a higher order disturbing signals are even better supressed ("**Noise Shaping**")

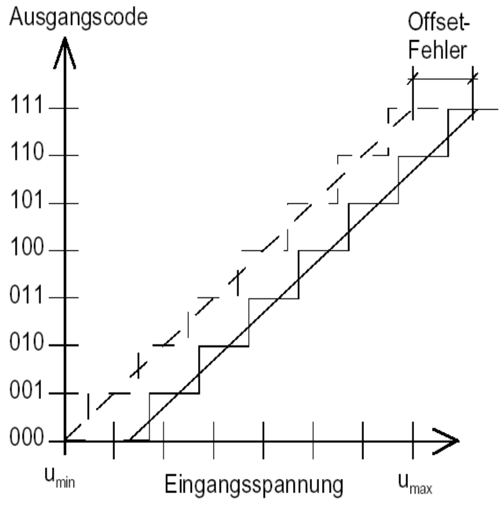
High Frequency

→ Signal is supressed

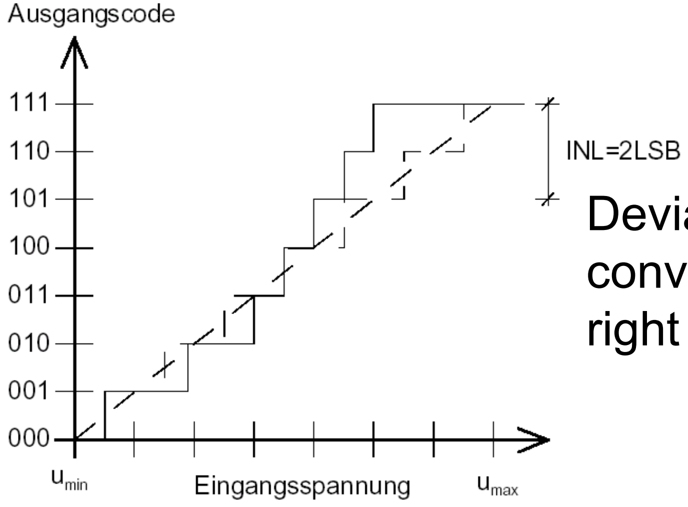
→ Distrubing Effects are amplified („Alias-Effekt")

7.6 errors by A/D-Converter

Offset-Error

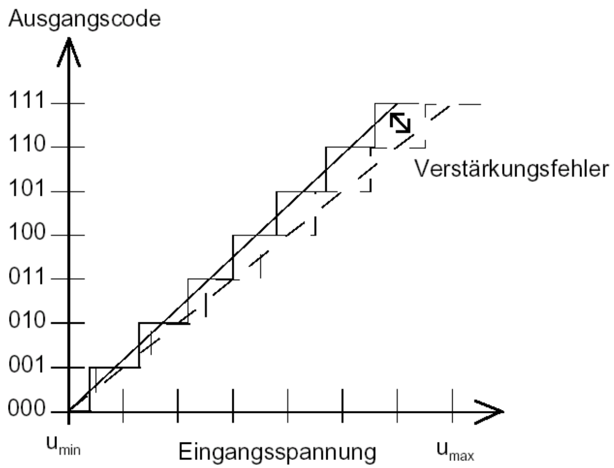


Integral Nonlinearity

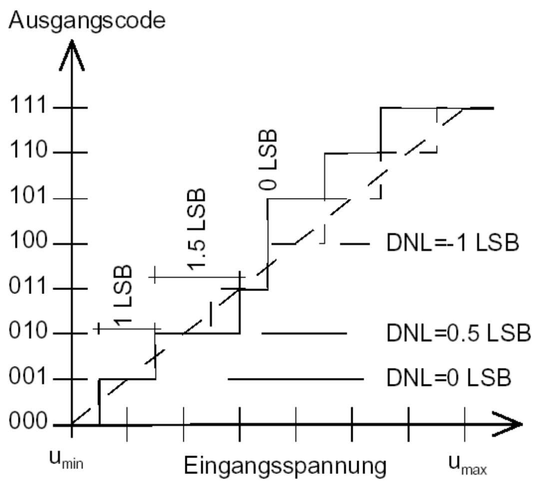


Deviation between converted value and the right value

Amplification Error



Differential Nonlinearity



Absolute Deviation of the width of the Quantisation Steps from Ideal Value 1 U_{LSB}

Overview A/D-Converter

	Flash Converter	Successive Approximation	Dual Slope	Sigma Delta
Main Advantages	Ultra-High Speed when power consumption not primary concern	Medium to high resolution (8 to 16bit), 5Msps and under, low power, small size.	high resolution, low power consumption, good noise performance	High resolution, low to medium speed, digital filter reduces anti-aliasing requirements.
Disadvantages	Metastability, high power consumption, large size, expensive.	Speed limited to ~5Msps. May require anti-aliasing filter.	Slow Conversion rate. High precision external components necessary	Higher order (4th order or higher) - multibit ADC and multibit feedback DAC.
Conversion Time	Ca. 10 ns-100ns Does not change with increased resolution.	Ca. 1 µs-100µs Increases linearly with increased resolution.	Ca. x ms Increases linearly with increased resolution.	Ca. 200 µs-2ms Tradeoff between data output rate and noise free resolution.
Typ. Resolution	4 bit 8 bit	8 bit 18 bit	12 bit 22 bit	16 bit 24 bit More bits?