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The picture of an oil tanker discharging oil into the sea exemplifies the irresponsibility of much of today's industry. In the past, the world could absorb such abuse with comparative ease since the greatest of man's enterprises amounted to little more than flea bites on its surface. The effects of pollution, however, are cumulative and our world is fast becoming very sick indeed. Environmental organizations have long recognized this and have spared no effort in alerting industry and the authorities to the disease, and to the need for responsible, concerted action before the disease becomes terminal. Heavy industry, nuclear power and motor vehicles are the main targets of these groups but that doesn't mean that other areas can afford to relax. The electronic-components industry too, can play its part in helping to clean up our world. Already much effort has gone into reducing the use of toxic materials in electronic components, and into developing environmentally-friendly packing materials. Maybe the world can never regain its pre-industrial purity, but we should at least ensure that our children's legacy is a viable one.

Contents

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Analog multi-standard colour decoder ICs TDA4650 and TDA4660

ECKHARD BRUNS, KLAUS JUHNKE

In Europe, in particular, there are many areas where TV transmissions of more than one colour transmission standard can be received. Multi-standard colour decoding is also an essential part of satellite TV reception and has been considerably extended by the requirements of the VCR, S-VHS standard. To satisfy the resulting demand for multi-standard TV colour decoders, we introduced the TDA4555/57 in the early 1980s. These ICs have been extremely successful and have been in mass production for nearly a decade. However, recent advances in switched-capacitor technology have now enabled us to replace the discrete glass delay line by integrated baseband delay line filters. The TDA4650 retains all the features of the TDA4555/57 which have been so successful, but is adapted to operate together with the switched-capacitor baseband delay line filters of the TDA4660.

It is essential for the multi-standard colour decoder to identify accurately and quickly the TV colour standard of the input signal for both CVBS signals and the separate luminance and chrominance components in S-VHS format from a VCR. It is equally essential to integrate as many of the functions of the multi-standard colour decoder as possible. Also, this multi-standard colour decoder is based on a line-locked clock, so its output colour-difference signals can be processed by a feature module to provide memory-based features (e.g. picture-in-picture, 100/120 Hz displays).

The baseband delay lines use CMOS switched-capacitor technology, based on serial sampling of the baseband colour-difference signals at a line-locked clock frequency. Delaying the baseband colour-difference signals by exactly one line and adding the non-delayed colour-difference signal provides comb filtering with a frequency response which is periodic in the line frequency. The comb filter maxima are integer multiples of the line frequency, the minima are at successive half multiples of the line frequency.

Multi-standard colour decoding with baseband delay lines has the following advantages:

- there are no delay line coils and potentiometer and therefore, no delay line adjustments
- the circuit configuration of the baseband delay line is the same for all colour transmission standards
- cross colour interference is reduced for NTSC colour signals due to the comb filters
- the possibility of crosstalk between the FM SECAM colour carriers (diaphoty) is eliminated.

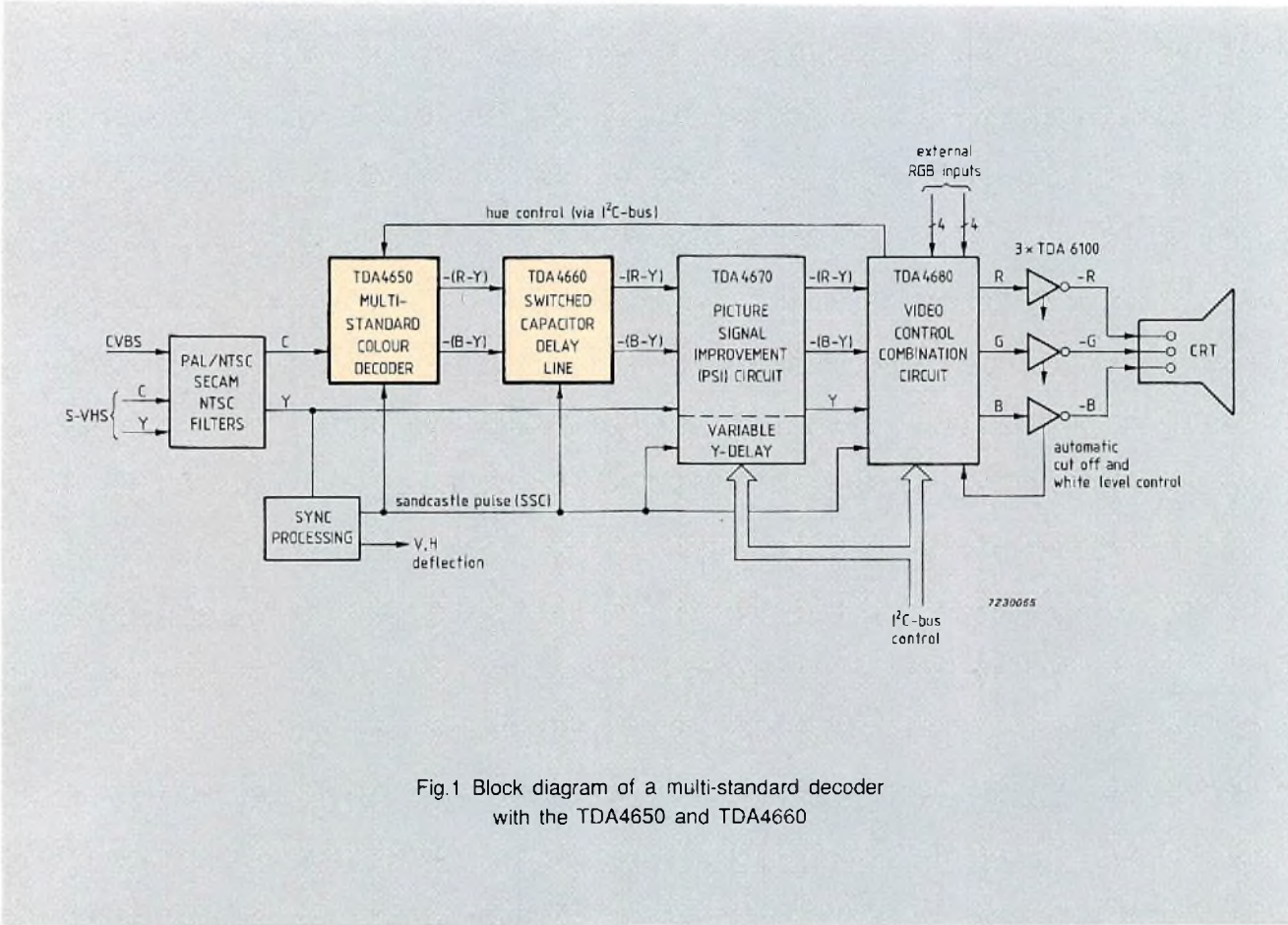


Fig.1 Block diagram of a multi-standard decoder with the TDA4650 and TDA4660

The TDA4650 and the TDA4660 are complementary in their function, therefore, the TDA4650 provides colour-difference signal outputs to the TDA4660 at pre-defined voltage levels, see Fig.1. The TDA4650, Multi-standard Colour Decoder performs colour transmission standard identification and multi-standard chrominance signal control and demodulation. The TDA4660, Switched Capacitor Delay Line, contains the two line-locked comb filters for an integrated multi-standard colour decoder. The TDA4660 can, however, be used with any colour decoder as a baseband colour-difference signal filter.

The colour-difference output signals from the TDA4660 are compatible with the TDA4670 Picture Signal Improvement (PSI) Circuit and the TDA4680 Video Control Combination Circuit. Both the TDA4670 and the TDA4680 incorporate I²C-bus control for display signal processing and control, the TDA4680 can select two external RGB inputs (e.g. peritelevision connector, teletext, etc.). The super sandcastle pulse (SSC) synchronizes colour decoding, luminance and colour-difference signal processing and correlates the RGB colour signals with the raster.

COLOUR TRANSMISSION STANDARD IDENTIFICATION

Colour transmission standard identification consists of an automatic control and scanning sequence with identification circuits which identify the transmitted colour standard, see Fig.2. The automatic control and scanning sequence sets the mode of the TDA4650 sequentially to PAL, SECAM, NTSC-M and NTSC-4.4. The outputs from the TV standard scanning circuits not only establish the internal mode of the Multi-standard Colour Decoder but also select the appropriate external PAL/NTSC SECAM NTSC filter (via the voltages on pins 25 to 28). The TDA4650 interrogates the chrominance signal by comparison with the characteristics of the chrominance signals of the different colour transmission standards in sequence. When a transmission conforming to a colour transmission standard is identified by the identification circuits, the mode of the TDA4650 is automatically selected.

The TDA4650 can decode colour signals which are defined according to the following transmission standards:

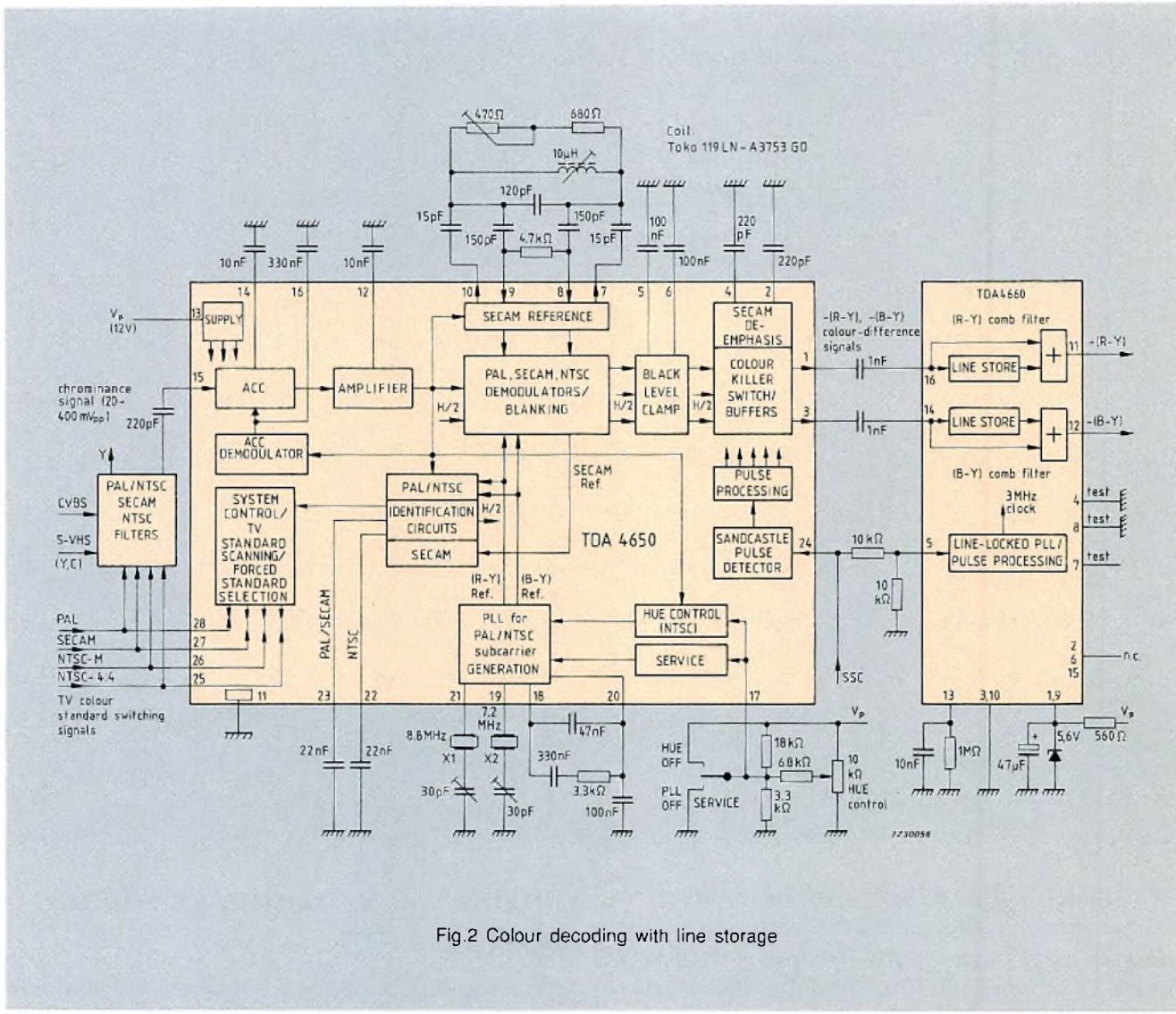


Fig.2 Colour decoding with line storage

- **QAM (Quadrature Amplitude Modulation)** of the colour carrier by the colour-difference signals.
  - **standard NTSC**, NTSC-M (f_{sc} = 3.579545 MHz) referred to as NTSC-3.5.
  - **non-standard NTSC**, with $f_{sc} = f_{sc}(PAL)$ = 4.43361875 MHz. This colour transmission standard is used in the Near East and is referred to as NTSC-4.4. As the colour carrier frequency is the same as that of the PAL-B, G, H, I standards, the same crystal oscillator is used to generate the reference frequency for both.
  - **PAL**, characterized by the phase reversal of the (R–Y) colour-difference signal on alternate scan lines. PAL-B, G, H, I: colour carrier frequency f_{sc} = 4.43361875 MHz. PAL-M: colour carrier frequency f_{sc} = 3.57561149 MHz. PAL-N: colour carrier frequency f_{sc} = 3.58205625 MHz.
- **SECAM**, characterized by transmission of the (R–Y) and (B–Y) colour-difference signals on alternate scan lines and frequency modulation of the colour carriers. The frequency of the colour-difference signals may vary between 3.900 and 4.756 MHz. The frequencies of the no-colour carriers are:
  f_o (B–Y) = 4.250 MHz,
  f_o (R–Y) = 4.40625 MHz.

Control And Scanning Sequence

The automatic control and scanning sequence determines the mode of the TDA4650 selected by the colour transmission standard scanning and system control circuits. These circuits switch the mode sequentially to the PAL, SECAM, NTSC-M and NTSC-4,4 standards,

each for a duration of four field periods (80 ms). This time interval is a good compromise between the stabilization of the chrominance signal at the input to the identification circuits and the suppression of the noise content of the chrominance signal. If the current chrominance signal is not identified, the control and scanning sequence selects the mode of the next colour transmission standard so that the chrominance signal is always identified within 320 ms. This time is increased by two field periods (colour switch-on delay) to 360 ms, at which time the colour-difference signals are enabled.

To provide reliable SECAM chrominance signal identification under all conditions, e.g. for SECAM-PAL transcoded signals, or when PAL chrominance signals are distorted by reflection, the control and scanning sequence includes PAL priority switching. The PAL priority circuit switches the Multi-standard Colour Decoder to the PAL mode after a SECAM chrominance signal is first identified. If a PAL chrominance signal is not identified during the following scanning period, the Multi-standard Colour Decoder reverts to the SECAM mode for a second identification. The PAL priority circuit increases the maximum identification time together with the colour switch-on delay to 520 ms (this is a worst-case condition, assuming, for example, that a SECAM chrominance signal exists but the control and scanning sequence starts in the NTSC-M mode). A further precaution for reliable SECAM identification is to identify the SECAM chrominance signal at 50 Hz only. An NTSC chrominance signal (60 Hz) can therefore, never be identified as a SECAM chrominance signal.

If no colour transmission standard is identified, as with black and white transmissions, or an unprepared colour transmission standard exists, the control and scanning sequence scans continuously. The colour decoding remains switched off until a subsequent chrominance signal is identified. If, due to interference, the established colour transmission standard is temporarily not identified, a delay of two field periods is included to prevent the immediate start of the control and scanning sequence.

During the control and scanning sequence, the amplitude of the colour transmission standard switching signals on pins 25 to 28 is approximately +2.5 V. When a colour transmission standard is identified, the amplitude of the associated switching signal rises to typically +5.8 V and the other switching signals are set to less than 0.5 V. The switching signal is used to select the appropriate chrominance filter and chrominance trap of the PAL/NTSC SECAM NTSC filters. If an external voltage greater than +9 V is applied to one of pins 25 to 28, then this forces the selection of PAL, SECAM, NTSC-M or NTSC-4.4. Forced standard selection overrides the colour transmission standard identification. The automatic colour-killer switch still operates with forced standard selection.

The TDA4650 requires a 3-level super sandcastle pulse (SSC) to generate all the necessary internal timing pulses. The sandcastle pulse amplitudes are >7.7 V for the burst key pulses, 4.5 ±0.4 V for the horizontal blanking pulses and 2.5 ±0.5 V for the vertical blanking pulses. Level detector circuits separate the three components of the sandcastle pulse from which the pulse processing circuits generate the required internal timing and clamping pulses.

Colour Transmission Standard Identification Circuits

The colour transmission standard identification circuits compare the mode of the Multi-standard Colour Decoder with the input chrominance signal, the result of this comparison determines the colour transmission standard. The identification circuits examine the nature of the signals present during the back porch interval of the chrominance signal. For PAL and NTSC chrominance signals this is the colour burst at the colour carrier reference frequency but for SECAM chrominance signals these are the no-colour frequencies (4.250 and 4.40625 MHz).

NTSC-M and NTSC-4.4 modes compare the phase of the colour burst signal with the (B–Y) reference signal generated by dividing the 7.2 or 8.8 MHz crystal oscillator frequency by two (NTSC-M and NTSC-4.4 respectively). In each case, the phase discriminator output pulses are unipolar. The pulses are integrated by an external capacitor connected to pin 22 to provide a DC level.

For PAL identification, the phase of the colour burst signal is compared with that of the (R–Y) reference signal, generated by dividing the 8.8 MHz crystal oscillator frequency by two. The output pulses from the phase discriminator alternate in polarity but, after being fed through an H/2 demodulator, have the same polarity as the NTSC pulses. These pulses are integrated by an external capacitor connected to pin 23 to provide a DC level.

In contrast to the QAM standards, SECAM uses frequency modulation of the colour carriers. For SECAM identification, the alternating no-colour carrier frequencies present on the back porches are demodulated. The two no-colour carrier frequencies generate

pulses of alternate polarity (as with PAL) which are therefore fed to the H/2 demodulator. The unipolar output pulses are integrated by the external capacitor connected to pin 23, again to provide a DC level.

The voltages present on pin 23 (PAL and SECAM discriminator outputs) and pin 22 (NTSC discriminator output) are used to identify the chrominance signal. These voltages are fed to comparators and logic circuits to derive a correct identification of the colour transmission standard. The capacitor voltage consists of a fixed component derived from internal biassing at half the supply voltage (6 V), plus an extra component δV22 or δV23 provided by the input chrominance signal.

Table 1 summarizes the resultant voltage levels on the capacitors connected to pins 22 and 23 generated by input chrominance signals conforming to each of the colour transmission standards. When a colour transmission standard is identified, the appropriate capacitor voltage increases (+) above the internal biassing value (0). In the PAL and SECAM modes, the voltage on the capacitor connected to pin 23 increases when the colour transmission standard is identified. In the NTSC-M and NTSC-4.4 modes, the voltage on the capacitor connected to pin 22 always increases when an NTSC transmission is identified. As shown in Table 1, for black and white signal transmissions no input chrominance signal can be identified, the average capacitor currents are zero, and δV22 and δV23 = 0.

When the TDA4650 is in the NTSC-4.4 mode, both PAL and NTSC phase discriminators are activated. The NTSC phase discriminator uses the (B–Y) colour-difference reference signal at 4.43 MHz which, in comparison with the colour burst signal of the PAL or NTSC-4.4 signal, generates pulses of the same polarity. These pulses charge the capacitor on pin 22 to V_c + δV_c. If the input chrominance signal conforms to the PAL colour transmission standard, the NTSC phase discriminator also outputs pulses with constant polarity since the PAL colour burst includes a component which is constant in the negative (B–Y) axis on each line. These pulses also charge the capacitor on pin 22 to V_c + δV_c so that, even though the TDA4650 mode is set to NTSC-4.4, the voltage on pin 22 is V_c + δV_c. Furthermore, since the PAL phase discriminator and H/2 demodulator are activated, the capacitor on pin 23 is also charged to V_c + δVc. Finally, if the input chrominance signal conforms to the NTSC-M or SECAM standard, the frequency difference between the colour burst and the 4.43 MHz reference frequency is so large that the output from the NTSC phase discriminator is zero (δV22 = 0).

PAL/NTSC Reference Frequency Generation

To identify and demodulate PAL and NTSC quadrature amplitude-modulated chrominance signals, the reference signals (R–Y) and (B–Y) are required. These reference signals are generated by a PLL consisting of a Voltage-Controlled Crystal Oscillator (VCXO), crystals X1 and X2, a 2:1 frequency divider and a phase detector. The phase detector compares the phase of the colour burst signal with the (R–Y) reference signal. The VCXO frequency is double the colour burst frequency for both X1 (PAL, NTSC-4.4) and X2 (NTSC-M) inputs at pins 21 and 19 respectively. This circuit has the advantage that both the quadrature colour-difference reference signals (R–Y) and (B–Y) are generated at the output of the frequency divider.

The colour burst output from the Automatic Colour Control (ACC) circuits is fed directly to the phase detector for PAL but via the hue control for NTSC. The phase of the colour burst signal is shifted by at least ±30° by 3 ±1 V applied to pin 17 from the resistive

TABLE 1

δV22, δV23 for the input chrominance signal and TDA4650 decoding mode

TDA4650 mode	PAL		NTSC-4.4		NTSC-M		SECAM		b/w	
	δV22	δV23	δV22	δV23	δV22	δV23	δV22	δV23	δV22	δV23
PAL	0*	+	0*	0	0*	0	0*	0	0	0
NTSC-4.4	+	+	+	0	0	0	0	0	0	0
NTSC-M	0	0	0	0	+	0	0	0	0	0
SECAM	0*	0	0*	0	0*	0	0*	+**	0	0

0 average capacitor charge current is zero, $\delta V_c = 0$, $V_c =$ supply voltage.
\+ average capacitor charge current >0, $\delta V_c > 0$ (reference oscillator locked and correct H/2 demodulator switching).
* NTSC phase discriminator switched off.
** 50 Hz SECAM transmission only.

potential divider. The phase detector is enabled by the burst key pulses from the pulse processing circuits. The PLL time-constant is determined by the second-order filter between pins 18 and 20.

Pin 17 is also connected to the SERVICE switch which is used to set up the crystal oscillator frequencies for PAL, NTSC-4.4 and NTSC-M. If the voltage on pin 17 is less than 0.5 V (e.g. connected to ground), the colour burst signal and the colour-killer switch are inhibited but colour decoding remains operational. The PLL is switched off and the VCXO free-runs. This enables the trimmer capacitors in series with crystal oscillators X1 (PAL and NTSC-4.4) and X2 (NTSC-M) to be adjusted for minimum colour rolling. If the voltage on pin 17 is greater than 5.5 V (e.g. connected to the supply voltage), hue control and the colour-killer switch are inhibited but otherwise the PLL and colour decoding operate normally.

The crystal oscillator is selected by internal switching under control of the colour transmission standard selection and switching circuits in accordance with the mode demanded by the automatic control and scanning sequence. VCXO lock-on frequency ranges are determined by the characteristics of the external second-order filter. To prevent interference, the VCXO is switched off when SECAM is selected.

CHROMINANCE SIGNAL CONTROL

The TDA4650 (and the TDA4660) must provide colour-difference signals of constant amplitude so that they are independent of variations in the amplitude of the CVBS or S-VHS chrominance signal. This maintains a fixed relationship between the amplitudes of the luminance signal (Y) and the −(R−Y) and −(B−Y) colour-difference signals independent of the IF filter characteristics and receiver de-tuning. For PAL and NTSC, the reference signal used for Automatic Colour Control (ACC) is the amplitude of the colour burst signal. For SECAM, the reference signals are the amplitudes of the no-colour frequency signals on the back porch.

The chrominance signal input is AC-coupled via pin 15 to a gain-controlled chrominance amplifier for which the chrominance signal gain is set by in-phase synchronous demodulation. This technique has the advantage that it has a single time-constant, determined by the capacitor connected to pin 16, for all colour transmission standards. It further uses the noise content of the chrominance signal to prevent the colour saturation increasing with high noise levels (colour bright-up effect). In-phase synchronous demodulation is also independent of the mode of the TDA4650 so that the chrominance signal stabilizes quickly. This is also important during the automatic control and scanning sequence to guarantee quick identification of the colour transmission standard. The chrominance amplifier uses low-distortion symmetrical circuits to avoid generation of even harmonics of SECAM chrominance signals. Biassing for the chrominance amplifier is stabilized by an independent DC feedback loop, decoupled by the external capacitor at pin 14.

The nominal peak-to-peak amplitude of the chrominance signal input at pin 15 is 200 mV with a 75% colour-bar signal. The ACC range is 20 mV to 400 mV which is adapted to a 1 V peak-to-peak CVBS signal input to the PAL SECAM PAL/NTSC filters.

The gain-controlled chrominance signal, including the colour burst signal, is fed to the colour transmission standard identification circuits and to the PLL for reference signal generation (via the hue control for NTSC chrominance signals). In addition, for PAL and NTSC, the chrominance signal is fed to the line/field blanking circuit prior to demodulation. In the case of SECAM, the chrominance signal is fed to a limiter-amplifier prior to demodulation.

CHROMINANCE SIGNAL DEMODULATION

The PAL/NTSC or SECAM chrominance signal demodulators are selected according to the automatic control and scanning sequence. The VH (vertical and horizontal pulses) from the pulse processing circuits blank the colour-difference signals. The H/2 signal inverts the phase of the PAL (R−Y) chrominance component and blanks the SECAM colour-difference signals line sequentially for compatibility with the TDA4660.

PAL/NTSC Chrominance Signal Demodulation

The (R−Y) and (B−Y) components of PAL/NTSC chrominance signals are demodulated by two conventional, balanced, synchronous cross-coupled differential amplifiers. The chrominance signal from the colour burst blanking circuits is fed to the emitters of the differential amplifiers while the (R−Y) and (B−Y) reference signals from the PLL are fed to the bases of the demodulator transistors. The VH pulses inhibit PAL/NTSC chrominance signal demodulation during the vertical and horizontal components of the sandcastle pulse.

The phase of the chrominance signal to the emitter of the (R–Y) demodulator is inverted line-sequentially by a PAL switching circuit, switched by the H/2 signal. This circuit is disabled in the NTSC mode. The PAL switching circuit provides the necessary phase reversal to demodulate the PAL (R–Y) colour-difference signal on successive horizontal scan lines with consistent polarity.

The gains of the PAL and NTSC demodulators are set so that the colour-difference signals at the outputs of the TDA4660 have nominal peak-to-peak values of –(R–Y) = 1.05 V and –(B–Y) = 1.33 V. Therefore, the outputs of the TDA4650 are approximately half these values in the PAL and NTSC modes.

SECAM Chrominance Signal Demodulation

The SECAM frequency-modulated (R–Y) and (B–Y) colour-difference signals are transmitted on alternate scan lines. Therefore, to decode these signals using baseband delay lines, only a single FM demodulator is required.

The SECAM chrominance signal is demodulated by a quadrature demodulator which follows a limiter-amplifier; this removes residual amplitude variations after automatic colour control. The quadrature demodulator is, as for PAL and NTSC, a four-quadrant linear multiplier with two pairs of inputs. One pair is directly connected to the SECAM chrominance signal from the limiter-amplifier and the other pair is connected to the external SECAM reference tuned circuit. This tuned circuit shifts the phase of the chrominance signal depending on its frequency. An additional high-pass filter consisting of 150 pF capacitors and a 4.7 kΩ resistor compensates for phase shifts after the SECAM reference tuned circuit.

During the H and V blanking intervals, SECAM chrominance signal demodulation is inhibited and artificial black levels are superimposed on the SECAM colour-difference signals. These SECAM artificial black levels are adjusted to the different black levels of the demodulated two colour-difference signals. The offsets of the two SECAM artificial black levels are determined by the black level frequency offsets of the SECAM chrominance signal and the FM-demodulator efficiency ($\delta V/\delta f$). The SECAM artificial black level offsets are internally set to a fixed value, therefore the FM-demodulator efficiency (mainly determined by the resonant frequency and the Q-factor of the SECAM reference tuned circuit) has to be adjusted to the internal value.

The line-sequential –(R–Y) and –(B–Y) SECAM colour-difference signals are de-multiplexed on to the parallel colour-difference signal paths. During the line-sequential, inactive colour-difference signal time the appropriate (clean) black levels are superimposed on the SECAM colour-difference signals.

In the TDA4660, the line-delayed colour-difference signal is added to the undelayed colour-difference signal. Therefore, for SECAM colour-difference signals, the active signal from the previous line which has been stored in the delay line is repeated during the black level line interval. To obtain the same colour-difference signal voltages at the outputs of the TDA4660 for all colour transmission standards, the amplitudes of the colour-difference signal outputs from the TDA4650 in the SECAM mode are twice those for PAL and NTSC. Thus the colour-difference signal outputs of the TDA4650 in the SECAM mode are –(R–Y) = 1.05 V and –(B–Y) = 1.33 V peak-to-peak (values for 75% colour-bar signal).

Demodulator Output Stages

The outputs of the PAL/NTSC and SECAM chrominance signal demodulators are connected in parallel. The colour-difference signals are filtered by low-pass filters with –3 dB frequencies at 1.0 MHz to suppress high-frequency interference signals and mixing products.

To establish a reference black level for all three colour transmission standards, the colour-difference signals are fed to the black level clamp circuit. The black level is set by comparing the colour-difference signal with a DC reference voltage during the burst key component of the sandcastle pulse. For PAL and NTSC modes, both colour-difference signals are clamped on each line. For the SECAM mode, alternate colour-difference signals are clamped on successive lines using the H/2 signal. The black level clamp circuits use the capacitors on pin 6 (R–Y) and pin 5 (B–Y) for storage.

In the SECAM mode only, the colour-difference signals are switched to a SECAM de-emphasis circuit. The de-emphasis time-constants are determined by the capacitors on pin 2 (R–Y) and pin 4 (B–Y). 220 pF capacitors and internal resistors set the SECAM de-emphasis time-constants to 1.85 µs.

The colour-difference signals are finally fed to the colour-killer switch. When the colour-killer is operational (no colour transmission standard detected) the colour-difference signal outputs are switched to the reference black level. The –(R–Y) and –(B–Y) colour-

difference signals are fed through buffer amplifiers (NPN emitter followers) to pins 1 and 3.

The TDA4650 is in a 28-pin DIL (SOT-117) package and operates over an ambient temperature range of 0 to +70°C.

BASEBAND SWITCHED-CAPACITOR DELAY LINES

The TDA4660, Switched-Capacitor Delay Line, consists of two colour-difference comb filters. Each comb filter consists of an undelayed signal path and a 64 μs-delayed signal path, see Fig.3. All the necessary switching signals are generated from a master clock with a nominal frequency of 3 MHz. The master clock is derived from a 6 MHz Current-Controlled Oscillator (CCO) which is line-locked by a PLL to the burst key component of the sandcastle pulse (SSC). Since the delay lines are locked to the line frequency via the burst key pulses, the TDA4660 functions correctly at the different PAL and NTSC line frequencies and at the variable line frequencies from a VCR.

The switched capacitor delay line operates according to the mode demanded by the colour transmission standard. In the PAL mode it operates as a geometric adder to satisfy the requirements of PAL demodulation. In the NTSC mode it reduces cross-colour interference. In the SECAM mode the delay line repeats the colour-difference signal on consecutive horizontal scan lines. The adder doubles the output signal amplitude in the PAL and NTSC modes.

The colour-difference signals are capacitively coupled to the TDA4660 at pins 16 and 14. The colour-difference signals are clamped at 1.5 V DC (V_{REF}) before being fed to the buffer amplifiers of the parallel, delayed and undelayed signal paths. The output of the undelayed colour-difference signal buffer amplifiers are fed directly to one input of the adders. These buffer amplifiers are loaded by dummy loads to ensure that the undelayed colour-difference signal paths have the same frequency and phase response as the buffer amplifiers of the delayed colour-difference signal paths with their capacitive loads. The delayed colour-difference signal is fed to the write rail from where it is switched by the parallel switches to the line store capacitors.

The line store consists of 190 parallel capacitors, each with a write switch and a read switch, see Fig.4. In contrast to most sample-and-delay circuits the line stores have a parallel structure. This eliminates the well-known cumulative error of series structures (e.g. CCD devices), since the pixel information is stored and delayed using only one write and one read charge transfer. Sampling and storage of the colour-difference signal for a complete horizontal line is performed by connecting each capacitor to the write rail in sequence, controlled by the shift register output logic signal. Simultaneous with writing the n^{th} sample on to capacitor C_n, the $(n + 1)^{th}$ sample from the previous line is being read, i.e. at the same instant that C_2 is connected to the write rail to write the present colour-difference signal voltage, the charge of C_3 is being transferred via the read rail to the sense/reset capacitor C_S.

The sense/reset circuit converts the charge read from the storage capacitor into a voltage. This is fed to the sample-and-hold circuit and then to a passive third-order Butterworth low-pass filter. The −3 dB cut-off frequency is 1 MHz which removes the 3 MHz master clock component present in the delayed signal read from the line store.

For a line frequency of 15.625 kHz and a master clock frequency of 3 MHz, there are 192 master clock cycles per horizontal line. There are 190 line store capacitors since due to the clock timing, the delay between the input buffer amplifier and the output from the sense/reset circuit is exactly one horizontal line period minus $3\tau/2$, where τ = 333 ns. The sample-and-hold circuit introduces a delay of $\tau/2$ and the low-pass filter a delay of exactly τ. As a result, the delayed colour-difference signal is delayed by exactly one line period at the input to the adder.

The delayed and undelayed colour-difference signals are added in the adder circuits. To correctly match the delayed and undelayed colour-difference signals, the timing error between them at the input to the adder must be less than 90 ns and the gain error between them less than ±0.2 dB. The outputs of the adder circuits are buffered and fed to pins 11 and 12. The output colour-difference signals from the TDA4660 have peak-to-peak levels of −(R−Y) = 1.05 V and −(B−Y) = 1.33 V with output impedances of nominally 300 Ω.

The pulse processing circuits are locked to the line frequency using the burst key component of the sandcastle pulse on TDA4660, pin 5. The timing reference is the leading edge of the burst key pulse. The burst key component is extracted from the sandcastle pulse in the sandcastle pulse detector. The comparator switching threshold voltage is 1.5 V less than the maximum value of the burst key component. This extracted burst key component is the Digital Burst Key (DBK) pulse and is the reference for the line-locked PLL.

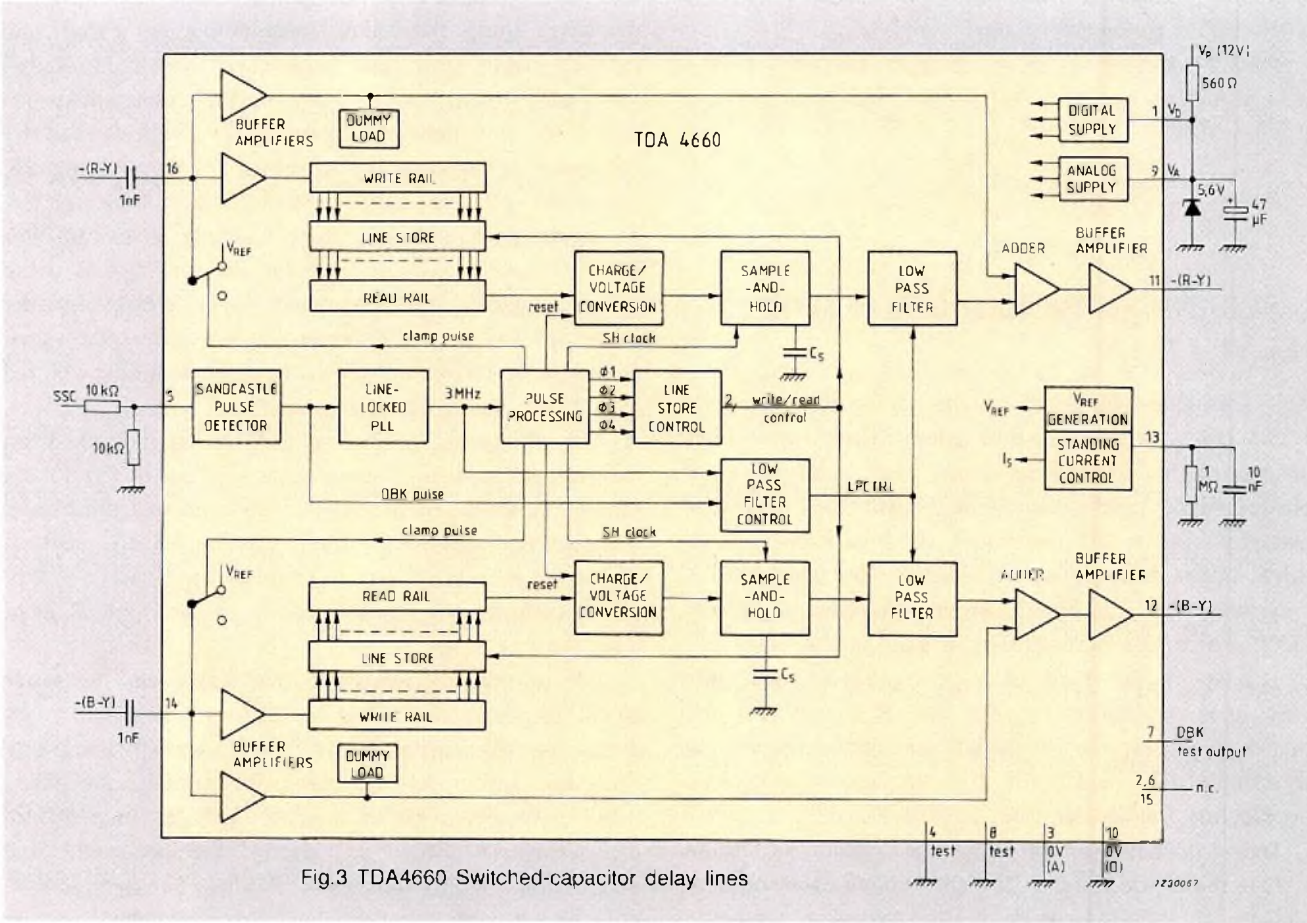


Fig.3 TDA4660 Switched-capacitor delay lines

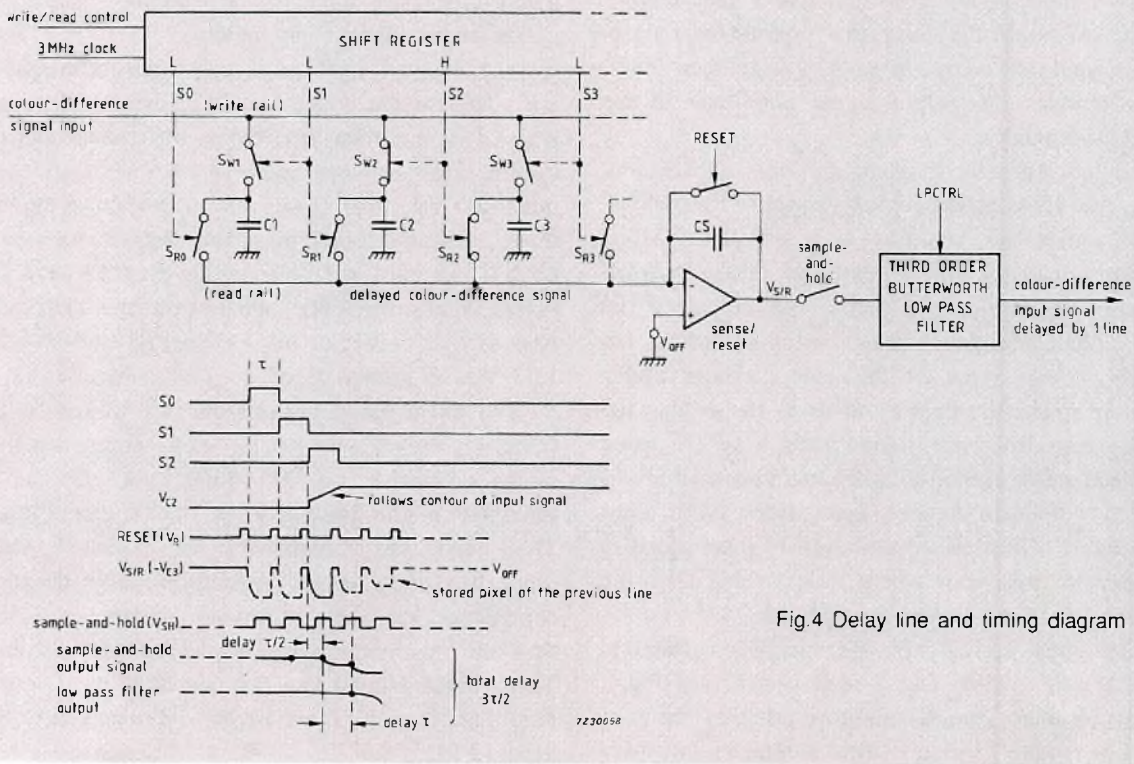


Fig.4 Delay line and timing diagram

The line-locked PLL contains a 6 MHz CCO, the frequency of which is divided by two to generate the 3 MHz master clock with a duty factor of 50%. In the PLL, the master clock frequency is divided by 192 to generate the line frequency pulses (FH2). The FH2 and DBK pulses are compared in the phase detector of the PLL and the resultant error signal is filtered and used to correct the frequency of the CCO. The 3 MHz master clock is buffered and fed to the pulse processing circuits.

The pulse processing circuits generate four clock signals (ϕ1-ϕ4) for line store control, the reset pulse train for the sense/reset circuits, the sample-and-hold clock signals and the clamp pulses for the input buffer amplifiers. The line store clocks are fed to the shift register to clock the switches of the 190 capacitors. The clocked write control pulse controls the duration of the horizontal scan line. The clamp pulses have a duration of 2 μs and occur 1 μs after the leading edge of the burst key component of the sandcastle pulse.

The delay in the third-order Butterworth low-pass filters has to be exactly τ to correctly match the delayed and undelayed colour-difference signals at the input to the adder. This delay has to be exact not only for both PAL and NTSC colour transmission standards but also for the variable line frequencies from VCRs. Since all the clocks and pulse trains in the TDA4660 are locked to the line frequency, the shift register logic outputs (S0- S189), sense/reset timing, the sample-and-hold clock and the clamp pulses all automatically track the input line frequency. To achieve an exact delay of τ in the low-pass filter, it also has to be locked to the existing line frequency. This is achieved by varying the -3 dB cut-off frequency of the Butterworth low-pass filters.

The Butterworth low-pass filters are multiple R/C structures in which the resistor values are controlled by the LPCTRL signal output from the low-pass filter control circuit. This contains a Butterworth low-pass filter, similar to those in the delayed colour-difference signal paths to monitor the delay, a pulse former, a phase detector and all the components necessary for a control loop. The pulse former generates a digital pulse with a duration of 5 clock cycles for every line which is fed to the low-pass filter input. The rise and fall times of the output pulses from this low-pass filter are considerably longer than those of the input pulses due to the filter bandwidth. The delay circuit measures the low-pass filter output voltage at the mid-point of the leading edge and exactly 5 clock cycles after it. When the low-pass filter has the correct bandwidth/delay, the difference between these two voltage measurements is zero. Otherwise, the voltage difference provides the control voltage to correct the bandwidth/delay of the Butterworth low-pass filter in the control loop. This control voltage (LPCTRL) is simultaneously fed to the Butterworth low-pass filters in the delayed colour-difference signal paths so that delay τ automatically tracks the line frequency.

The TDA4660 is alignment-free and consumes only 35 mW from a single supply (+5.6 V). The TDA4660 is in a 16-pin DIL (SOT-38) package and operates over an ambient temperature range of 0 to +70°C.

PAL/NTSC, SECAM, NTSC FILTERS

The logic levels of the colour transmission standard switching signals (TDA4650, pins 25, 26, 27 and 28) select the appropriate external chrominance filter. The filter circuits shown in Fig.5 also extract the luminance/sync component from the CVBS signal using a chrominance trap, and provide S-VHS/CVBS chrominance signal selection. The luminance channel is considerably simplified since aperture correction is not included to improve the luminance transient response. This is provided by the TDA4670, Picture Signal Improvement (PSI) Circuit, under control of the I^2C-bus.

When the CVBSN logic input is open-circuit the S-VHS chrominance signal is selected, when it is LOW, the CVBS signal is selected. The chrominance filter is a bandpass RLC tuned filter with a Q-factor of exactly 16, trimmed to 4.286 MHz in the SECAM mode for HF de-emphasis. For PAL and NTSC-4.4 modes this bandpass filter is substantially damped by a switched parallel 330 Ω resistor to establish a bandwidth of approximately 1.4 MHz (Q-factor approximately 3.2). In the NTSC-M mode, the resonant frequency of the bandpass filter is set to approximately 3.58 MHz by a switched parallel 270 pF capacitor, again damped by a 330 Ω parallel resistor. The logic signals from the TDA4650 pins 25, 26 and 28 switch transistors (Q3 and Q4) to select the PAL/NTSC-4.4, SECAM or NTSC-M chrominance filter as required.

The luminance/sync component is selected by one of three parallel emitter followers (Q5 to Q7). The emitter follower in operation is the one with the highest positive potential on its base which consequently switches off the other two. The S-VHS emitter follower (Q5) is switched on when the CVBSN logic input is

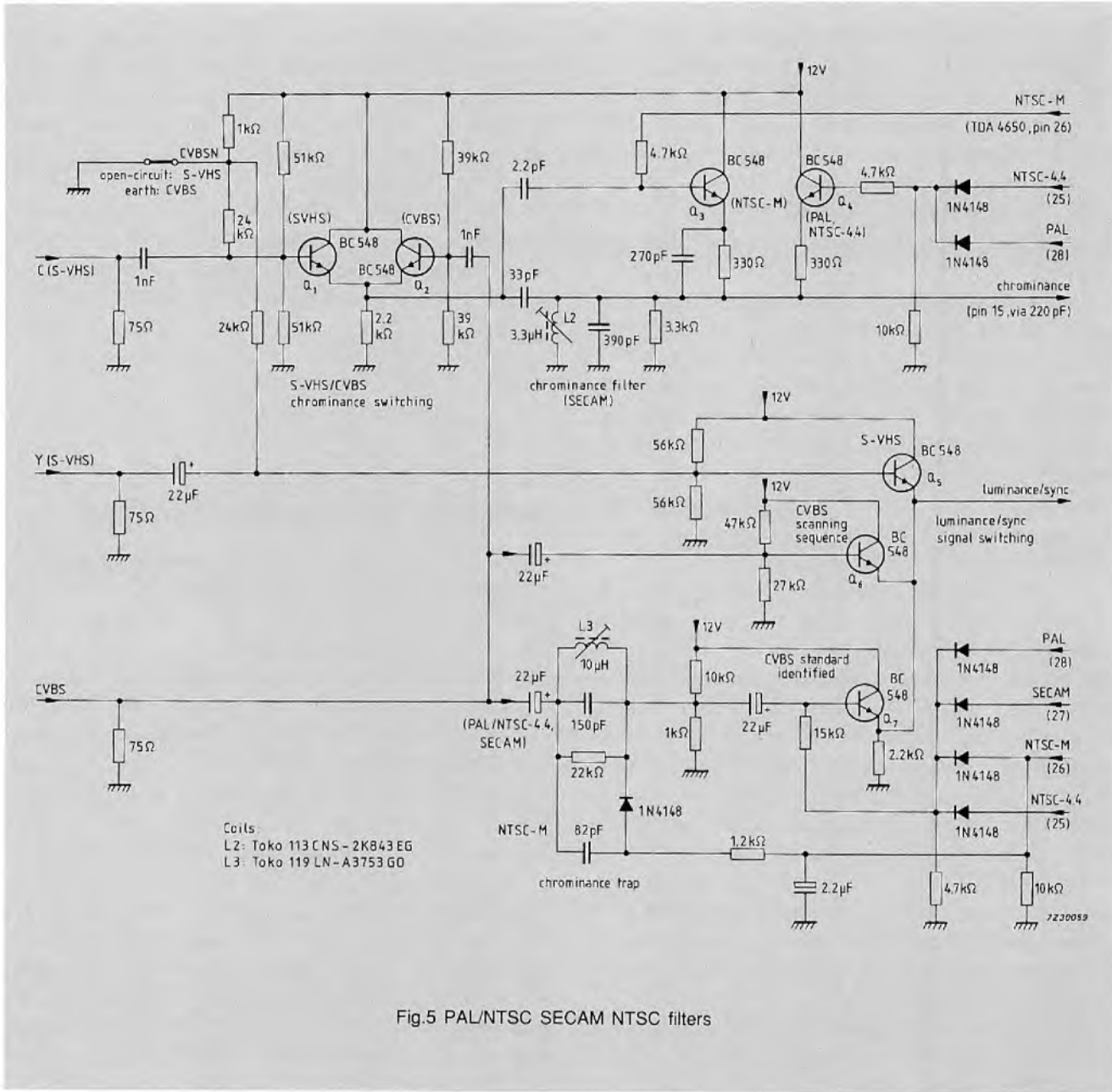
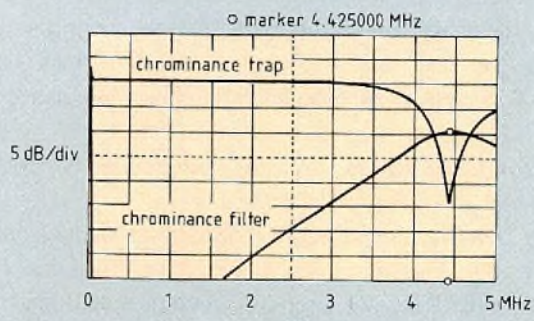


Fig.5 PAL/NTSC SECAM NTSC filters

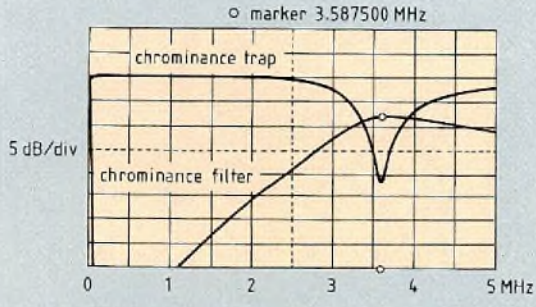
open-circuit, while the status of the two CVBS emitter followers is determined by the voltage levels on the TDA4650, pins 25, 26, 27 and 28. To avoid bandwidth limitation resulting from filtering during the automatic control and scanning sequence, the CVBS standard identified transistor (Q7) is inhibited by the reduced levels of the colour transmission standard switching signals (approximately +2.5 V). When a colour transmission standard is identified one of the colour transmission standard switching signals rises to typically +5.8 V. This switches on the CVBS standard identified transistor (Q7) and switches off the CVBS scanning sequence transistor (Q6).

For the PAL-B, G, H, I, SECAM and NTSC-4.4 modes the chrominance trap center frequency is 4.4 MHz. For the NTSC-M mode, the center frequency of the chrominance trap tuned circuit is set to approximately 3.6 MHz by switching an additional 82 pF parallel capacitor. The frequency response characteristics of the chrominance filters and the chrominance traps are shown in Fig.6.

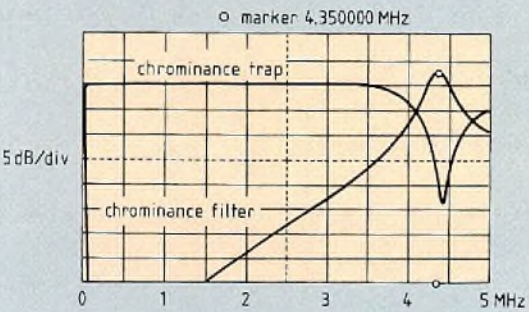
The PAL/NTSC SECAM NTSC filters of Fig.5 ensure that the bandwidth of the luminance signal is not restricted for S-VHS VCR inputs. Completely separate luminance and chrominance signal channels eliminates cross colour and cross luminance interference.



PAL/NTSC-4.4, f_{sc} = 4.433 MHz



NTSC-M, f_{sc} = 3.579 MHz



SECAM, $f_{o(B-Y)}$ = 4.250 MHz
$f_{o(R-Y)}$ = 4.406 MHz
f_{res} = 4.286 MHz

7Z30060

Fig.6 Chrominance filter and chrominance trap characteristics

Alignment Of PAL/NTSC SECAM NTSC Filters and the TDA4650

The PAL/NTSC SECAM NTSC filters require few components and are trimmed, together with the TDA4650, by the following procedure:

- Set CVBSN to LOW.
- Select the SECAM mode by connecting the +12 V supply to TDA4650, pin 27. Connect a SECAM colour-bar signal to the CVBS filter input and trim the 3.3 µH inductor of the SECAM Bell filter (L2) for minimum chrominance amplitude-modulation at pin 15 using an oscilloscope.
- Trim the SECAM reference tuned circuit, TDA4650, pins 8 and 9, with the oscilloscope connected to pins 1 and 3 (refer to Fig.2). Adjust the 10 µH inductor to set the no-colour level of the -(B−Y) colour-difference signal to the blanking voltage level. Then trim the parallel damping resistor to set the no-colour level of the -(R−Y) colour-difference signal to the blanking voltage level.
- Trim the PAL/NTSC-4.4 crystal oscillator frequency (X1, pin 21) with the PAL mode selected, i.e. TDA4650, pin 28 at +12 V. Set the SERVICE switch to PLL OFF (TDA4650, pin 17 less than 0.5 V) so that the crystal oscillator free-runs and is unaffected by the colour burst signal. Apply the PAL colour-bar signal to the CVBS filter input and trim the 30 pF capacitor in series with X1 for minimum beat frequency (colour rolling on the picture) of the −(R−Y) and −(B−Y) colour-difference output signals.
- Trim the chrominance trap inductor L3 in the PAL mode to obtain the minimum chrominance signal level at the luminance/sync (Y) output.
- Finally, select the NTSC-M mode by setting TDA4650, pin 26, to +12 V. Switch the SERVICE switch to PLL OFF (TDA4650, pin 17 less than 0.5 V) and apply the NTSC-M colour-bar signal to the CVBS filter input. Trim the 30 pF capacitor in series with crystal oscillator X2 for minimum beat frequency (colour rolling) of the −(R−Y) and −(B−Y) colour-difference output signals.

APPLICATIONS

The PCB shown in Fig.7 has been designed to include the TDA4650, TDA4660 and the PAL/NTSC, SECAM, NTSC filters. The complete printed-circuit board also includes the TDA4670, Picture Signal Improvement Circuit, the TDA2579A Horizontal/Vertical Synchronization Circuit and a HEF4011B, Quadruple 2-Input NAND Gate (for sandcastle pulse generation). I^2C-bus control is necessary for the TDA4670 whereas both

multi-standard colour decoding and sync processing are independent of I²C-bus control. If picture signal improvement is not required, the luminance and colour-difference inputs and outputs of the TDA4670 are bridged by jumpers. The SERVICE switch and the hue control resistors (TDA4650, pin 17) are the only components shown in Figs 2 and 5 which have to be connected externally to the printed-circuit board.

The PCB has a 96-pin connector interface. The inputs are the +12V supply (pin A5), the +8V supply (pin A4), the S-VHSN TTL logic signal (pin A28), the S-VHS chrominance and luminance signal components (pins A29 and A30), the CVBS signal (pin A32), the hue control input (pin A11), the four colour transmission standard switching signals (pins A13 to A16) and the I²C-bus inputs SDA and SCL (pins A23 and A24). The outputs are the colour-difference signals (pins C15 and C17), the luminance signal (pin C19), the super sandcastle pulse (pin C27), the monitor sync signal (pin C32) and the vertical and horizontal pulses (pins C25 and C26). The PCB supplies luminance and colour-difference signals to the TDA4680, Video Control Combination Circuit, or indirectly to the TDA4680 via a feature module.

To achieve the versatility needed to manufacture a family of colour decoders all based on the same PCB, the TDA4650 can be used for multi-standard decoding or it can be replaced by either of the single-standard decoders, TDA4510 (PAL) or TDA4570 (NTSC). These are low-cost alternatives and can be used instead of the TDA4650 with the appropriate changes in the colour decoder's peripheral components.

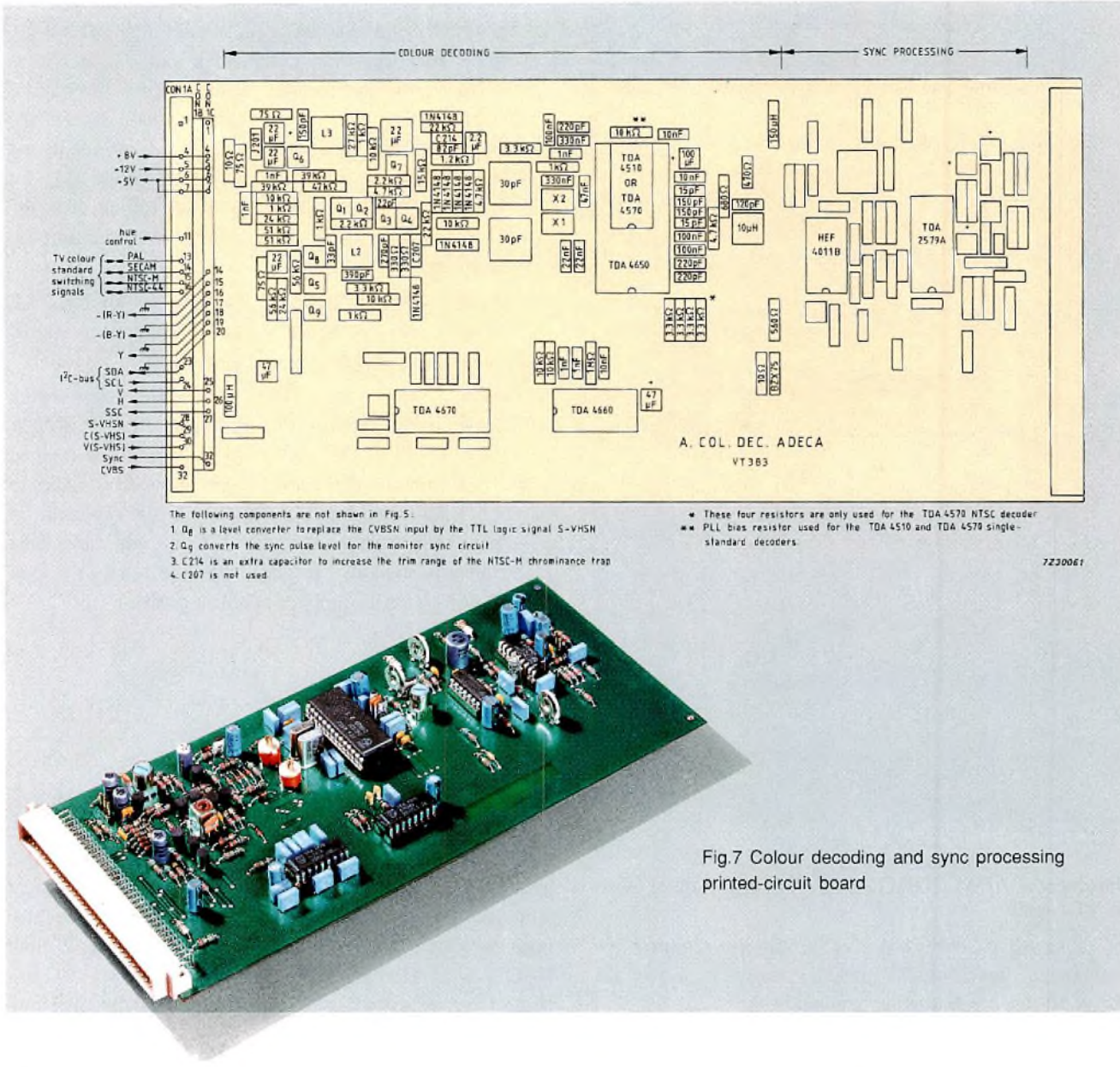


Fig.7 Colour decoding and sync processing printed-circuit board

PERFORMANCE DATA

Typical performance data for the TDA4650 and TDA4660 are as follows:

TDA4650	
supply voltage:	12 V
supply current:	65 mA
chrominance signal input (75% colour-bar):	200 mVpp
-(R-Y) colour-difference output in PAL/NTSC modes:	0.535 Vpp
-(B-Y) colour-difference output in PAL/NTSC modes:	0.675 Vpp
-(R-Y) colour-difference output in SECAM mode:	1.05 Vpp
-(B-Y) colour-difference output in SECAM mode:	1.33 Vpp
hue control range in NTSC mode, (pin 17, 3 ±1 V):	±30° min.
transmission standard switching signal, OFF-state:	0.5 V max.
transmission standard switching signal, scanning-state:	2.45 V
transmission standard switching signal, ON-state:	5.8 V
transmission standard switching signal, forced selection:	9.0 V min.
TDA4660	
supply voltage:	5.6 V
supply current:	5.5 mA
-(R-Y) colour-difference output, PAL, NTSC, SECAM:	1.05 Vpp
-(B-Y) colour-difference output, PAL, NTSC, SECAM:	1.33 Vpp
-(R-Y) to -(B-Y) channel gain tolerance:	±0.5 dB
delay line time:	64 ±0.06 µs
output impedance:	300 Ω
Super Sandcastle Pulse (SSC)	
burst key pulse:	>7.7 V
horizontal blanking pulse:	4.5 ±0.4 V
vertical blanking pulse:	2.5 ±0.5 V

REFERENCE

1. Van Gurp, Boudewijns, Van Keeken: 'Switched Capacitor Chrominance Baseband Delay Lines For Colour Decoders', IEEE Transactions on Consumer Electronics, Vol. CE-33, No.3, August 1987.

Logic level FETs

ARTHUR WOODWORTH

Standard power MOSFETs require a gate-source voltage of 10 V to achieve a 'saturated' on-state condition. With Logic Level FETs (L^2FETs) however, the same level of saturation is possible with a gate-source voltage of only 5 V. They can therefore be driven directly from 5 V TTL/CMOS ICs without the need for the level shifting stages required for standard MOSFETs, see Fig.1. This makes them ideal for today's sophisticated automotive electrical systems, where microprocessors are being used to drive switching circuits.

This characteristic of L^2FETs is achieved by reducing the gate-oxide thickness from about 800 nm to about 500 nm, which reduces the threshold voltage of the device from the standard 2.1 – 4.0 V to 1.0 – 2.0 V. However, the result is a reduction in gate-source voltage ratings, from ±30 V for a standard MOSFET to ±15 V for the L^2FET. Nevertheless this is still an improvement over the industry standard voltage rating of ±10 V for L^2FETs.

Although a 5 V gate-drive is ideal for L^2FETs, they can be used in circuits with gate-drive voltages of up to 10 V. Using a 10 V gate-drive results in a reduced $R_{DS(ON)}$ (see Fig.2), but the turn-off delay time is increased. This is due to excessive charging of the L^2FET's input capacitance.

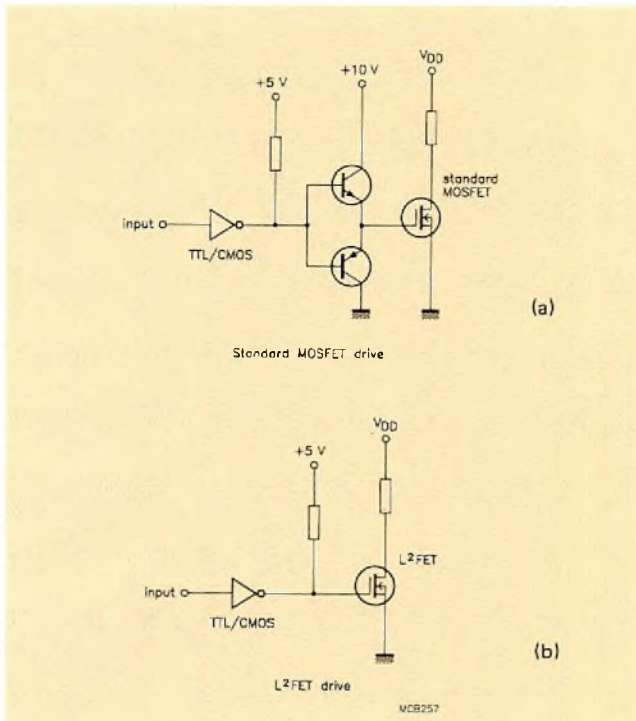


Fig.1 Drive circuit for (a) a standard MOSFET and (b) an L^2FET

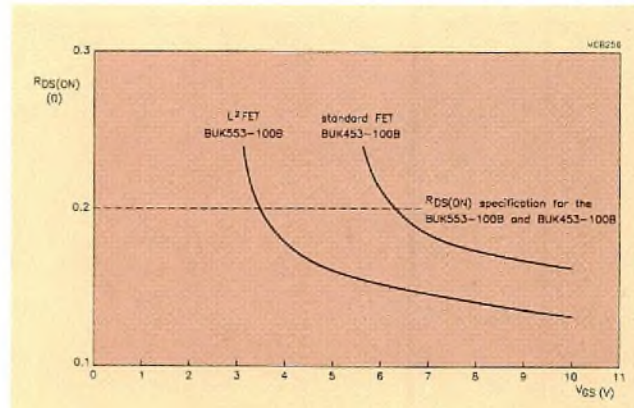


Fig.2 $R_{DS(ON)}$ as a function of V_{GS} for a standard BUK453-100B MOSFET and a BUK553-100B L^2FET. T_j = 25 °C; I_D = 5 A; V_{GS} = 10 V

L^2FET CAPACITANCES

Figure 3 shows the parasitic capacitance areas of a typical Power MOSFET cell. Both the gate-source capacitance C_{gs} and the gate-drain capacitance C_{gd} increase due to the reduction in gate-oxide thickness, although the increase in C_{gd} is only significant at low levels of V_{DS}, when the depletion layer is thin. Increases in input capacitance C_{is}, output capacitance C_{os} and reverse transfer capacitance C_{rs} result in an overall capacitance increase of 25% for the L^2FET, compared with a similar standard type, at V_{DS} = 0 V. This is not a problem however, as these parasitic capacitances are virtually negligible at the standard measurement condition of V_{DS} = 25 V.

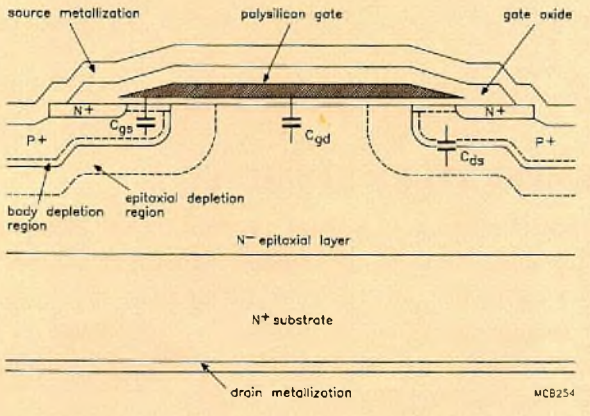


Fig.3 Parasitic capacitances of a typical Power MOSFET cell

TRANSCONDUCTANCE AND GATE CHARGE

Forward transconductance g_{fs} is a function of the oxide thickness, so the g_{fs} of an L^2FET is typically 40% – 50% higher than a standard MOSFET. This increase in g_{fs} more than offsets the increase in the overall capacitance of an L^2FET, so the turn-on charge requirement of the L^2FET is lower than that of the standard type, see Fig.4. For example, the standard BUK453-100B MOSFET requires about 17 nC to be fully switched on (at a gate-source voltage of 10 V), while the BUK553-100B L^2FET only needs about 12 nC (at a gate-source voltage of 5 V).

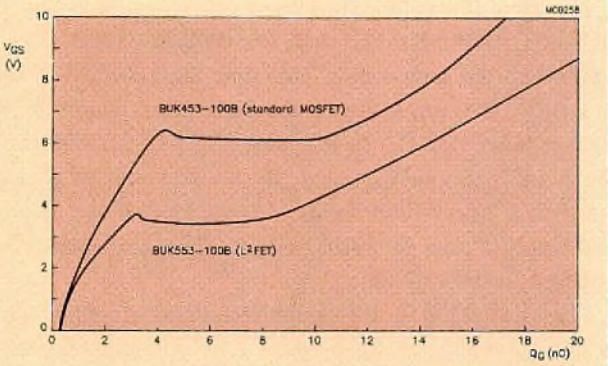


Fig.4 Turn-on gate charge curves of a standard BUK453-100B MOSFET and a BUK553-100B L^2FET. V_{DD} = 20 V; I_D = 12 A

SWITCHING SPEED

Figure 5 compares the turn-on performance of the standard BUK453-100B MOSFET and the BUK553-100B L^2FET, under identical drive conditions of 5 V from a 50 Ω generator, using identical loads. Thanks to its lower gate threshold voltage $V_{GS(TO)}$, the L^2FET can be seen to turn on in a much shorter time from the low-level drive.

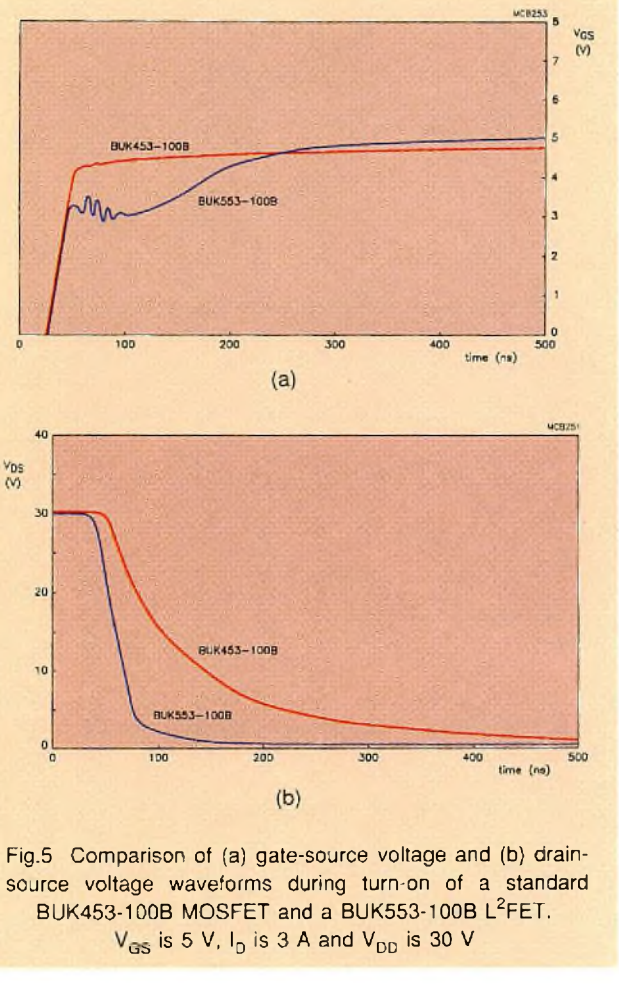


Fig.5 Comparison of (a) gate-source voltage and (b) drain-source voltage waveforms during turn-on of a standard BUK453-100B MOSFET and a BUK553-100B L^2FET. V_{GS} is 5 V, I_D is 3 A and V_{DD} is 30 V

Figure 6 shows the turn-off performance of the standard BUK453-100B MOSFET and the BUK553-100B L^2FET, again with the same drive. This time the L^2FET is slower to switch. The turn-off times are determined mainly by the time required for C_{gd} to discharge. The C_{gd} is higher for the L^2FET at low V_{DS}, and the lower value of $V_{GS(TO)}$ leads to a lower discharging current, due to the internal resistance of the gate-drive circuit. The net result is an increase in turn-off time.

Fast switching in, for example, automotive applications is not important. In areas where it is important however, the drive conditions should be examined. For example, for a given load power, a 10 V drive requires a 50 Ω source impedance, whereas a 5 V drive will require one of only 12 Ω. This results in faster switching for the L^2FET compared with standard MOSFETs.

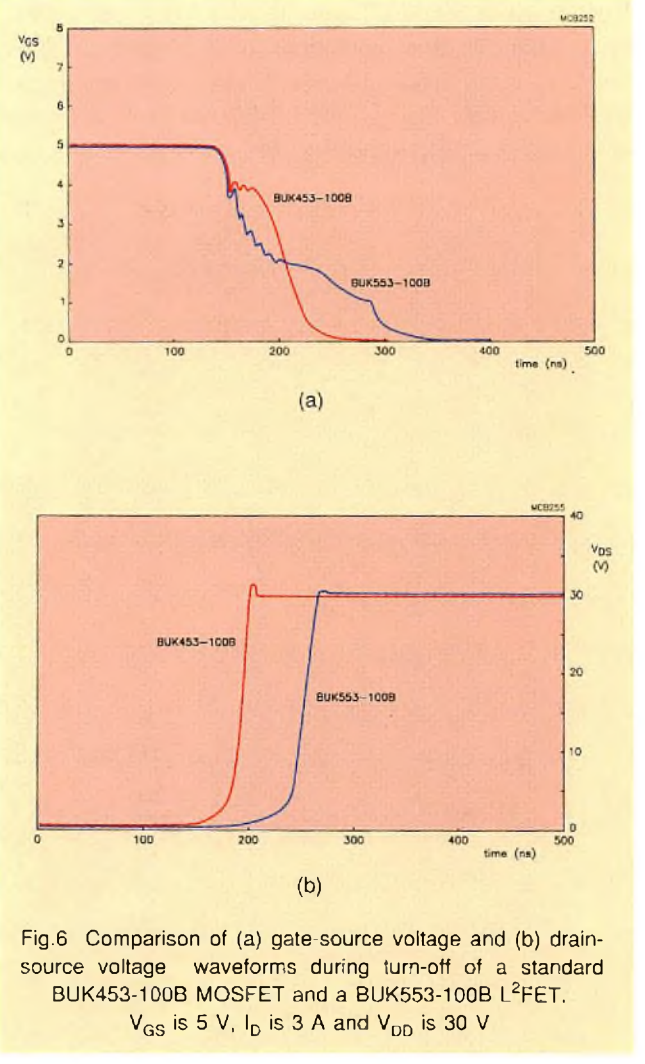


Fig.6 Comparison of (a) gate-source voltage and (b) drain-source voltage waveforms during turn-off of a standard BUK453-100B MOSFET and a BUK553-100B L^2FET. V_{GS} is 5 V, I_D is 3 A and V_{DD} is 30 V

RUGGEDNESS AND RELIABILITY

Automotive applications frequently require L^2FETs to withstand the energy of an unclamped inductive load turn-off. This energy is dissipated in the bulk of the silicon however, and stress is avoided in the gate oxide. A thinner gate oxide in L^2FETs does not affect their ruggedness or reliability. Good control of key process parameters such as pinhole density, mobile ion content and interface state density ensures good oxide quality. The present range of L^2FETs includes devices which can withstand drain-source voltages of up to 400 V.

The V_{GS} rating of an L^2FET is about half that of a standard MOSFET, but this does not affect the V_{DS} rating, which can be the same for both types of FET. In principle, an L^2FET version of any standard MOSFET is feasible.

TEMPERATURE STABILITY

In general, threshold voltage decreases with increasing temperature. Although the threshold voltage of L^2FETs is lower than that of standard MOSFETs, so is their temperature coefficient of threshold voltage (about ½ in fact), so their temperature stability compares favourably with standard MOSFETs.

APPLICATIONS

The automotive industry in particular will benefit from L^2FETs, which can switch regulators and converters, drive electromechanical parts like motors and solenoids, and are reliable enough to displace mechanical relays. Since they enable power loads to be driven directly from ICs, they may be considered to be the first step towards intelligent power switching. The low voltage (≤200 V) L^2FETs are available in SOT186 and TO220 outlines, and have a T_{jmax} rating of 175 °C, rather than the industry standard of 150 °C. The projected MTBF is 2070 years at 90 °C, at a 60% confidence level.

ICs for electronically-tuned car radios

ARNOLD GARSKAMP

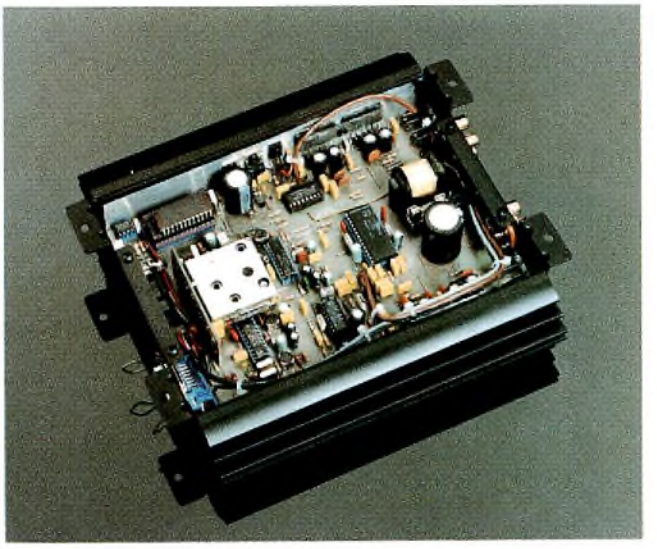
A moving car is probably the worst possible operating environment for a radio. There are wide variations of battery voltage and temperature, considerable vibration, a lot of interference generated by the engine and constantly changing reception conditions. Furthermore, demands for extra facilities such as cassette and CD players severely limit the amount of space available for radio circuitry. Further difficulties arise because the increasing number of transmissions on the air makes tuning more difficult for the listener who must concentrate on driving rather than operating the radio.

Much research has been devoted to developing radio circuitry to solve these problems; highly integrated circuitry for increased reliability, variable-capacitance diode tuning, interference limiting and DC controlled audio functions are now commonplace. More recent innovations include microcomputer control of tuning with search facilities, preset station selection and digital frequency indication.

By using our unrivalled experience of developing and fabricating ICs and using them in Philips equipment we have now extended the horizons of car radio design yet further with a set of state-of-the-art ICs for electronically-tuned car radios. To demonstrate the capabilities of this new chip-set, we have developed the circuitry and software for an AM/FM stereo electronic car radio application proposal in which the tuning system, frequency display, stored station memory and audio functions are microcomputer-controlled via the simple bidirectional two-wire Inter IC (I^2C) bus[1].

The partitioning of our car radio chip set is determined by the need to avoid peripheral interfaces and to meet the specific requirements of car radios, namely:

- To minimize wiring, the CMOS microcontroller and display driver must be positioned on or near the control panel close to the LCD display.
- To achieve sufficient input sensitivity to match the outputs from the tuner local oscillators, the PLL frequency synthesizer must be bipolar.
- Search tuning stop information is derived by IF counting to eliminate elaborate AM/FM window detection circuitry.
- To avoid spurious feedback and achieve unconditional stability, the IF counter must be as close as possible to the IF circuit from where it receives its input.



Development model of an electronically-tuned car radio built with the range of ICs described in this article. The control pushbuttons and LCD are in a separate unit (not shown) connected to the main radio by a cable.
(Photo by courtesy of Autosonik, Italy).

[1] Purchase of Philips I^2C components conveys a license under the Philips I^2C patent to use the components in the I^2C system, provided the system conforms to the I^2C specifications defined by Philips.

We have met these requirements by keeping the PLL frequency synthesizer separate from the MOS microcontroller and fabricating it with bipolar technology. We have also integrated the digital IF counter on the same bipolar chip as the analog IF circuit. Future steps in our continuing systems approach to increase the level of integration and minimize peripheral components will include combining the tuner and PLL frequency synthesizer circuitry.

As shown in the overall block diagram of Fig.1, the car radio, the FM and AM tuner sections are integrated in the TDA1574 and TEA6200 respectively. The AM tuner has linear wideband input circuitry which eliminates alignment and AM band switching. Spurious intermodulation products are eliminated because the linear wideband circuitry can handle the strongest signals without influencing the weaker ones. The AM IF is increased to 10.7 MHZ so that low-pass filtering can adequately suppress the image frequency and higher out-of-band frequencies.

We have also increased the integration level of the IF system and tuning interface TEA6100. Since the main function of the digital section of this IC is to determine the correct tuning point for AM/FM stations (centre of the IF bandpass characteristic) by counting the 10.7 MHz IF, AFC is no longer necessary. We have therefore been able to insert a field-strength dependent (soft) muting stage with switch-on delay between the high gain IF amplifier and the FM detector in the analog section of the IC. Although the FM detector is a highly-integrated quadrature type, the soft muting stage gives it the performance advantages of a discrete component ratio detector (good AM suppression and effective noise reduction during weak signal reception). The soft muting stage is controlled by an adjustable level from five internal IF level detectors. On FM, multipath and adjacent channel information is also derived from the level signal and can be used externally to automatically adjust the high-frequency audio response and/or control the stereo channel separation, or skip the station during search tuning.

The PLL frequency synthesizer TSA6057 is used for electronically tuning the AM and FM sections. It has a digital memory phase detector with its output applied to a programmable charge pump so that the loop gain can be software controlled to combine fast search tuning with stable locking. Two loop amplifiers allow the loop characteristics to be independently set for AM and FM.

FM TUNER TDA1574

This bipolar IC (Fig.2) contains a mixer/oscillator, a single-stage linear IF preamplifier and an AGC processor which controls the gain of an external dual-gate MOSFET RF preamplifier with selectivity determined by external varicap-tuning at its input and output. The aerial is capacitively coupled to the tuned input circuit of the MOSFET.

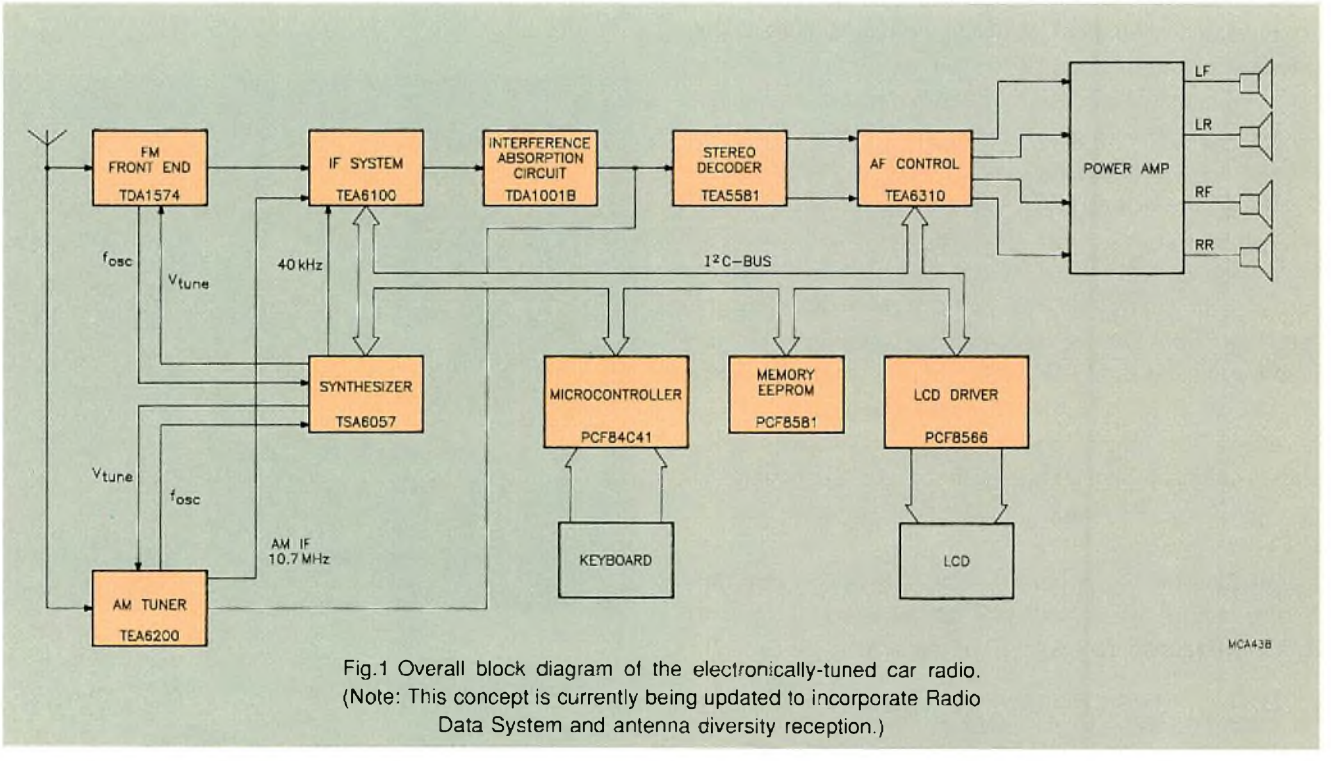


Fig.1 Overall block diagram of the electronically-tuned car radio. (Note: This concept is currently being updated to incorporate Radio Data System and antenna diversity reception.)

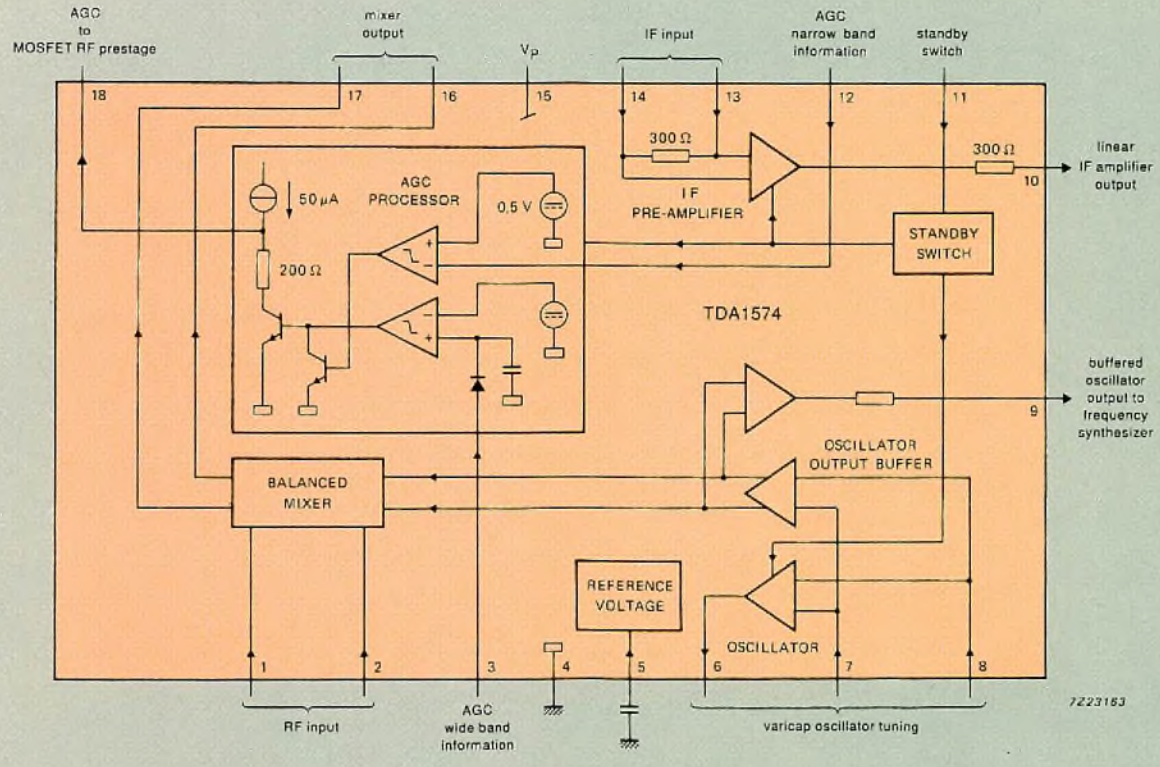


Fig.2 Block diagram of FM tuner TDA1574

The varicap-tuned oscillator is formed by a differential amplifier with an internal buffered connection to the mixer and an additional buffered output for direct connection to the frequency synthesizer. The mixer is a double-balanced multiplier to obtain good large signal handling and minimize radiation of the oscillator signal from the aerial. Its output is LC tuned for matching to an external ceramic filter at the input of the IF preamplifier. The output from the IF preamplifier is coupled to the IF system in the TEA6100 via a 10.7 MHz ceramic filter.

Additional features of the TDA1574 are:

- The AGC processor can be controlled by a combination of narrow-band and wide-band information (keyed AGC) or by narrow-band or wide-band information only.
- A stabilized reference voltage is available for setting the oscillator frequency range via a potentiometer.
- An electronic standby switch disables the oscillator, IF amplifier and AGC processor during AM reception.
- Oscillator is free of phase noise.
- Wide dynamic range and low noise figure.

AM UP-CONVERSION RECEIVER TEA6200

At the input to the TEA6200 (Fig.3), a wideband RF preamplifier with capacitive feedback eliminates the need for input tuning and LW/MW/SW band switching components. Wide aerial input dynamic range (up to at least 2 V) is ensured by internally applying the output from the RF pre-amp to a level detector. For input signal levels above 320 mV, this detector operates an internal switch which can reduce the RF preamplifier gain by using an additional capacitor to increase the negative feedback.

Since this up-conversion receiver has an IF of 10.7 MHz, the image frequency is easily suppressed by a low-pass filter between pins 20 and 2 before the RF signal is applied to a double-balanced mixer. A local oscillator LC circuit at pin 9 is varicap tuned by a tuning voltage from frequency synthesizer TSA6057.

The IF output from the mixer is transformer coupled to a ceramic filter which determines the selectivity of the system at the input to the wideband gain-controlled IF amplifier.

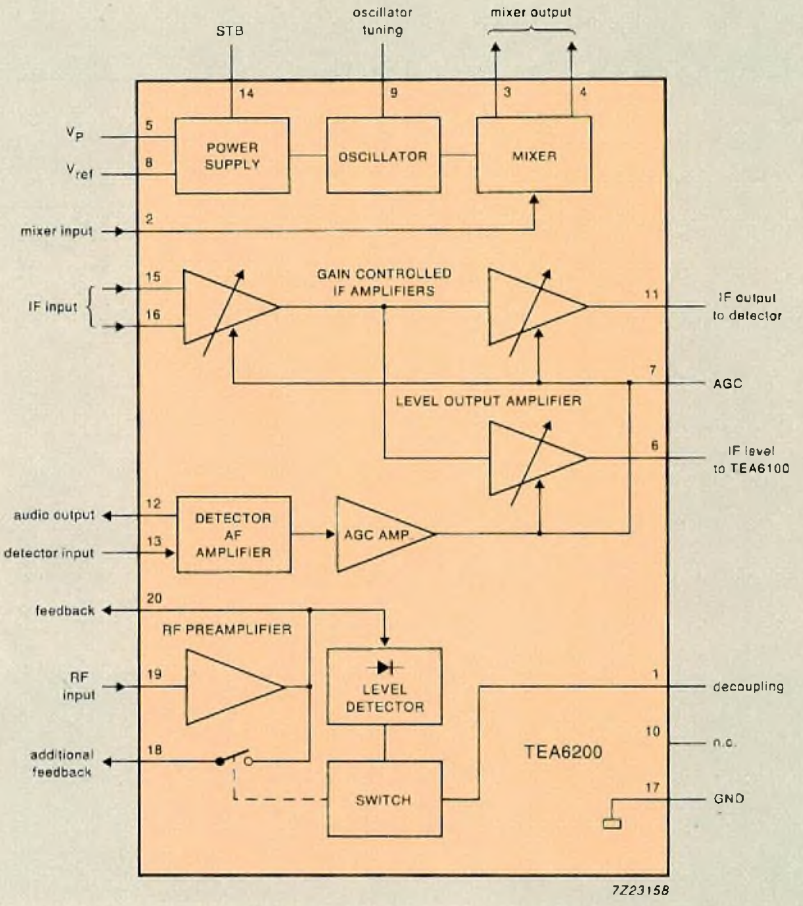


Fig.3 Block diagram of AM up-conversion receiver TEA6200

An IF signal for use in the IF system and microcomputer-based tuning interface IC TEA6100 is derived from pin 6 and passed through a ceramic filter to eliminate noise and spurious signals. Another ceramic filter at the output of the IF amplifier serves the same purpose for the IF signal before it is demodulated and passed through an audio preamplifier to the output at pin 12.

Other features of the TEA6200 are:

- The RF input is protected against lightning induced surges.
- The high IF increases the oscillator frequency so that only a small min/max capacitance ratio is required to tune it. This means that an inexpensive single diffused varicap as used for FM radios can be used.
- Doesn't require alignment.

FM IF SYSTEM AND MICROCOMPUTER-BASED AM/FM TUNING INTERFACE TEA6100

The analog FM IF system section

The analog section of the TEA6100 (Fig.4) can be software-controlled to operate in an FM or AM mode. It comprises a 4-stage symmetrical limiting IF amplifier followed by IF level detectors/amplifier and a driver for the IF counter in the digital tuning interface section of the IC. In the FM mode only, the IF amplifier is followed by a soft muting stage, quadrature demodulator and a single-ended audio output stage. The IF signals from the AM (460 kHz or 10.7 MHz) and FM (10.7 MHz) front ends are applied to the software selectable inputs of the IF amplifier, the sensitivity of which can be adjusted at pin 14 to compensate ±10 dB spreads of front-end gain.

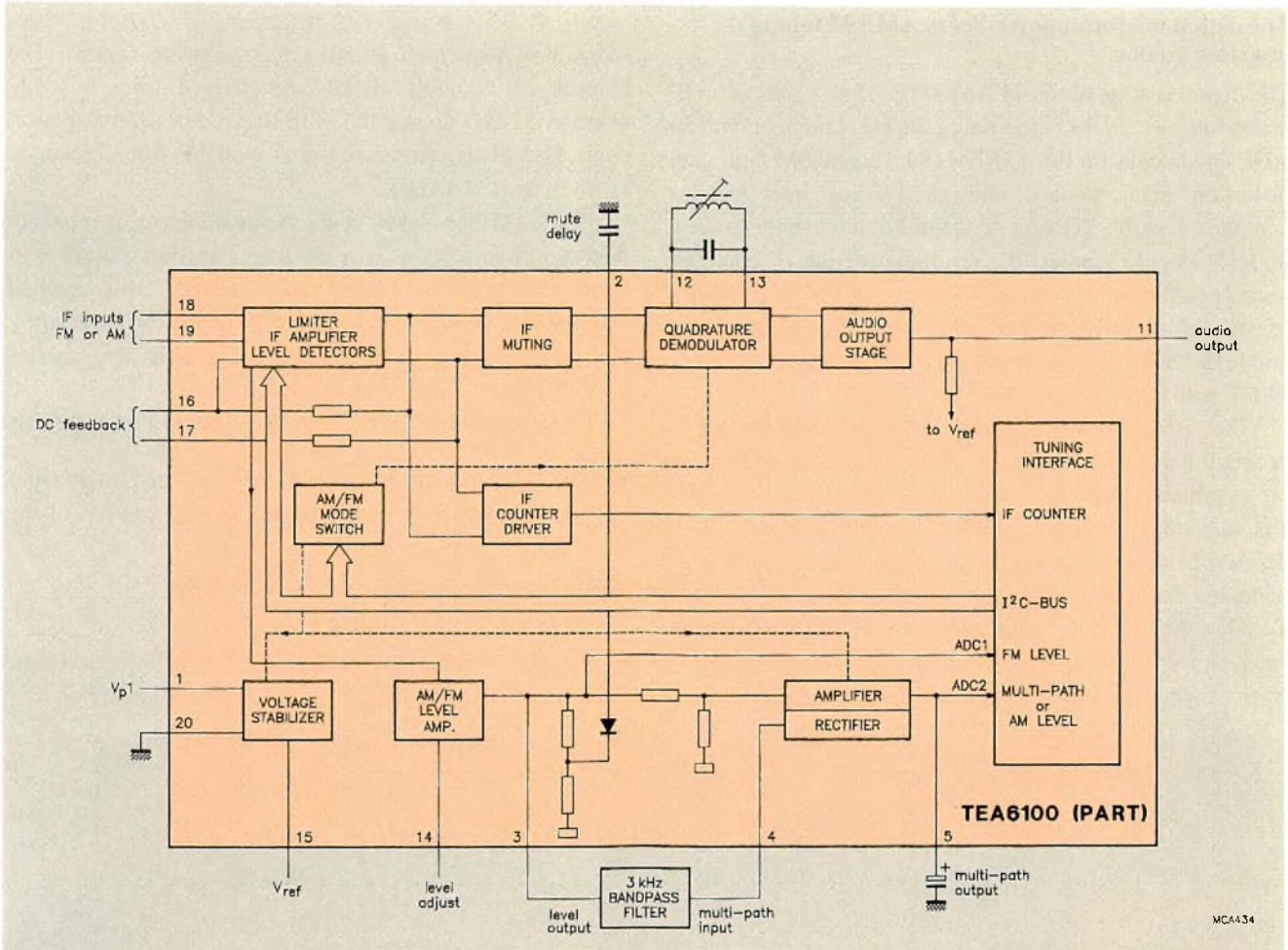


Fig.4 Block diagram of the analog FM IF system section of the TEA6100

The soft muting stage is controlled by a voltage derived from the IF level detectors which is also passed to the microcomputer via the digital tuning interface and made available at pin 3. A capacitor at pin 2 causes a delay so that the muting stage is switched on quickly and off slowly to avoid on/off effects due to rapid variations of the aerial signal. On FM, the level detectors also sense multipath and adjacent channel information which, after filtering at pins 3 and 4, is internally rectified, passed to the digital tuning interface and made available at pin 5. On AM, a capacitor at pin 5 decouples the amplitude modulation from the level information. The multipath/adjacent channel information at pin 5 during FM reception can be used to automatically adjust the high-frequency audio response and/or control the stereo channel separation, or skip the station during search tuning.

The inclusion of signal-dependent muting with switch-off delay after the IF amplifier allows considerable reduction of the number of peripheral components. This is because it allows the FM demodulator to be a highly integrated symmetrical quadrature type but adds the AM suppression and noise limiting capabilities more usually associated with a ratio detector which cannot be integrated.

Other features of the analog section of the TEA6100 are:

- A voltage stabilizer based on the band-gap principle allows the circuit to operate with a supply of between 7.5 V and 12 V.
- A reference voltage at pin 15 is switched on by software during FM operation. This is used as a source of level adjustment voltage for pin 14 on FM and allows the level adjustment voltage to be derived from an external source on AM.

The digital microcomputer-based AM/FM tuning interface section

The digital section of the TEA6100 (Fig.5) consists of an IF measuring system for determining the exact tuning point, an ADC and latches for the AM/FM IF level and FM multipath distortion level signals, and an I²C-bus interface for computer control. Because of the different channel spacing of AM and FM signals, the resolution of the IF counting must be adjustable. A unique feature of this IC is its ability to count a 10.7 MHz AM IF with a resolution of 500 Hz, a 460 kHz AM IF with a resolution of 250 Hz and a 10.7 MHz FM IF with a resolution of 6.4 kHz.

The AM/FM IF measuring system consists of a programmable prescaler, a time window circuit, a programmable timebase circuit, a 1-stage accuracy divider and an 8-stage frequency counter. The time window circuit defines the counting period. For example, if the window is wide, the counting period is long and the accuracy is high. To allow flexibility of application, a trade-off can be made between measuring speed and accuracy by switching the 1-stage accuracy divider on (wide window/slow speed) or off (narrow window/high speed) under software control. The control and window signals are derived from a stable external 32 kHz source or, as in this radio, from a quartz-controlled 40 kHz reference signal available from frequency synthesizer IC TSA6057.

The AM/FM level and multipath/adjacent channel distortion information from the analog section is applied to a multiplexed 3-bit ADC and latched. This latched information, and the 8-bit latched IF count can be read by the microcomputer via the I²C-bus which also carries control data for AM/FM mode switching.

Other features of the digital section of the TEA6100 are:

- The power supply lines are fully isolated to prevent crosstalk between the digital and analog sections of the IC.
- Prescaler programmable for AM/FM and 460 kHz/10.7 MHz operation.
- Timebase circuit programmable for AM/FM, 32 kHz or 40 kHz reference frequency and high/low resolution.

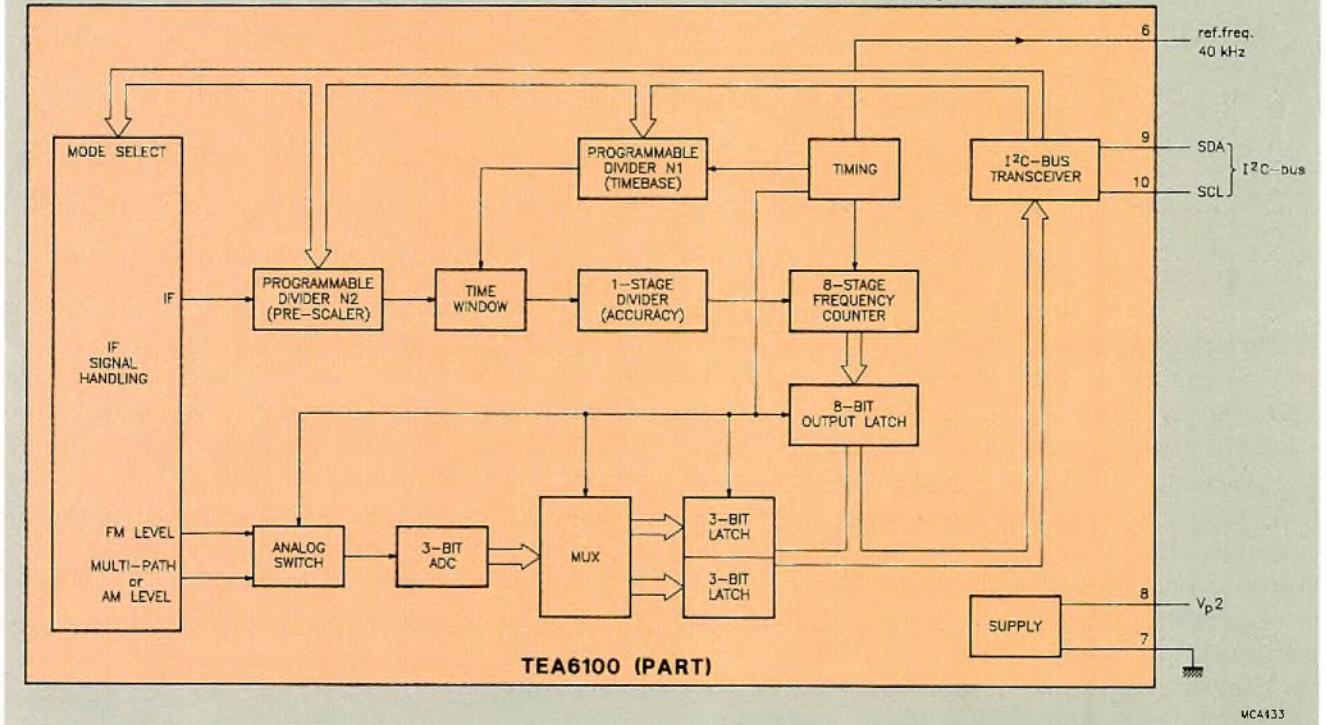


Fig.5 Block diagram of the digital microcomputer-based tuning interface section of the TEA6100

PLL FREQUENCY SYNTHESIZER TSA6057

As shown in Fig.6, this is an I²C-bus controlled AM/FM PLL frequency synthesizer with sensitive prescalers to receive VCO signals directly from the AM and FM tuners, a frequency counter comprising a 4-bit swallow counter plus a 13-bit main counter, a powerful digital memory phase detector for fast tuning and individual software-selected active loop filters for generating tuning voltages up to 10.5 V for the AM and FM tuners. The RC networks for the loop filters are external so that the loop characteristics can be individually determined for AM and FM. The IC has an operating frequency range of 512 kHz to 30 MHz for AM and 30 MHz to 150 MHz for FM. An on-chip low-distortion oscillator/counter controlled by a 4 MHz crystal generates a software-selectable internal reference frequency of 1 kHz, 10 kHz or 25 kHz for the phase detector on either AM or FM. It also generates a 40 kHz reference signal for the IF counter in the digital tuning interface section of the TEA6100.

Additional features of the TSA6057 are:

- The phase detector output is applied to programmable charge pump so that the loop gain can be software-controlled to ensure fast tuning and stable locking.
- Includes a software-controlled open-collector AM/FM switch.
- The I²C-bus interface address includes a bit that can be hard-wire programmed so that two synthesizers can be used in the same system.

INTERFERENCE ABSORPTION CIRCUIT TDA1001B

Our well-known interference and noise absorption IC TDA1001B (Fig.7) is incorporated between the IF system and the stereo decoder of the FM channel. Its operation is based on active high-pass filtering to separate the interference from the audio signal and using it to trigger suppression pulses to interrupt the audio signal after it has been delayed by an active low-pass filter. During the suppression periods, the audio output level is maintained by an external RC network. An internal 19 kHz generator sustains the stereo pilot tone during interference suppression. An AGC circuit decreases the trigger sensitivity during high duty factor interference, thereby preventing excessive audio distortion.

Other important features of the TDA1001B are:

- Operates from a supply of 7.5 V to 16 V.
- Adjustable sensitivity to interference spikes.
- After interference absorption, the peak-to-peak amplitude of the residual pulse on the audio signal waveform is less than 3 mV.
- Continues to absorb interference spikes during extremely high level noise at the input.
- Internal voltage stabilization.

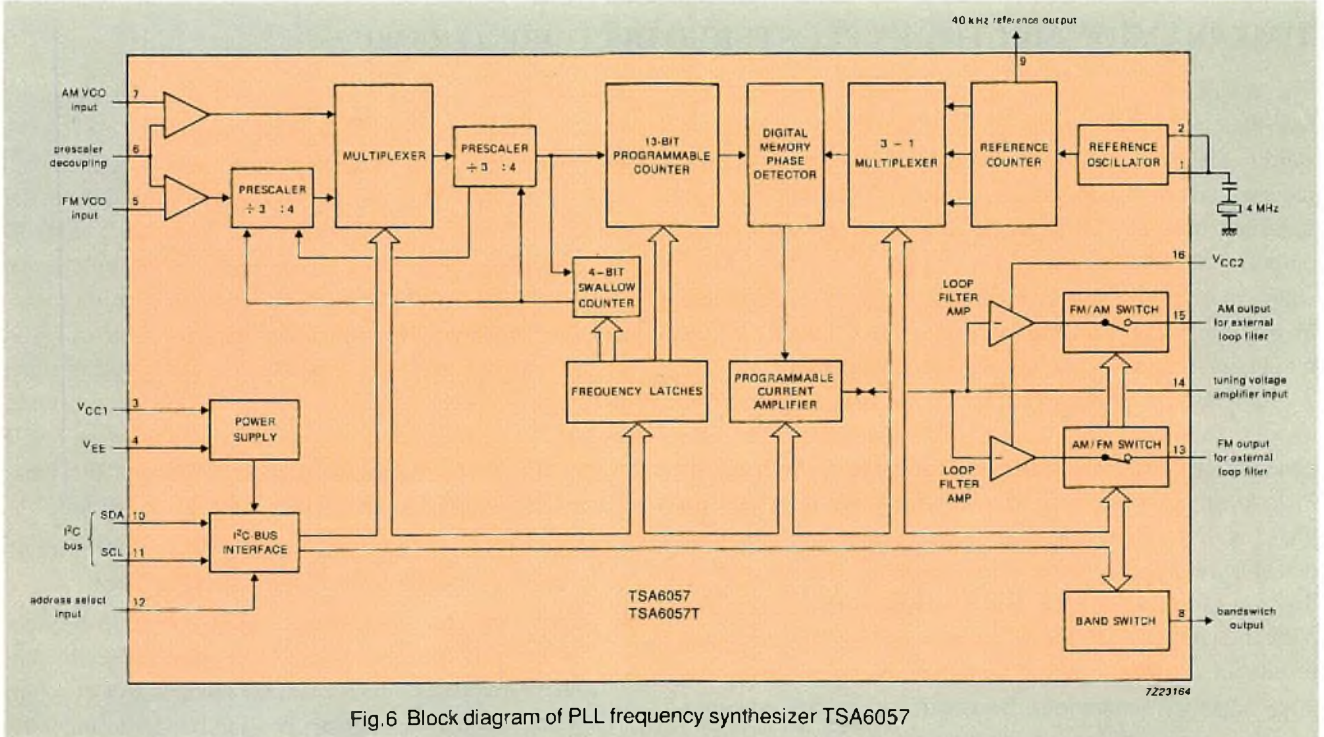


Fig.6 Block diagram of PLL frequency synthesizer TSA6057

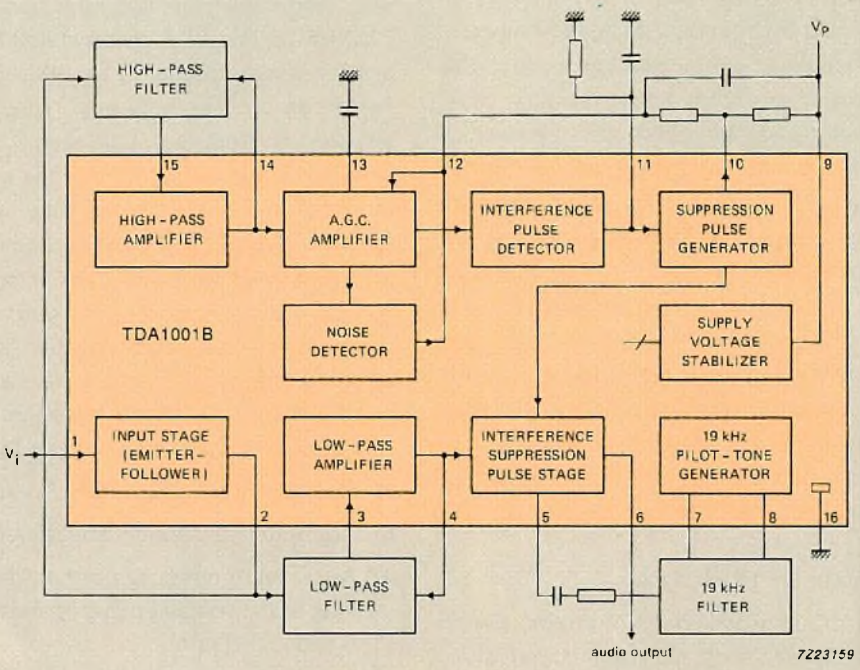


Fig.7 Block diagram of interference absorption circuit TDA1001B

TIME-DIVISION MULTIPLEX PLL STEREO DECODER TEA5581

The main function of this IC shown in Fig.8 is to extract the L-R stereo information by phase comparing the detected stereo MPX signal with a stable 38 kHz subcarrier regenerated by a PLL. The L-R information is then matrixed with the MPX signal to recover the two stereo outputs. A radio/cassette switch input allows the MPX signal to be muted so that audio signals from an AM radio or cassette player can be applied to the V_i inputs of the output buffers which can be muted for silent tuning.

In addition to regenerating the 38 kHz subcarrier, a divider following the 228 kHz VCO in the PLL also generates a 19 kHz phase detector reference for locking the PLL to the pilot tone and a second 19 kHz reference (in phase with the pilot tone and in quadrature with the phase detector reference) for a pilot presence detector which drives a mono/stereo switch and "stereo" LED driver. The perfect symmetry of these squarewave reference signals results in a high degree of interference suppression and good channel separation. However, since the reference signals are squarewaves, demodulation of odd harmonics is inevitable. To eliminate the effects of this, the frequency divider following the PLL also generates a 114 kHz reference for a second demodulator which generates a signal for suppressing the 3rd harmonic of the regenerated subcarrier. The frequency divider also generates 57 kHz for a circuit which suppresses interference caused by German traffic warning (VWF) broadcasts. The 19 kHz pilot tone is cancelled under control of the pilot presence detector before the MPX signal enters the demodulator. During weak signal reception, a signal dependent stereo (SDS) circuit, under control of a signal strength dependent signal from the FM IF system IC TEA6100, ensures smooth control of the stereo channel separation. Other features of the TEA5581 are:

- Compensation of an IF roll-off of 2 dB at 38 kHz results in 40 dB channel separation without adjustment.
- Supply voltage stabilization allows operation between 7 V and 16 V, gives excellent supply ripple rejection and a VCO frequency which is almost independent of supply voltage. The VCO can be inhibited during AM reception.

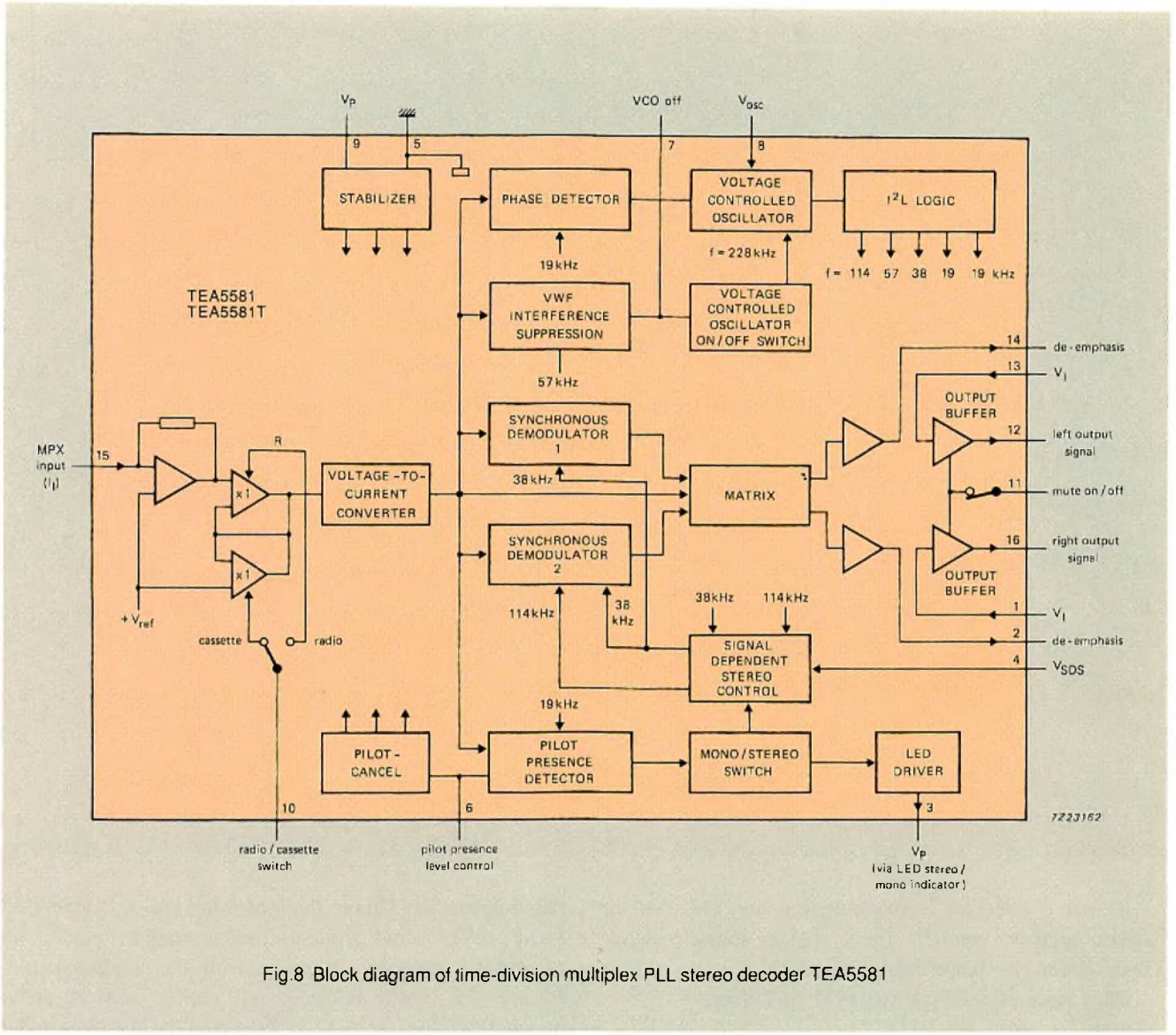


Fig.8 Block diagram of time-division multiplex PLL stereo decoder TEA5581

SOUND FADER CONTROL CIRCUIT TEA6300/TEA6310

The TEA6310 (Fig.9) consists of resistive voltage dividers connected to multi-input op-amps, the tail currents of which are digitally controlled to adjust volume level, stereo balance, bass level, treble level and fader/output selection. The advantages of this principle are very wide dynamic range combined with low noise and distortion because the gain is distributed over several stages. The low noise and distortion figures have resulted in approval for use with cassette players with Dolby B and C noise reduction.

The volume control has a maximum internal gain of 20 dB and a control range of 86 dB with a step resolution of 2 dB. The volume control also has a mute position for silent search tuning and preset station selection. The mute is automatically activated during switch on/off to eliminate switching noise. Stereo balance control is achieved by individually adjusting the volume control of the two stereo channels.

The bass and treble controls have control ranges of +15 dB to −12 dB and +12 dB to −12 dB respectively, adjustable in 3 dB steps.

The fader control is independent of the volume control and has a control range of 0 to −30 dB in 2 dB steps. It permits sound distribution adjustment between two stereo pairs audio power amplifiers (front and back) and incorporates an extra mute function to silence a speaker pair. There is also a hardware override facility to permanently silence a speaker pair in a two-speaker system. The nominal output per channel into a 5 kΩ load is 500 mV.

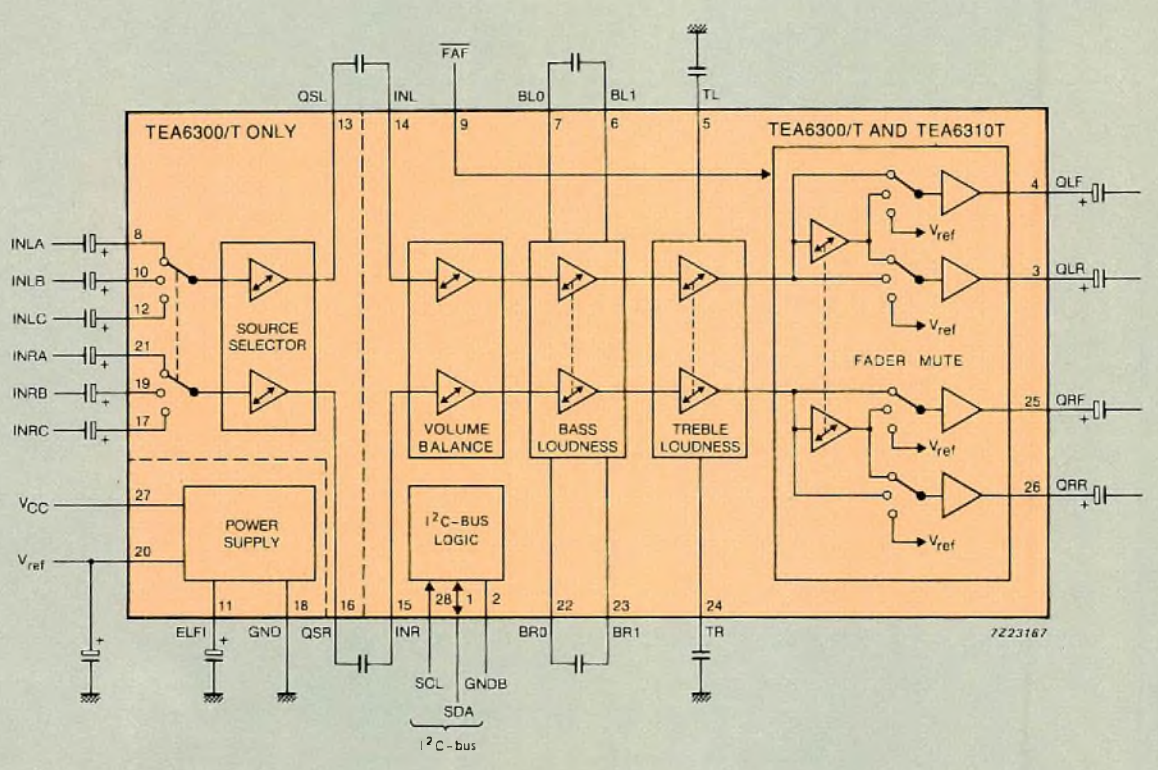


Fig.9 Block diagram of sound fader control circuits TEA6300/TEA6310

If source selection is required (e.g. for FM, AM or cassette player inputs), sound fader control circuit TEA6310 can be replaced with a TEA6300.

Other features of the TEA6300/TEA6310 are:

- THD of only 0.05% at full output over the frequency range 20 Hz to 12.5 kHz.
- Input level for clipping is >1.65 V with an 8.5 V supply and >3 V with a 12 V supply.
- Crosstalk between the I²C-bus inputs and the audio output is −110 dB.
- Typical supply current consumption is 26 mA.

CAR RADIO AUDIO POWER AMPLIFIER ICS

There is a trend in car radios toward higher audio output power because of the low efficiency loudspeaker enclosures and an increasing requirement for a wider dynamic range to suit compact disc reproduction. There is also a need to reduce the number of peripheral components because of the lack of space within the case of the radio. These requirements have led to the increasing use of Bridge-Tied Load (BTL) configurations which don't require an electrolytic capacitor in series with the loudspeaker(s). Finally, for power boosters and radios with an audio preamplifier like our TEA6310, the overall gain of the audio power amplifier need only be 20 dB instead of the 40 dB required for radios without an audio preamplifier. Our range of audio power amplifier ICs for car radios is fully described in the brochure 'Audio power amplifier ICs', ordering code 9398 369 00011.

RADIO COMPUTER-CONTROL SYSTEM CCR310S

CCR310S is a radio receiver local/remote control system based on a PCF84C41 microcontroller with a software package to control radio functions such as tuning, sound functions and keyboard decoding via the simple 2-wire bidirectional I²C-bus. It is adaptable for application in all markets.

Microcontroller PCF84C41

The PCF84C41 is a single-chip microcontroller used as the control processor for the radio. It has an 8-bit CPU, a 128-byte RAM, a 4 K ROM, an 8-bit programmable timer/event counter, a single level, three source interrupt structure and a hardware I²C-bus interface. It is in a 28-pin DIL or SO package.

A similar microcontroller incorporating an LCD driver with 24 outputs (max. 96 segments) will be available shortly. This microcontroller (PCF84C430) will be in a 64-lead quad flat-pack (SOT-208).

Universal LCD driver PCF8566

The PCF8566 interfaces to almost any LCD with low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 24 segments. It can be easily cascaded for driving larger LCDs.

EEPROM PCF8581

The PCF8581 is a 5 V 1-Kbit electrically-erasable programmable read-only memory organized as 128 bits by 8 bits.The stored information can be altered word by word.

Brief specification of the system

Tuning

- Three frequency bands; FM, MW and LW.
- Automatic store (AST) tuning for FM and AM.
- Five presets for each band (2 × 5 for the FM band).
- Manual tuning up and down.
- Search tuning up and down.
- Direct access to a preset frequency.
- Silent search tuning (no interstation noise).
- Saving of last selected band and frequency.

Display

- 48 segment LCD, 1:3 multiplex, or LED.
- Indication of frequency, band, preset programme number, stereo, AST, loudness, signal level, cassette (CR) etc.
- Indication of bass, treble, stereo balance, fader, manual tuning ('t'), programming ('p') of the EEPROM and the position of balance, fader, bass or treble.
- Blinking during the AST search.

Control

- Up to 17 control keys.

Sound

- Volume, balance, fader, bass and treble control.
- Automatic muting during search tuning.
- Loudness switching.
- Sound settings in which unique frequency responses for different wavebands are programmable. These settings are recalled after power-on reset.
- Stereo/mono switching.

Memory

- Storage of 20 presets; 10 for FM, 5 for MW and 5 for LW.
- Storage of 10 presets for AST tuning; 5 for FM and 5 for MW.
- Storage of the analog sound control settings; volume, balance, fader, bass, treble, loudness and mute control.
- Storage of the last selected band and frequency at switch off.
- Check bytes to test whether the EEPROM is programmed.

Options

- Remote control with up to 32 keys.
- Enable or disable the loudness function.
- A single key to select balance, fader, bass and treble instead of four keys.
- 5 or 10 FM presets.
- Inputs for stereo cassette player and CD player.

Power-on functions

- Check if EEPROM is programmed; if not, then program it.
- Recall the last tuned frequency, sound controls and switch settings.

Power-off functions

- If the frequency has been changed since the radio was switched off, store the new frequency in the EEPROM before going into the "idle" mode.

CUSTOMER SUPPORT

PC-controlled demonstration board

Digital tuning and control of radios via the simple 2-wire bidirectional Inter IC (I^2C) bus has brought many benefits to both manufacturers and listeners. However, it has also caused many new headaches for design and service engineers who have to quickly gain an understanding of digital techniques and software with which they were previously unfamiliar. To help solve this problem, we've now extended our radio IC applications support to embrace both hardware and software.

This extended customer support package includes a demonstration board of an electronically-tuned car radio using the ICs described in this publication, a PC-based I^2C-bus control program on a 5 1/4 inch diskette, and a user's guide. Although the radio is normally controlled by its own microcontroller, a PC is used to control the evaluation model because the keyboard and monitor display offer more and improved demonstration facilities. The demonstration package allows engineers to evaluate and test the functions of the I^2C-bus compatible radio ICs, even if they have little or no understanding of the internal software structure of the circuits. All that's needed to run the program is an IBM or compatible PC with MS-DOS/PC-DOS and at least 512 kbytes of RAM. An I^2C-bus interface board must be connected between the I^2C bus of the demonstration board and the CENTRONICS parallel printer port of the PC. The simple interface boards (for either single-master or multi-master systems) can be assembled by the user or can be ordered from Philips Components. The single-master interface (3280 version 86 06 03) is timed by the PC and operates at about 10 kHz. The multi-master interface (3530) can be set by software to operate at one of fifteen speeds between 1 kHz and 99 kHz.

The program incorporates a database containing IC control data, and a set of easy to use dedicated/universal menus for controlling the ICs. All the menus are self-explanatory and the desired functions can be accessed with a single keystroke. The dedicated menus show all the control functions of the associated IC divided into logical groups. All data communication on the I^2C-bus is subjected to error checking and, if errors occur, they're displayed on the screen of the PC as simple, easily understood messages. All data written to the register(s) of the IC are checked for illegal range and forbidden combinations with other control settings.

For information regarding the availability of the demonstration board, program diskette and interface board, please contact one of the addresses on the back cover.

PERFORMANCE OF THE RADIO

General

Supply voltage range	10.2 to 16 V
Operating ambient temperature	−30 to 75 °C
FM frequency range	87.5 to 108 MHz
AM frequency range	510 to 1650 kHz
FM IF	10.7 MHz
AM IF	10.7 MHz
FM aerial input impedance	135 Ω asymm.

FM characteristics

V_{supply} = 14.4 V, T_{amb} = 25 °C, f_0 = 98 MHz, Δf = 22.5 kHz, f_{mod} = 1 kHz unless otherwise specified. Dummy aerial as shown in Figs.10 and 11.

Aerial input voltage V_{in} (Z_s = 135 Ω asymm.)	
for −3 dB limiting (adjustable)	3 to 30 μV
for (S + N)/N = 26 dB	1.8 μV
Signal-to-noise ratio;	
over most of the frequency range	66 dB
RF signal handling capability;	
for THD < 2% at Δf = 75 kHz	> 1 V
AF output over most of the signal range;	
measured at output of TEA6100	180 mV
AM suppression;	
V_{in} = 10 μV to 100 mV	> 50 dB
THD over most of the signal range;	
Δf = 75 kHz	0.7% typ.
IF selectivity S_{300}	62 dB
IF bandwidth B_{3dB}	160 kHz
Frequency counter resolution	6.3 kHz

AM characteristics

V_{supply} = 14.4 V, T_{amb} = 25 °C, f_0 = 1 MHz, m = 0.3, f_{mod} = 1 kHz unless stated otherwise. Dummy aerial as shown in Fig.12.

Aerial input voltage V_{in}	
for (S + N)/N = 6 dB	10 μV
for (S + N)/N = 20 dB	50 μV
for (S + N)/N = 26 dB	110 μV
for P_o = 500 mW	5.4 μV

Signal-to-noise-ratio	
for V_{in} = 1 mV	45 dB
AGC range	
V_{in}/500 mV for 10 dB variation of AF output	90 dB
RF signal handling capability	
at m = 0.8, THD < 10%	3 V
THD over most of the AGC range	
m = 0.8, f_{mod} = 400 Hz	< 2%
Total bandwidth B_{3dB}	5 kHz
Fidelity (−3 dB)	30 Hz to 2 kHz
IF suppression	
tuned frequency 1400 kHz, V_{in} = 20 µV	62 dB
Image rejection	
tuned frequency 1400 kHz, V_{in} = 20 µV	76 dB
Frequency counter resolution	500 Hz

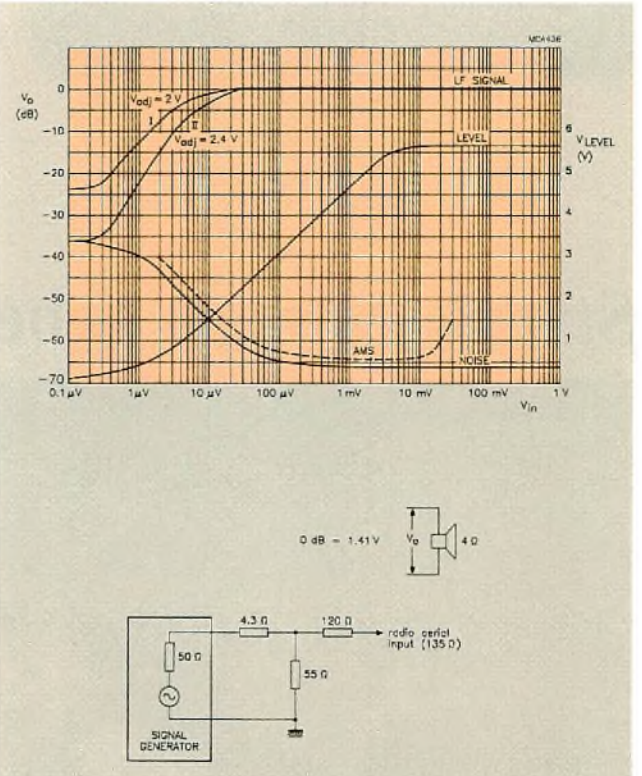


Fig.11 LF output and level signal performance of the FM channel

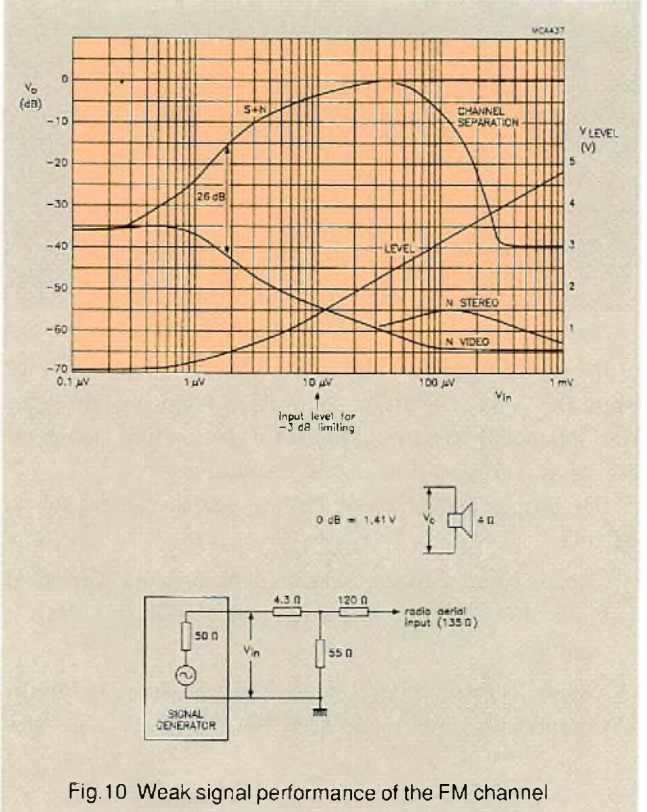


Fig.10 Weak signal performance of the FM channel

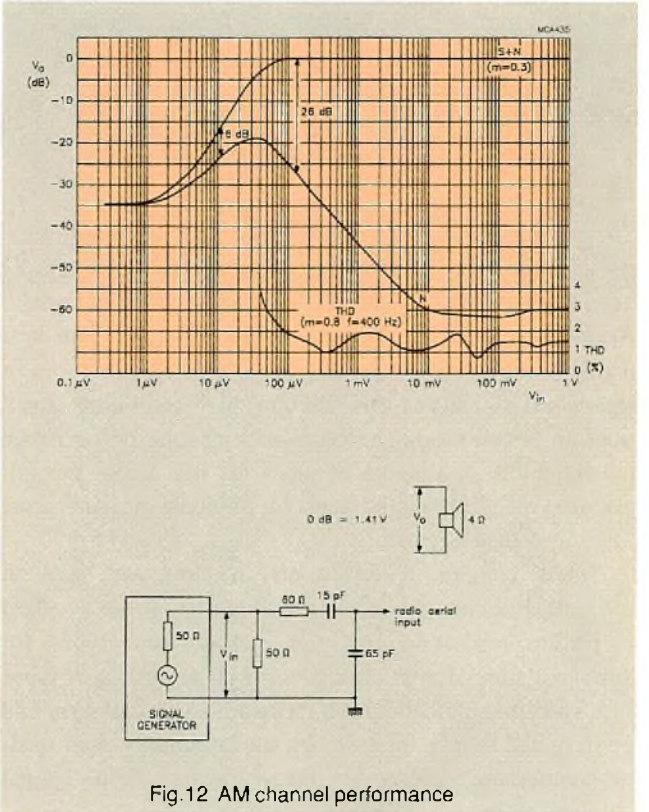


Fig.12 AM channel performance

Product profile

Streak camera tubes

World-class scientific research projects demand the best available technology in all engineering disciplines. And in high-speed signal analysis, Philips' high-resolution streak tubes are second-to-none. Renowned for their performance and reliability, our range of tubes for use across the full spectrum meets all requirements for photonic measurements down to a picosecond.

Streak camera manufacturers in particular have an unequalled choice of tubes with which to set the standard in picture resolution and can choose from types for combined streak/frame cameras as well as dedicated types for a specific application. All tubes are easy-to-control and are designed to take into account the commonly-used read-out equipment, preferred image formats and optical coupling of today's cameras.

Shown here are the P510 (left) and P920 tubes for use in the visible spectrum. Besides 'visible' tubes, tubes for use in the X-ray spectrum are available and include types with bilamellar electron optics for picosecond temporal resolution and ultra-fine spatial resolutions.

For further details about Philips' streak camera tubes, ask for:

- 'Streak camera tubes.' Philips Components Technical Publication DC001, ordering code 9398 075 40011, June 90.
- 'Streak camera tubes' (short-form catalogue), Philips Components, ordering code 9398 372 80011, July 90.

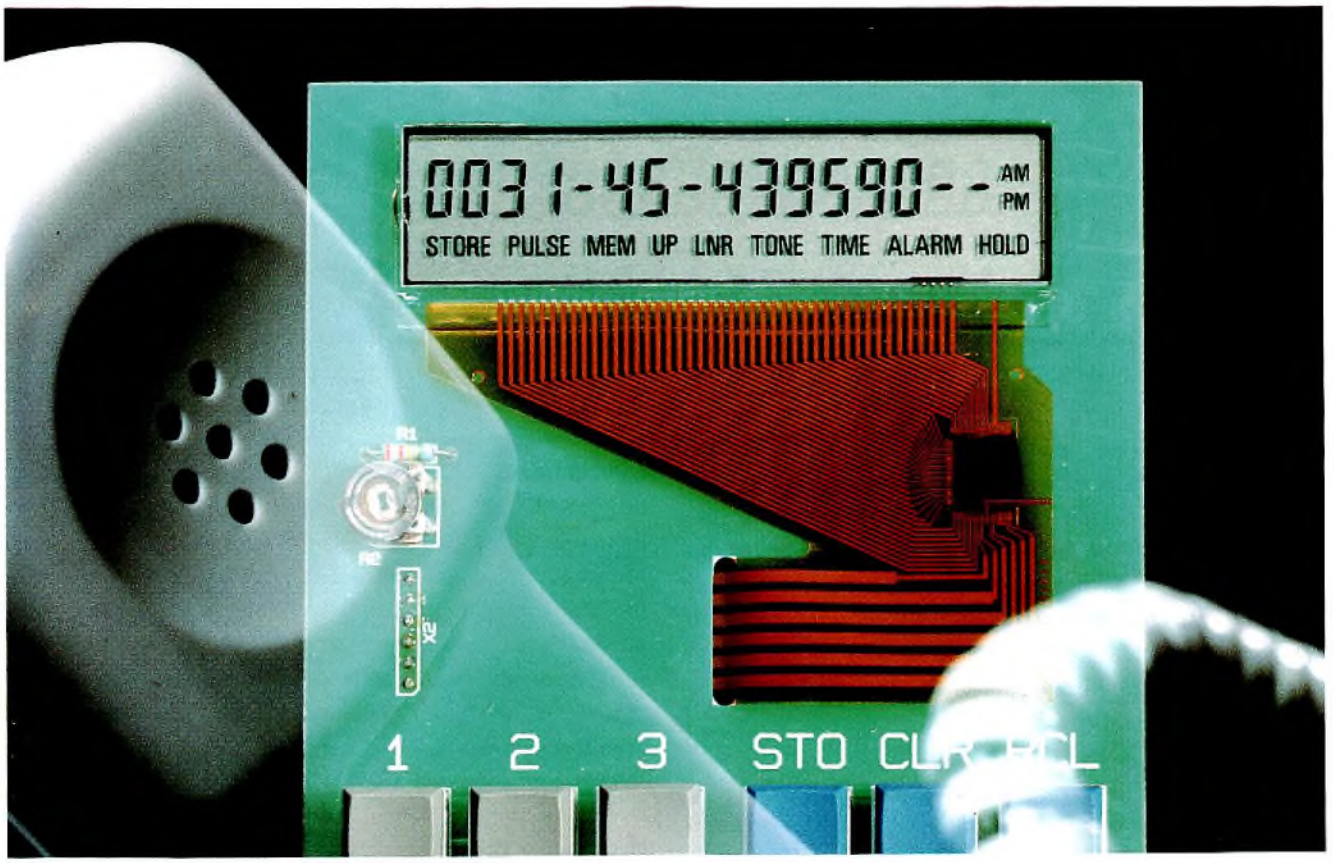
Chip-on-foil – the flexible approach to LCD modules

WIM STIJNS

Today's technology allows increasingly complex electronics to be accommodated in smaller modules. Products such as telephones, pagers and cellular radio sets are now pocket sized and offer a whole range of functions. There is a growing demand for improved display facilities for these articles to simplify their operation and enhance their aesthetic appeal.

There's no doubt that LCDs will continue to be the first choice display for these applications: they're thin and lightweight, consume little power and have proven popularity with consumers. But as more electronics is squeezed into smaller packages, what's needed is a new method for connecting the drive electronics to the LCD that uses the minimum of space and offers improvements in reliability and cost.

In conventional LCD modules, the driver IC is mounted on a PCB at the rear of the display, and connected to the LCD via soldered fixed-pins or clamped-on elastomer connectors. This method more than doubles the overall thickness of the display, so the exceptionally thin profile of an LCD is not fully exploited. A lower profile display, at the expense of increased width, can be made by connecting the PCB with a length of flexible foil (known as flexfoil). However, for all these conventional mounting systems, the quality of the bonds in every connection from the driver IC to the LCD can be improved. Bond quality



is especially important in LCDs, which need a large number of connections for individual control of every display segment.

Chip-on-foil offers a new way of integrating the LCD with the driver circuitry as a single, very thin unit that can be mounted in a fraction of the space used by PCB-mounted displays. In chip-on-foil, the LCD driver chip is bonded directly to a piece of flexfoil which in turn is bonded to the LCD. This arrangement offers a significant improvement in reliability, since all the bonds used to connect the chip to the LCD are sealed and protected from the environment.

The following features have prompted manufacturers to use chip-on-foil modules for their display requirements:

- *small and lightweight* – with chip-on-foil technology, the weight and volume of the LCD/driver combination is minimized
- *flexible mounting* – the flexibility of the flexfoil allows it to be clamped in almost any position, however small or awkward, according to the requirements of the housing[1]. Alternatively, the low weight of the flexfoil and the strength of the bonding allows the circuitry to be totally free-standing, requiring no support at all
- *high reliability* – the LCD and driver electronics are irreversibly bonded together as a single continuous unit. This gives it better resistance to vibration, temperature effects and mechanical stress so that the user is not concerned with maintaining or protecting the connection
- *product adaptability* – the nature of the connection between the flexfoil and driver IC allows the same flexfoil design to be used for a range of LCD modules including dot-matrix displays which may require two drivers cascaded on the same bus
- *facilitates back-lighting* – with the flexfoil mounted to one side of the LCD, a greater choice of back-lighting systems is available than for conventional PCB-mounted displays.

The maximum benefit from chip-on-foil technology is gained when I²C-bus[2] compatible LCD drivers are used. Developed and patented by Philips as a universal system for interconnecting microcomputers and peripherals, the I²C-bus concept allows all communication to be carried out over two lines. Combining I²C-bus with chip-on-foil technologies reduces the total number of connection terminals required for supply and control of the LCD module. This simplifies connection and minimizes the surface area of the flexfoil.

1. The foil must not be bent over a radius of less than 4 mm.
2. Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

CHIP-ON-FOIL FABRICATION

To make chip-on-foil modules to a high standard we developed new methods to join the driver chip to the flexfoil and the flexfoil to the LCD. All connections must meet the following rigorous requirements:

- high performance electrical characteristics – no noise or crosstalk
- high mechanical strength
- resistance to corrosion and other chemical effects
- resistance to humidity and temperature variations.

Figure 1 illustrates the manufacturing steps we use to make chip-on-foil modules.

In developing our chip-on-foil design we've been able to fully exploit a recent Philips breakthrough in IC fabrication known as Tape Automated Bonding (TAB). Because TABed chips are mounted on polyamide foil they can be readily bonded to the flexfoil used in chip-on-foil technology.

Tape Automated Bonding (TAB)

TAB allows high lead-count ICs to be manufactured in low-profile surface-mount technology and is ideally suited for LCD controllers. TABed ICs are directly bonded to and supported by a polyamide carrier tape. The tape has sprocket holes in a movie-film format to facilitate fully automated control of the ICs during both fabrication and placement. The tape is prepared from a laminate of polyamide and copper. The copper is etched to provide connection tracks for ICs and plated with gold or tin for corrosion protection. The polyamide is then etched to leave square openings (slightly larger than the dimensions of the IC) such that the copper leads overlap and form inner-leads for connecting an IC placed in the middle (see Fig.2). Openings are also etched to form outer connection leads.

Before the IC is bonded to the inner leads (in a process known as inner-lead bonding) it is hermetically sealed with a corrosion-proof passivation layer and plated with gold bumps at the connection terminals. The inner leads are bonded to the gold bumps by thermocompression bonding using a heated thermode under pressure (Fig.3). The thermode aligns its four heated blades with the IC, picks it up with a vacuum sucker and positions it precisely over the leads on the tape. A computer then controls the pressure and temperature applied to the thermode to simultaneously bond all leads to the chip. The use of pulsed heating (Fig.4) minimizes thermal effects to achieve a uniform, highly reliable bond.

After inner-lead bonding, the ICs are tested by applying probes to connector pads at the outer ends of the printed leads and rejects are punched out of the carrier tape.

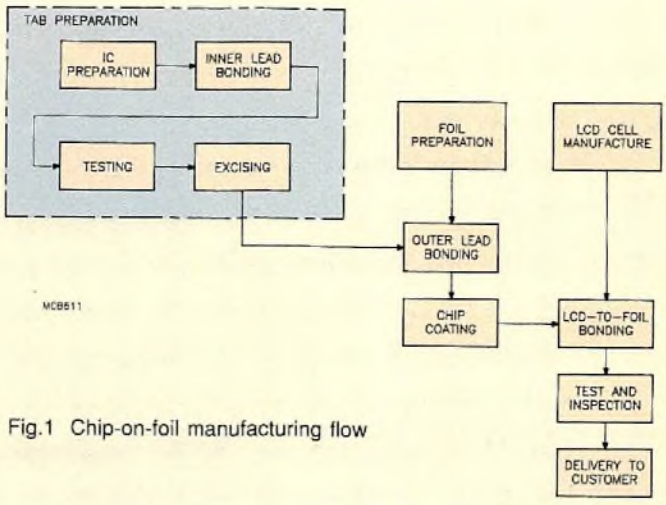


Fig.1 Chip-on-foil manufacturing flow

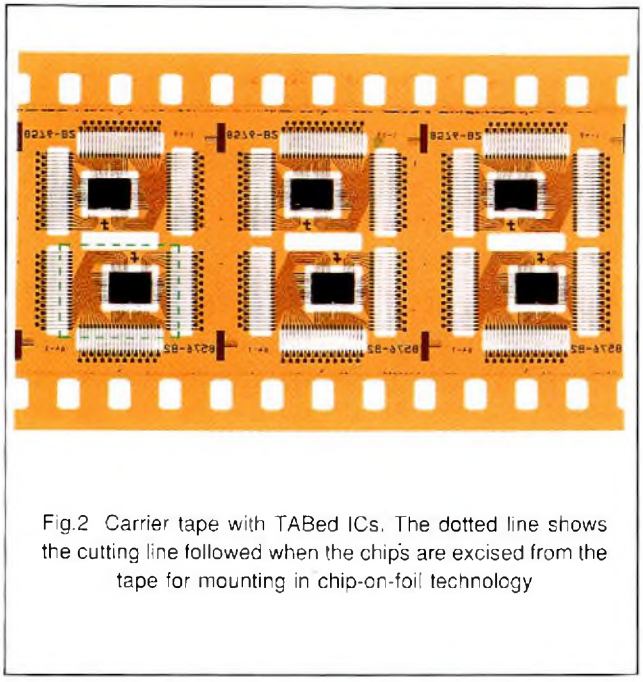


Fig.2 Carrier tape with TABed ICs. The dotted line shows the cutting line followed when the chips are excised from the tape for mounting in chip-on-foil technology

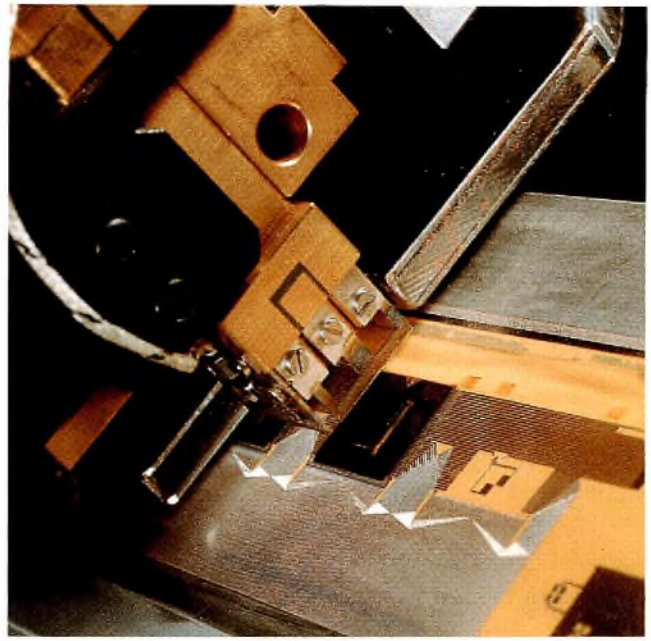


Fig.3 Thermode for use in TAB.

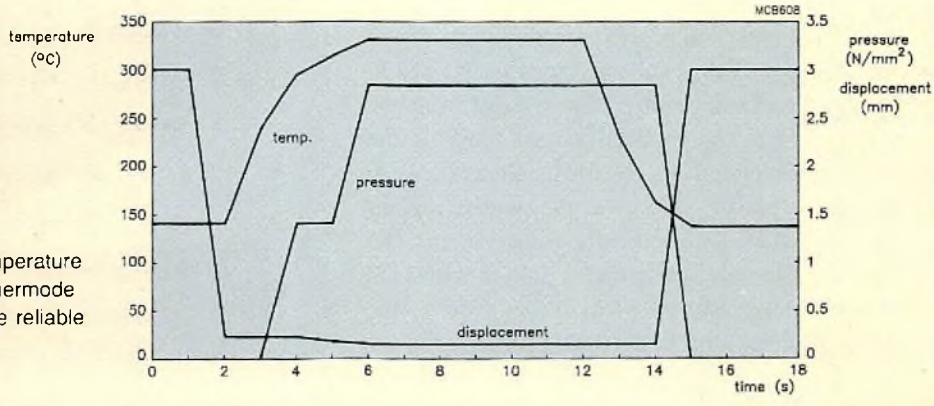


Fig.4 During bonding, the temperature and pressure applied by the thermode is carefully controlled to ensure reliable bonding of IC leads

Foil manufacture

For our chip-on-foil technology we use polyamide foil for its flexibility and resistance to the high temperatures incurred during bonding of the IC, LCD and external connectors. Starting with a sheet of polyamide/copper laminate, copper tracks are etched out and the foil is cut to the required dimensions. The tracks are given a lead/tin solder plating and a plastic coating for UV protection and corrosion resistance.

Chip-to-foil bonding

TABed chips are excised from their supporting tape by cutting the outer leads. (see Fig.2). Before making electrical connection of the TAB's outer leads to the tracks on the flexfoil (outer-lead bonding), the TAB film is glued to the flexfoil with the connectors pads and conductive strips aligned and facing each other. In a similar process to that used in TAB, a thermode is used to press the connectors together at a temperature high enough to form a permanent soldered bond.

Finally the chip is covered in a black epoxy resin for scratch protection and prevention of chemical contamination. This also gives extra strength to the connecter leads.

LCD-to-foil bonding

The LCD is connected to the driver chip via ITO (indium tin-oxide) contacts on a ledge formed by the wider of the two glass plates that make up the liquid-crystal cell. For chip-on-foil displays, this ledge must be at least 3.8 mm wide to provide sufficient contact area for the flexfoil bond and to prevent the cell itself from being damaged during the bonding process. The contact strip at the edge of the foil is coated with a thermosetting plastic (such as polyamide) which has been imbedded with conductive particles of gold, nickel, tungsten carbide or carbon fibres. The particles are evenly and thinly dispersed so the plastic acts as an insulator.

The flexfoil and LCD cell are positioned with the conductive tracks aligned and pressed together with a heat-seal bar comprising a silicone rubber coated bar heated to 180-200 °C. As the plastic melts, it runs away from the narrow regions close to the conductive tracks leaving the conductive particles which make electrical contact between them. The excess plastic flows to the wider regions between the conductors to electrically isolate them. The resulting bond is extremely strong and is able to withstand a peeling force of at least 500 g/cm. What's more, the bond is totally insulated and is not liable to corrosion or the effects of dust particles. Figure 5 shows the principle of LCD-to-foil bonding.

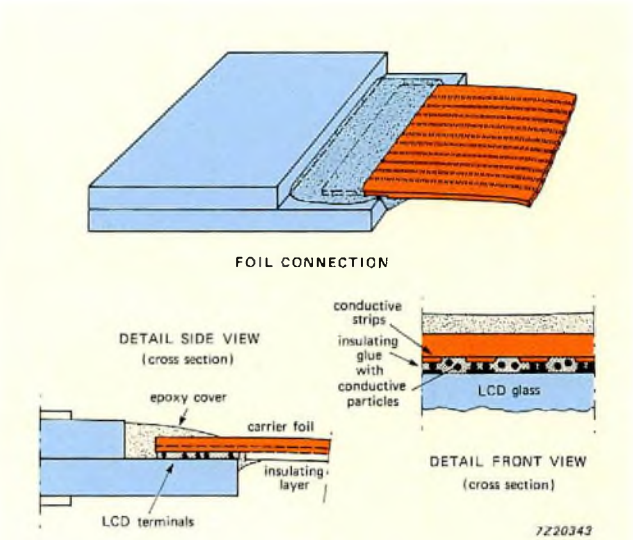


Fig.5 The LCD and foil are bonded together by a particle-impregnated glue which only conducts between the contact strips

DISPLAY DESIGN WITH CHIP-ON-FOIL MODULES

Introducing the LP-3566-B telephone display

To illustrate the design requirements to control Philips' chip-on-foil modules, the following guide takes the LP-3566-B (Fig.6) telephone display as an example. Although designed specifically for telephones, the LP-3566-B is a variation of a standard cell which can be customized to the requirements of the user.

The cell is an 80 × 25 mm display comprising 16 numeric characters and 11 function words for indicating

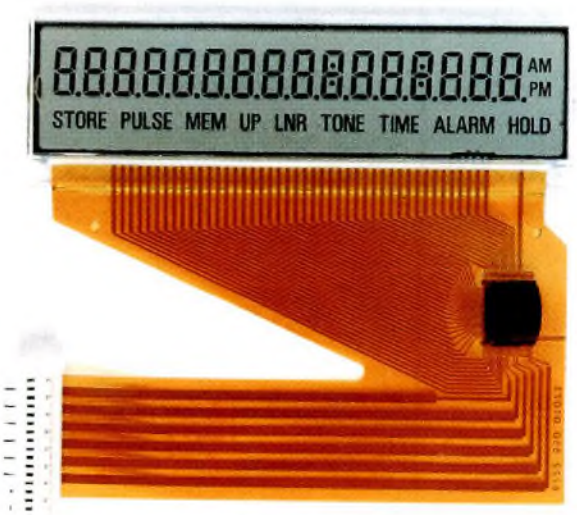


Fig.6 The LP-3566-B with all segments driven on

various telephone control modes. It requires a 1:4 multiplex drive at 1/3 bias.

The cell is driven by Philips PCF8576 universal driver IC mounted in chip-on-foil technology on a 100 mm wide flexfoil with six connection terminals. The driver features I^2C-bus interfacing with control electronics, such as a microprocessor, and is suitable for almost any LCD requiring a low multiplex ratio.

Connecting the LP-3566-B

Only six lines are needed to connect the LP-3566-B to the supply voltages and control electronics. Connection is via parallel copper tracks at the edge of the flexfoil using one of the connection methods illustrated in Fig.7.

Figure 8 shows all connections to and from the PCF8576 including the recommended values for external supply voltages and resistors. The value of pull-up resistors R_p must be selected from a range of 1.5 to 10 kΩ according to the capacitance of the I^2C-bus and the ICs connected on it. V_{LCD} determines the LCD operation voltage (V_{op}) according to $V_{op} = V_{DD} - V_{LCD}$. Voltage level V_{LCD} should be adjusted for the optimum contrast of on and off character segments. Also, if the display is to be operated in a variable temperature environment (e.g. for outdoor use), V_{LCD} must be compensated for temperature fluctuations (see Box 1).

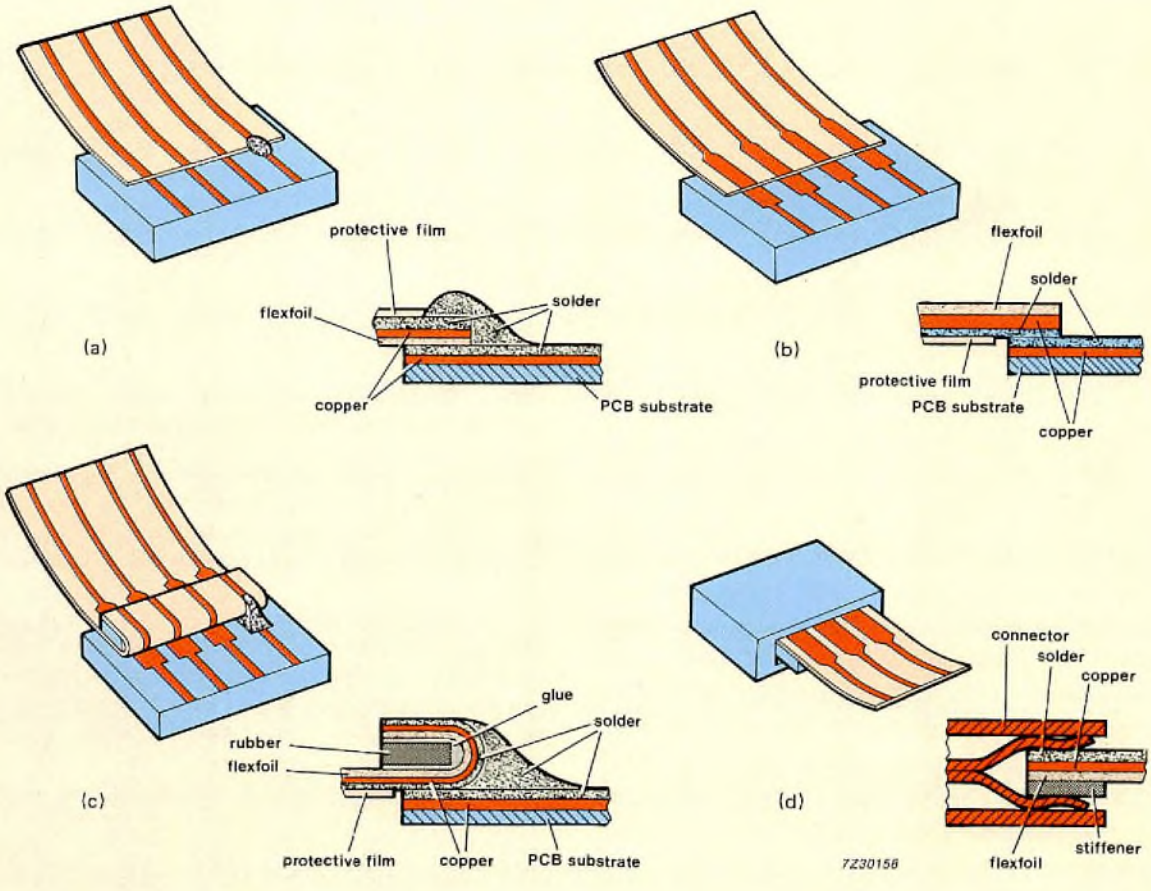


Fig.7 Connection techniques for chip-on-foil:
(a) soldered connection suitable for reflow and dip soldering.
(b) soldered connection made under high pressure.
(c) fold-over solder joint for conventional soldering – a glued on rubber insert allows the end of the foil to be folded back provide a continuous metal profile over which the solder joint is formed.
(d) spring-clip connection – gluing an extra layer of foil at the connection edge gives the foil sufficient strength to allow connection using a spring-clip connector like the one shown. Suitable connectors for chip-on-foil modules are made by Burndy, Dupont, Molex and Noble

Recommended values	
V_{DD}	5 V
V_{SS}	0 V
V_{LCD}	= 1.9 V
R_{osc}	180 kΩ
R_p	1.5 ... 10 kΩ

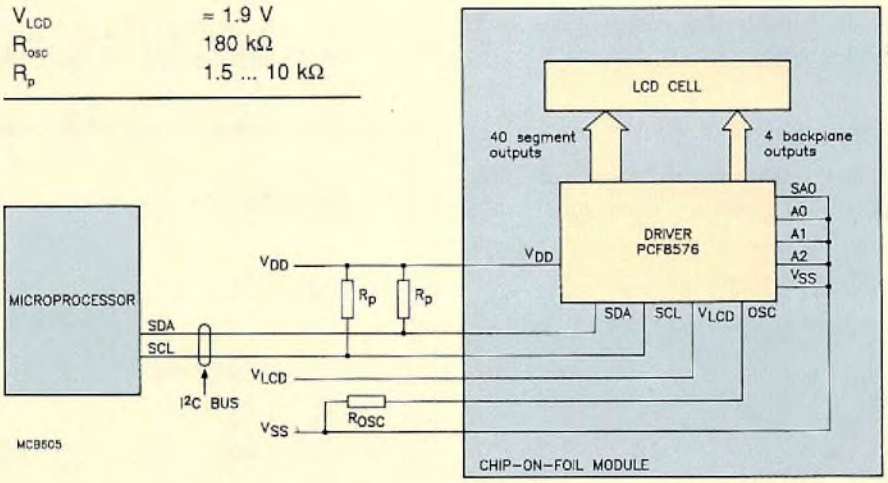


Fig.8 By using an I²C-bus to carry all the control signals from the control electronics, the LP-3566-B requires only six external connections

R_{OSC} determines the internal clock frequency (f_{CLK}) of the PCF8576 according to:

$$f_{CLK} = \frac{3.4 \times 10^7}{R_{OSC}} \text{ kHz}$$

This sets the rate of data exchange within the chip and the frame frequency of the display. The choice of R_{OSC} depends on the power mode (see Table 1). In power-saving mode (selected by a command byte on the I²C-bus) f_{CLK} is reduced by a factor of six for the same frame frequency. The reduced clock frequency and the increased value of R_{OSC} together significantly reduce power dissipation. With a lower clock frequency the response time will increase at high data rates but the I²C-bus protocol ensures that no data loss occurs.

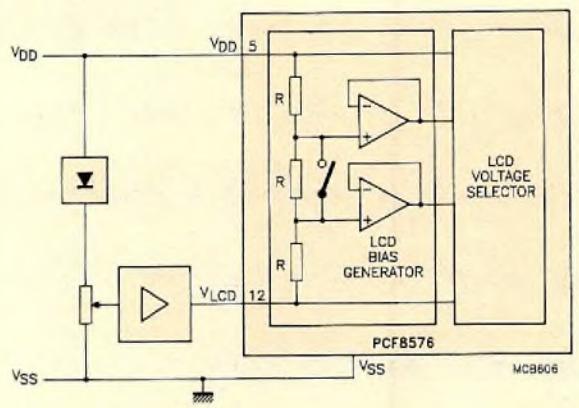
TABLE 1
Selection of clock frequencies according to power mode

power mode	recommended R_{OSC} (kΩ)	f_{CLK} (kHz)	f_{frame} (Hz)
normal	180	190	64
power-saving	1200	31	64

BOX 1: TEMPERATURE COMPENSATION

For a consistent contrast display in fluctuating temperature conditions, the LCD supply voltage (V_{LCD}) for the LP-3566-B must increase with temperature at 14 mV/°C. The figure shows the operating principles of a suitable temperature compensation circuit.

The amplifier supplies a stable voltage source (V_{LCD}) to the LCD bias generator of the PCF8576. With increasing temperature, the resistance of the diode circuit decreases so that the amplifier input voltage rises. The amplifier output provides the required rate of voltage increase in V_{LCD} with temperature.



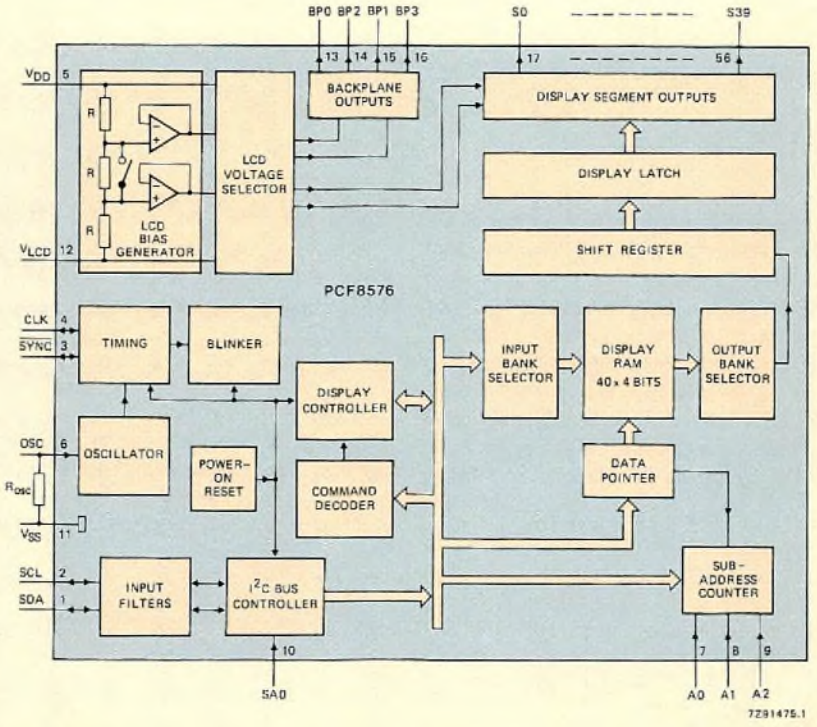


Fig.9 Block diagram of Philips PCF8576 universal LCD driver for low multiplex ratios

The PCF8576 universal LCD driver

Figure 9 is a block diagram of the PCF8576 universal LCD driver. In response to commands and data received on the I²C-bus from a microprocessor or other controller, the PCF8576 sends drive signals to the LCD to produce the desired display. The display message is stored in display RAM using an auto-incrementing address system which simplifies communication.

The LCD is controlled by backplane and segment outputs. The backplane outputs are switched automatically by the LCD voltage selector according to the required multiplex ratio and the selected clock frequency. The forty display segment outputs are controlled according to the contents of display RAM.

I²C-bus interface

The PCF8576 acts as a slave receiver on the I²C-bus system and therefore doesn't initiate bus transfers or transmit data. It only responds when the I²C-bus sends a start condition (see Box 2) followed by an address byte including its slave address. Two I²C-bus slave addresses (0111000 and 0111001) are reserved for the PCF8576 to allow two different types of LCD to be controlled on the same bus. The lowest significant bit (LSB) is determined by the level of input SA0. In the LP-3566-B, SA0 is tied to ground to give slave address 0111000.

Figure 10 shows the protocol used for sending command and data bytes to the PCF8576. The LSB of the address byte (the R/$\overline{W}$ bit) is set to logic 0 indicating that further bytes are to be sent to the PCF8576. After each byte is received, the PCF8576 must respond with an acknowledge bit (see Box 2).

The next byte sent to the PCF8576 must be a command byte. The MSB of each command byte (bit C) is known as the continuation bit and determines whether the next byte sent is a command (bit C = logic 1) or a data (bit C = logic 0) byte. A message string can comprise any number of command and data bytes and is terminated by a STOP condition from the transmitter (see Box 2).

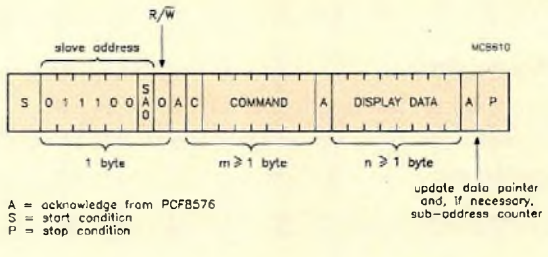


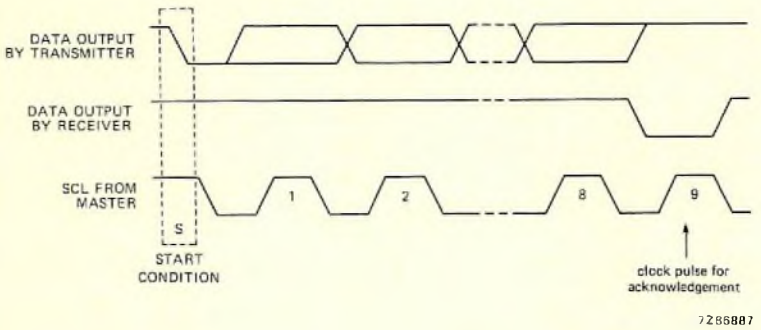
Fig.10 I²C-bus protocol

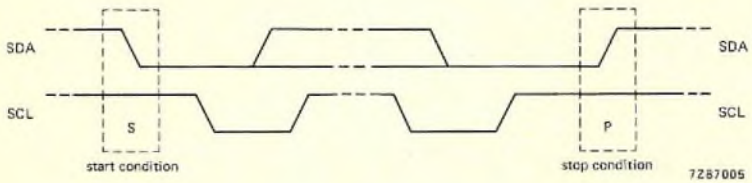
BOX 2: I²C–BUS OPERATION

The I²C-bus allows communication between any number of ICs using only two bidirectional lines known as the SDA (serial data) and SCL (serial clock) lines. Communication is on a master-slave basis with each IC having a unique address. The I²C-bus is a multi-master system and uses an arbitration system to determine which master IC takes control of the bus. SCL carries the clock signal from the master to set the rate at which data is sent over SDA. Data on SDA is valid during the high period of SCL. After each byte of data the receiver is obliged to return an acknowledge signal to the transmitter by pulling down SDA to logic 0 during the next high period of SCL (see Fig.A). A master initiates and terminates data transfer by making START and STOP conditions as follows (see Fig.B):

- START condition: A HIGH to LOW transition while SCL is HIGH
- STOP condition: A LOW to HIGH transition while SCL is HIGH.

For more detailed information refer to "The I²C-bus Specification"; Order No. 9398 358 10011.





Command bytes

The operating status of the PCF8576 is set by the command bytes received on the I²C-bus. These determine the following:

- the *multiplex ratio* – this can be 1:2, 1:3, 1:4 or static drive
- *the LCD bias* – 1/3 bias (normal operation) or 1/2 bias (low-voltage operation)
- the *power mode* – a choice of normal or power-saving mode
- *data input control* – determines the memory locations for storing incoming data
- *blinking* – the whole display can be switched on and off at one of three blinking frequencies, or by external control.

Figure 11 defines the command bytes used by the PCF8576.

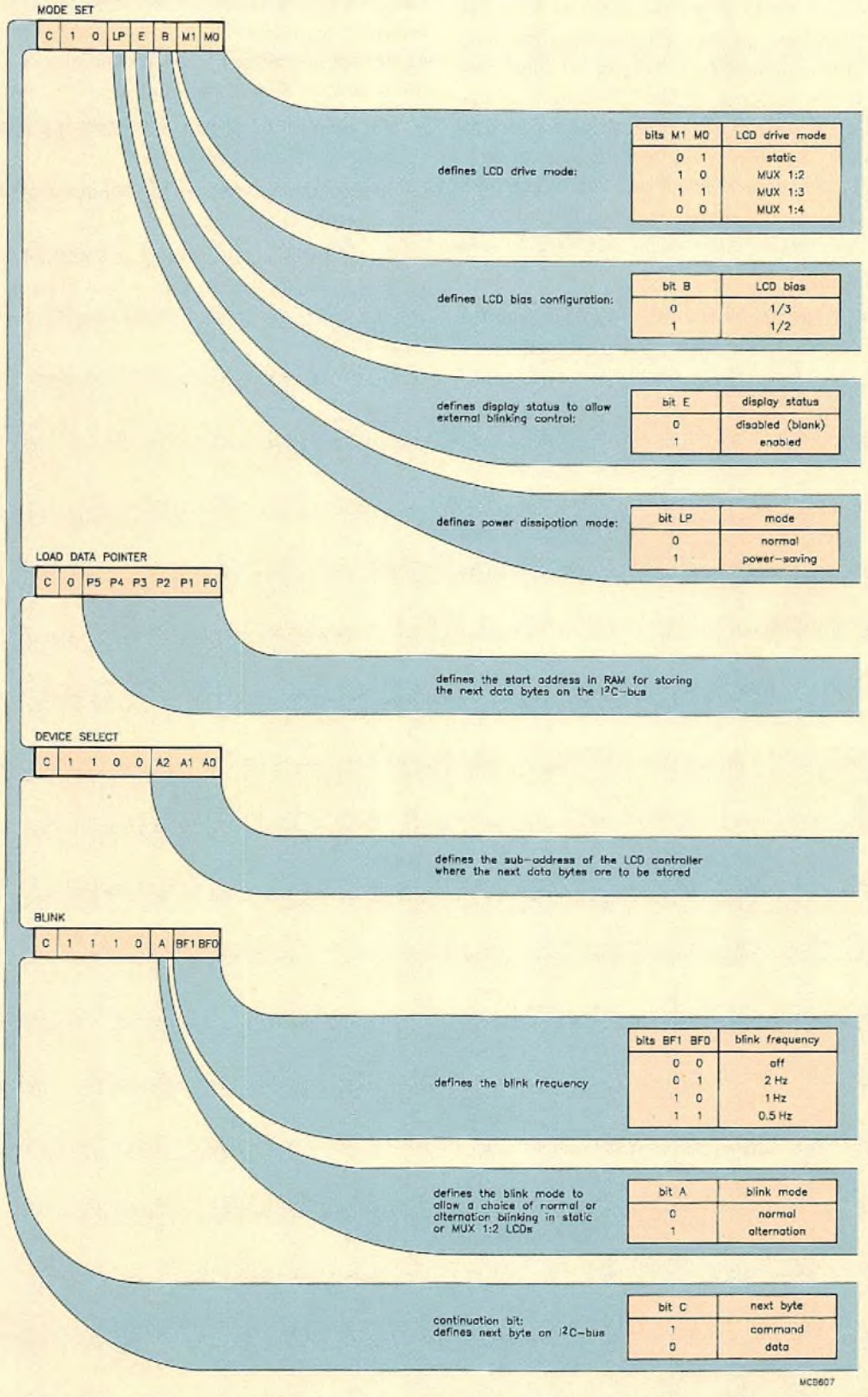


Fig.11 Command byte set for controlling the LP-3566-B

LCD drive

The drive voltages for the LCD are controlled by the LCD voltage selector according to the multiplex ratio and bias level chosen by the command bytes. Figure 12 illustrates the drive waveforms required by the LP-3566-B which operates at MUX 1:4 and 1/3 bias. With these waveforms the RMS voltage at any display segment has one of only two values: one for a dark segment and the other for a light segment. This ensures an even contrast display.

Memory organization

The key to the efficient operation of the PCF8576 is in the organization of display data in RAM. Data representing the required display pattern is stored in 40 × 4-bit RAM such that each bit represents the on (dark) or off (clear) state of a display segment with logic 1 or logic 0 respectively. To enable auto-incrementing addressing, the PCF8576 handles the data according to the multiplex ratio such that:

- the number of display bits stored at each address is equal to the multiplex ratio
- the location of display bits within a memory location corresponds to a backplane.

Since the LP-3566-B operates at a multiplex ratio of 1:4, each address stores four display bits. Figure 13 shows how the addresses correspond to the display segments of the LP-3566-B.

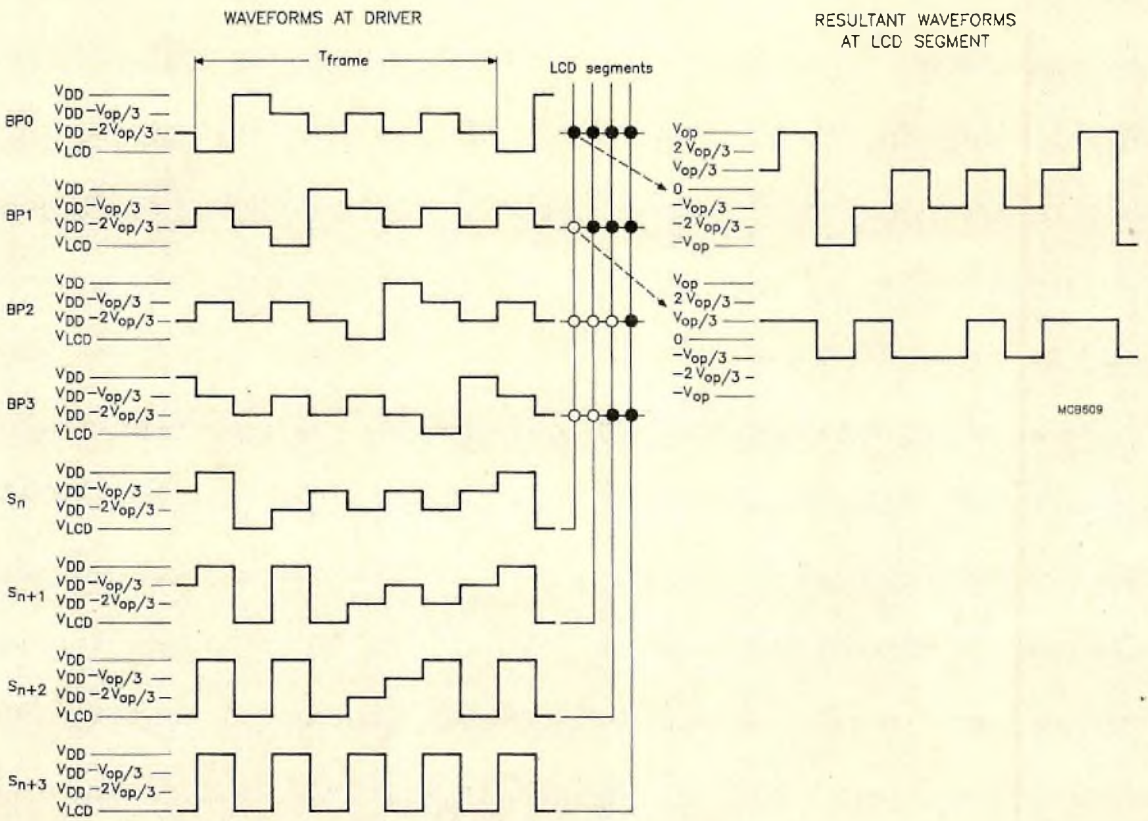
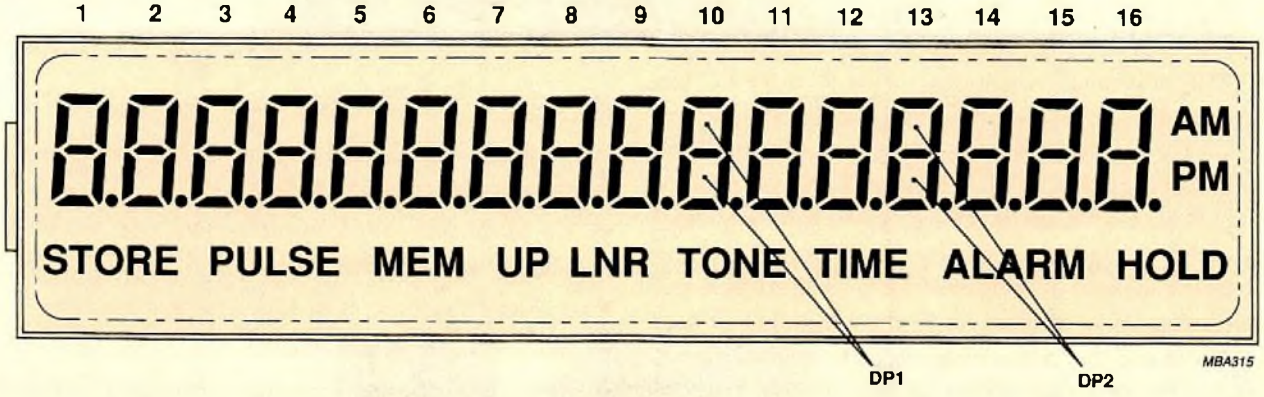
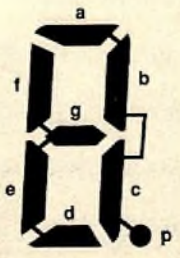
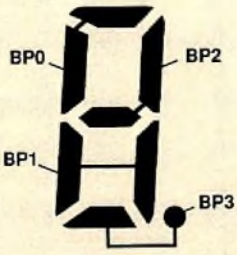


Fig.12 Illustration of the drive waveforms required by the LP-3566-B







RAM address	data byte							
	MSB							LSB
00	–	–	DP1	–	AM	PM	DP2	HOLD
02	a16	c16	b16	P16	f16	e16	g16	d16
04	a15	c15	b15	P15	f15	e15	g15	d15
06	a14	c14	b14	P14	f14	e14	g14	d14
08	–	–	–	ALARM	–	–	–	TIME
0A	a13	c13	b13	P13	f13	e13	g13	d13
0C	a12	c12	b12	P12	f12	e12	g12	d12
0E	a11	c11	b11	P11	f11	e11	g11	d11
10	a10	c10	b10	P10	f10	e10	g10	d10
12	a9	c9	b9	P9	f9	e9	g9	d9
14	–	–	–	TONE	–	–	–	LNR
16	a8	c8	b8	P8	f8	e8	g8	d8
18	a7	c7	b7	P7	f7	e7	g7	d7
1A	a6	c6	b6	P6	f6	e6	g6	d6
1C	a5	c5	b5	P5	f5	e5	g5	d5
1E	–	UP	–	MEM	–	STORE	–	PULSE
20	a4	c4	b4	P4	f4	e4	g4	d4
22	a3	c3	b3	P3	f3	e3	g3	d3
24	a2	c2	b2	P2	f2	e2	g2	d2
26	a1	c1	b1	P1	f1	e1	g1	d1
backplane	BP0	BP1	BP2	BP3	BP0	BP1	BP2	BP3

Fig.13 The display data is stored in RAM so that the location of each bit corresponds to the relevant backplane

Memory control

The *input bank selector* controls the way display data is stored in RAM. The command byte LOAD DATA POINTER determines where data received on the I²C-bus is to be stored by setting the data pointer to the relevant address. The auto-incrementing addressing system allows a large string of data to be loaded in RAM following a single LOAD DATA POINTER command byte. The input bank selector handles data in 8-bit bytes. For 1:4 multiplex, each byte is split into two four-bit nibbles and stored at successive memory locations. When the first byte has been stored, the data pointer is incremented by two, ready for the next two nibbles of display data from the I²C-bus.

The *output bank selector* automatically reads out data from RAM to control the display segment outputs. These are set according to the contents of the display latch which must be updated at a rate determined by the internal clock frequency. The *output bank selector* reads one bit from each memory location from RAM and loads it in the shift register. When full, the shift register empties its contents into the display latch, in time to control the display segment outputs during the next backplane cycle. For 1:4 multiplex, the output bank selector operates in four cycles, transferring in every cycle the bit from each memory location that corresponds to the selected backplane output.

Cascaded operation

Thanks to the PCF8576 design, up to eight of them can operate on the same I²C-bus with the same address. In this configuration, all controllers on the bus act on the same command bytes but control different LCDs with the same MUX rate and bias. This type of operation, known as cascaded operation, is made possible by inputs A0, A1 and A2 which are tied HIGH or LOW to give each RAM in the cascade a unique sub-address. The sub-address for each data message is determined by the DEVICE SELECT command. The LP-3566-B has A0, A1 and A2 are tied LOW and does not allow cascaded operation.

Illustrated operation

Table 2 is an example of the operating sequence needed to control the LP-3566-B. The table shows the messages which must be sent on the I²C-bus to display a telephone number plus a few function words. Operation of the control electronics for sending these messages is not described here.

Power-on

When power is switched on, the PCF8576 resets to a defined starting condition as follows:

- all backplane and segment outputs are set to V_{DD} (display switched off)
- the drive mode is set to MUX 1:4 and 1/3 bias
- blinking mode is deselected
- the data pointer and sub-address counter are cleared.

1 ms after power-on, the LP-3566-B is ready to receive information from the I²C-bus.

Command and data message

After power-on, the control electronics activates the display by sending a message string as shown in Table 2. Message transfer is begun by sending a START condition on the I²C-bus followed by the slave address byte for the PCF8576. The next byte sent must be one of the command bytes in Fig.11.

Immediately after power-on, the following command bytes must be sent:

- the MODE SET command to indicate the type of LCD to be controlled.
- the LOAD DATA POINTER command to indicate the address of the first data byte
- the DEVICE SELECT command to set the sub-address counter to 000.

Messages sent later need only contain the LOAD DATA POINTER command together with a string of display data. The only other command byte relevant to the LP-3566-B is BLINK MODE which can be sent at any time to set the blink frequency.

Table 2 shows the command byte sequence after power-on. In the last command byte, bit C is set to logic 0 to indicate that any further bytes will be data for transfer to RAM. After power-on the PCF8576 should receive a complete set of display data so that all display segments are precisely defined. The message is terminated by a STOP condition from the control electronics.

TABLE 2

Message sequence to control the LP-3566-B

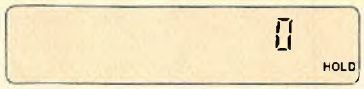
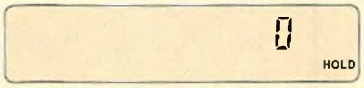
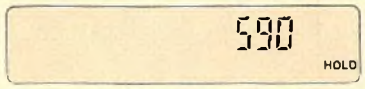
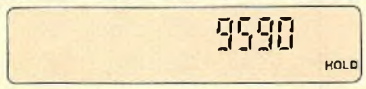
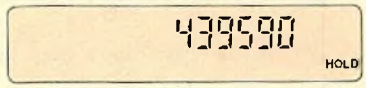
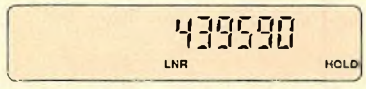
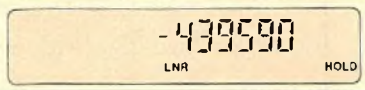
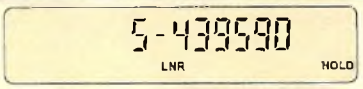
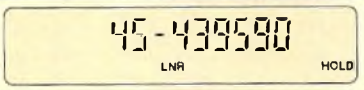
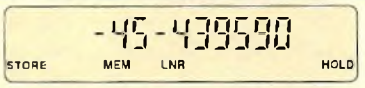
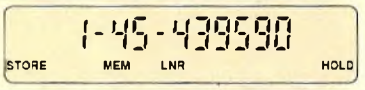
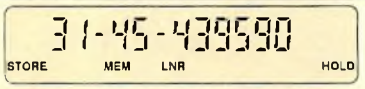
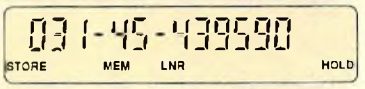
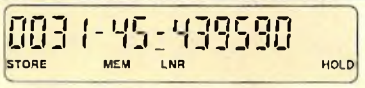
message on I²C-bus	byte (binary)	HEX	action
1 Power on			The module is initialised. No display.
2 START condition			The PCF8576 compares the next byte on the I²C-bus with its slave address.
3 Slave address	01110000	70	The PCF8576 is set ready to receive control bytes from the I²C-bus.
4 Mode set	11001000	C8	The LCD drive is set to MUX 1:4 and 1/3 bias. The display is enabled and normal power mode is selected.
5 Load data pointer	10000000	80	The data pointer is set to address 00 (HEX) in display RAM.
6 Device select	11100000	E0	The hardware sub-address of the LP-3566-B is selected (A2,A1,A0 = 0,0,0).
7 Blink mode	01110000	70	Blinking is switched off and with MSB (the control bit C) 0. the PCF8576 prepares to receive display data.
8... 20 Display data			The next 20 bytes of display data are written into RAM so that the LCD is driven to make the required display. The drawings below illustrate how each display byte contributes to the final display. In practice, the display is formed instantaneously.
8	00000001	01	
9	00000000	00	
10	00000000	00	
11	11101101	ED	
12	00000000	00	
13	11101011	EB	
14	11001011	CB	
15	11101011	EB	
16	11100011	E3	
17	01101010	6A	
18	00000001	01	
19	00000010	02	

TABLE 2 continued

message on I²C-bus	byte (binary)	HEX	action
20	11001011	CB	
21	01101010	6A	
22	00000010	02	
23	00010100	14	
24	01100000	60	
25	11100011	E3	
26	11101101	ED	
27	11101101	ED	
28 STOP condition			The PCF8576 accepts no more bytes from the I²C-bus.

QUALITY ASPECTS

To ensure reliable operation, all Philips LCDs are subjected to a number of environmental and mechanical tests before being released for distribution. The following tests are especially relevant to chip-on-foil modules:

- the foil solderability test to ensure that the module connection is able to withstand soldering
- the pull-strength and peel-off-strength tests for ensuring the quality of the LCD-to-foil bond (see Figs.14 and 15)
- the vibration and bump tests to ensure the quality of the chip-to-foil bond.

To allow customers to make a choice according to application, we supply Chip-on-foil modules in two climatic categories

- *commercial* – for operation under normal environmental conditions
- *extended* – for applications where the display will be subjected to extremes of temperature and humidity.

Modules in both climatic categories must pass our rigorous and extensive test procedures, although for some tests the requirements for commercial grade products are less demanding. Table 3 lists the product release tests for chip-on-foil modules.

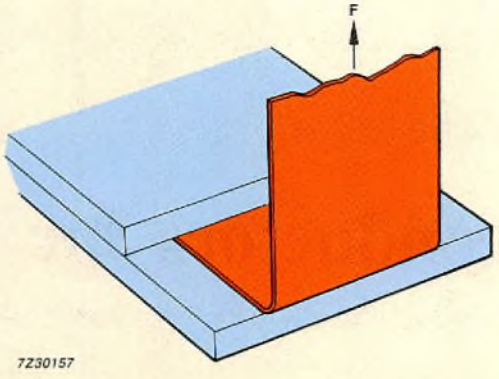


Fig.14 Peel-off-strength test

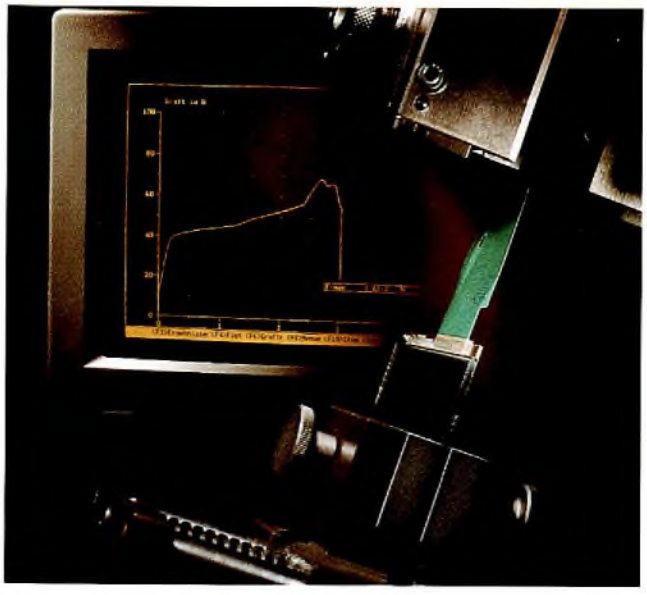


Fig.15 Pull-strength test

TABLE 3
Product release tests for chip-on-foil modules[1]

test name	test description according to climatic category	
	commercial	extended
high temperature storage (IEC 68-2-2: Test Bb)	+70 °C for 21 days	+90 °C for 21 days
low temperature storage (IEC 68-2-1: Test Ab)	−25 °C for 21 days	−40 °C for 21 days
damp heat, steady state (IEC 68-2-3: Test Ca)	+40 °C/90% RH for 21 days	+80 °C/90% RH for 21 days
change of temperature (IEC 68-2-14: Test Na)	−10 °C for 30 min. followed by +70 °C for 30 min. repeated × 10	−25 °C for 30 min. followed by +85 °C for 30 min. repeated × 10
low air pressure	+25 °C/500 mbar for 24 hours	+25 °C/500 mbar for 24 hours
high air pressure	+60 °C/5 bar for 1 hour	+60 °C/5 bar for 1 hour
leakage and seal line adhesive strength	+25 °C in freon for 3 hours	+25 °C in freon for 3 hours
vibration (IEC 68-2-6: Test Fc)	10 sweeps from 10 to 150 and back to 10 Hz in X, Y and Z directions at 3 mm peak-to-peak amplitude 10-55 Hz with a constant amplitude of 0.75 mm 55-150 Hz with a constant acceleration of 10 g	10 sweeps from 10 to 150 and back to 10 Hz in X, Y and Z directions at 3 mm peak-to-peak amplitude 10-55 Hz with a constant amplitude of 0.75 mm 55-150 Hz with a constant acceleration of 10 g
bump (IEC 68-2-29: Test Eb)	6 ms/40 g peak repeated × 1000	6 ms/40 g peak repeated × 1000
foil solderability (IEC 68-2-20: Test Tb)	260 °C for 10 seconds	260 °C for 10 seconds
peel-off-strength[2]	5 N/cm	5 N/cm
pull-strength	40 N/cm	40 N/cm
sulphur dioxide test (IEC 68-2-42: Test Kc)	–	25 °C/75% RH/25 ppm for 10 days
UV light exposure	1.1 kW Xenon tube at 20 cm for 100 hours	1.1 kW Xenon tube at 20 cm for 100 hours
full functional test	+60 °C for 500 hours	+85 °C for 500 hours

[1] test conditions for future LCD modules may vary from this table
[2] tested before making environmental tests

ICs and Discrete Semiconductors for TV and VCR Tuners

NICO BAARS

Development of TV and VCR tuners is a lengthy specialist task that requires extensive TV-systems experience combined with a full understanding of sensitive high-frequency mixer/oscillator circuitry. However, the tuner designer's task is greatly simplified if the more difficult circuitry is integrated. This is why we have developed our wide range of mixer/oscillator ICs for highly-integrated tuners, supported by integrated PLL frequency synthesizers and prescalers (frequency dividers) for complete TV tuning systems. We also have small-signal bipolar transistors and MOSFETs, diodes for tuning, mixing and band-switching, and a comprehensive range of passive components.

All Philips components are backed by our world-wide research and manufacturing facilities and benefit from our unrivalled experience as pioneers of surface-mount technology. Our total commitment to quality embodies aims such as zero defects and includes quick remedial action based on customer feedback in the unlikely event of any defects escaping our intensive screening during manufacture.

MIXER/OSCILLATOR ICs FOR TV AND VCR TUNERS

Whenever standards authorities (e.g. Cenelec, West German FTZ and Amtsblatt, or the American FCC) change, or introduce, compulsory 'recommendations' for the operating characteristics of TV tuners, circuit designers are put under extreme pressure to satisfy the new requirements. Although it's possible to develop a prototype TV tuner within a few months, refining the design to satisfy all existing and new national or international standards usually involves making many prototypes which can easily take up to two years. For example, the West German Amtsblatt specification, which will soon become the basis for most European standards, demands a very low level of tuner local-oscillator signal at the aerial input. Also, the selectivity of the tuner has to be increased to achieve the low permitted levels of intermodulation and cross-modulation.

The design of the mixer/oscillator section of a TV tuner has always been a particularly delicate compromise. Requirements must be met for handling a wide range of input signal levels, covering an extended frequency range and reducing spurious radiation. This is where we have come to the designer's rescue by crystallizing the solutions to all these problems in our comprehensive range of mixer/oscillator ICs listed in Table 1.

TABLE 1
Mixer/oscillator ICs for TV and VCR tuners

type	package	band coverage
TDA5030A	DIL18	VHF/hyper
TDA5030AT	SO20	VHF/hyper
TDA5330T	SO28	VHF/hyper/UHF
TDA5331T	SO28	VHF/hyper/UHF
TDA5332T	SO20	VHF/hyper/UHF
TDA5333T	SO20	VHF/hyper/UHF
TDA5630FT	SSOP20	VHF/hyper/UHF
TDA5630T	SO20	VHF/hyper/UHF

By integrating the VHF, hyperband and UHF mixer/oscillator sections of a TV tuner, we have improved the performance and reliability of tuners and cut design time by up to 60%. Our mixer/oscillator ICs also allow TV tuner designers to reduce costs by:

- achieving design repeatability due to small spreads
- reducing assembly time
- more easily satisfying CENELEC, German FTZ/Amtsblatt and American FCC requirements
- simplifying stock control
- determining the IF selectivity with an external SAW filter, thereby allowing the tuner to be adapted to any TV standard.

Frequency bands covered by our mixer/oscillator ICs

The frequency limits of the conventional VHF bands I/III + CATV "S" channels, hyperband and the UHF band are not optimum for tuning with unswitched LC circuits incorporating variable-capacitance diodes. The frequency bands covered by our mixer/oscillator ICs are therefore designated as the 'low-band' (45 to 180 MHz VHF), the 'mid-band' (160 to 470 MHz VHF + hyperband) and the 'high-band' (430 to 860 MHz UHF). Figure 1 shows how these frequency bands have been allocated and indicates the frequency coverage of all our mixer/oscillator ICs.

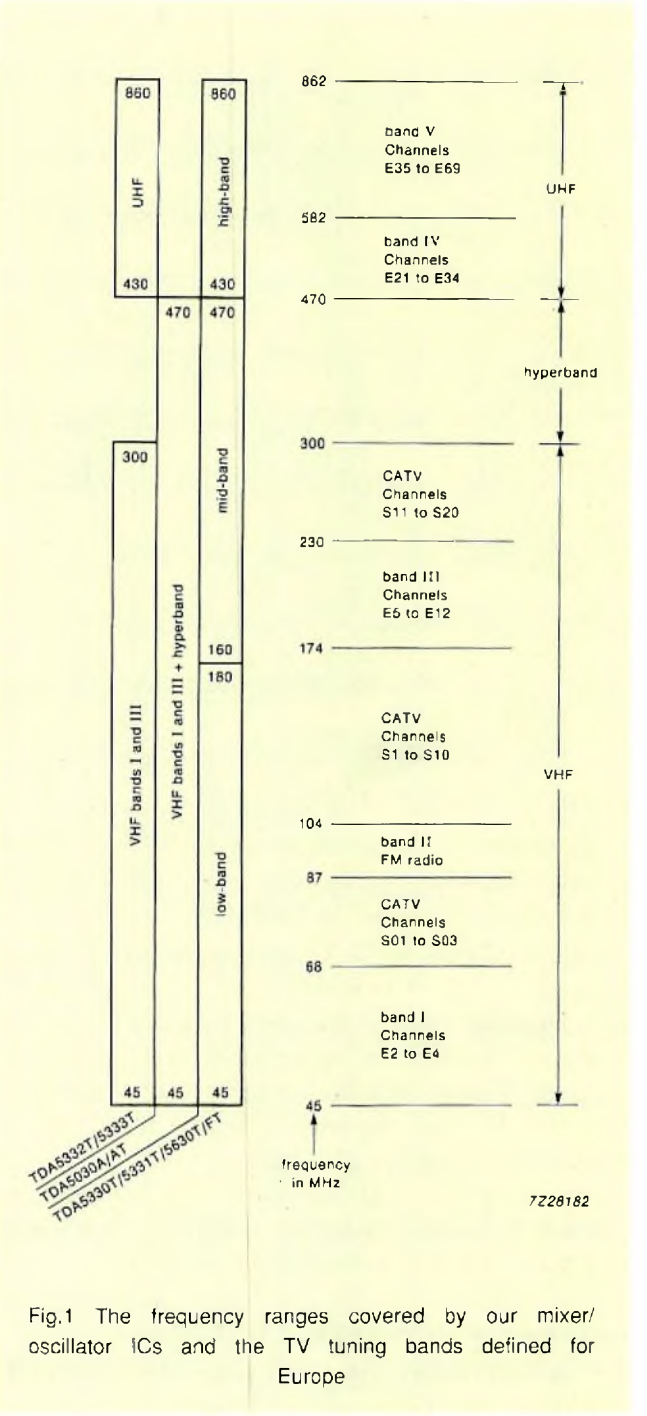


Fig.1 The frequency ranges covered by our mixer/oscillator ICs and the TV tuning bands defined for Europe.

Mixer/oscillator ICs for VHF + hyperband TV tuners

TDA5030A/AT

The TDA5030A was the first in our family of integrated mixer/oscillators for TV tuners. Manufactured with a high-frequency bipolar oxide-isolated process, it was the first single-chip mixer/oscillator capable of covering an uninterrupted frequency range from 45 to 470 MHz; encompassing VHF band I, VHF band III, the CATV "S" channels and the hyperband. The TDA5030A is in an 18-pin DIL package and the TDA5030AT is in a 20-pin small outline (SO) package for surface mounting. Both ICs operate from a single 12 V supply over the temperature range −25 to +80 °C.

The basic circuit arrangement of a TV tuner using one of these ICs is shown in simplified form in Fig.2.

Some important features of the TDA5030A/AT mixer/oscillator ICs are:

- balanced VHF + hyperband mixer
- amplitude-controlled VHF + hyperband local-oscillator which makes the design of the peripheral oscillator circuitry extremely simple
- buffered output from the local-oscillator for driving a prescaler (e.g. our SAB6456 or SAB6457), or PLL frequency synthesizer (e.g. one of our TSA551x family)
- IF preamplifier for the IF signal from an external UHF mixer
- IF amplifier with an output for connection to an external SAW filter
- voltage stabilizer

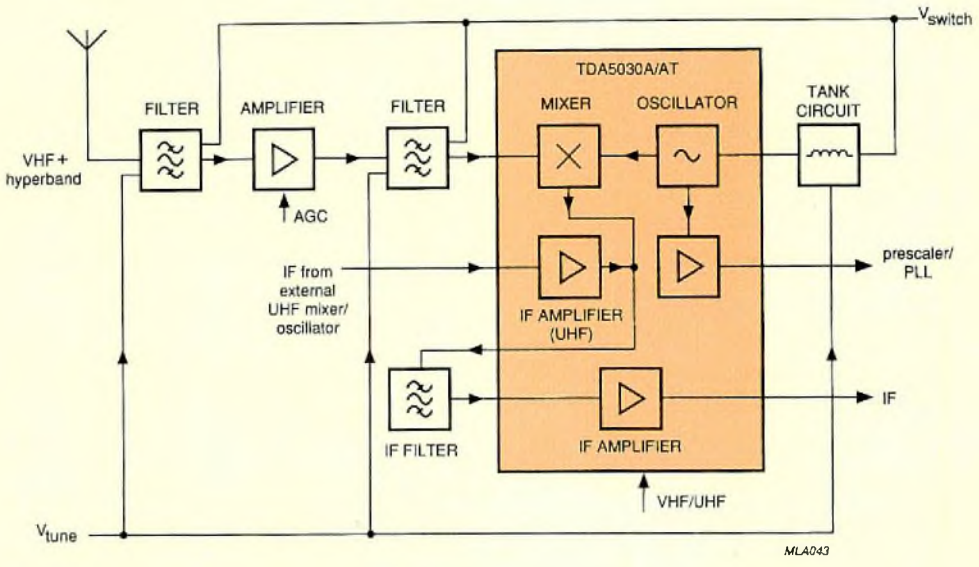


Fig.2 Basic circuit arrangement of a TV tuner using the VHF + hyperband mixer/oscillator IC TDA5030A/AT

- VHF + hyperband/UHF band-switching circuit
- electrostatic discharge protection diodes on the band switching input, the buffered local-oscillator output, and the IF outputs to the SAW filter.

The block diagram of Fig.3 shows an all-band TV tuner incorporating the TDA5030A, and also indicates the most important discrete semiconductors which we can supply to complete the components package for the tuner. A discrete-transistor oscillator and a Schottky-barrier diode mixer are used to extend the frequency coverage to include the UHF band.

The peripheral VHF/hyperband tuned-circuits are switched by discrete diodes and the VHF + hyperband/UHF band switching is incorporated in the IC.

Three-band mixer/oscillator ICs for all-band tuners

Our all-band mixer/oscillator ICs are the TDA5330T/TDA5331T and the low-power TDA5630T/FT. Suited to the highest standards of colour television design, they all cover the entire frequency range 45 to 860 MHz in three bands; the low-band (45 to 180 MHz), the mid-band (160 to 470 MHz) and the high-band (430 to 860 MHz). Since these bands encompass VHF, the hyperband and UHF, these ICs obviate the need for the 30 to 40 discrete components that would be required to build peripheral UHF or hyperband mixer and oscillator circuitry if the previously described TDA5030A/AT mixer/oscillator ICs were used in an all-band TV tuner.

Outstanding features of our all-band mixer/oscillator ICs are:

- balanced, common-emitter high-impedance input stage with internal feedback for the low-band to ensure good signal handling properties
- balanced common-base low-impedance input stages for mid and high-bands to allow designers to choose their own compromise between noise, signal handling properties and gain by adapting the source impedance
- double-balanced mixer and voltage-controlled local-oscillator for each band
- IF preamplifier with an output impedance of less than 100 Ω for connection to an external SAW filter
- buffered all-band local-oscillator output which provides an extremely pure symmetrical or asymmetrical drive signal for an external prescaler (e.g. SAB645x family) or PLL frequency synthesizer (e.g. TSA551x family)
- bandgap voltage stabilizer and temperature compensation circuitry to ensure oscillator stability
- three-band (low, mid, high-band) electronic switching circuit
- electrostatic discharge protection diodes on the band switching input and IF output pins.

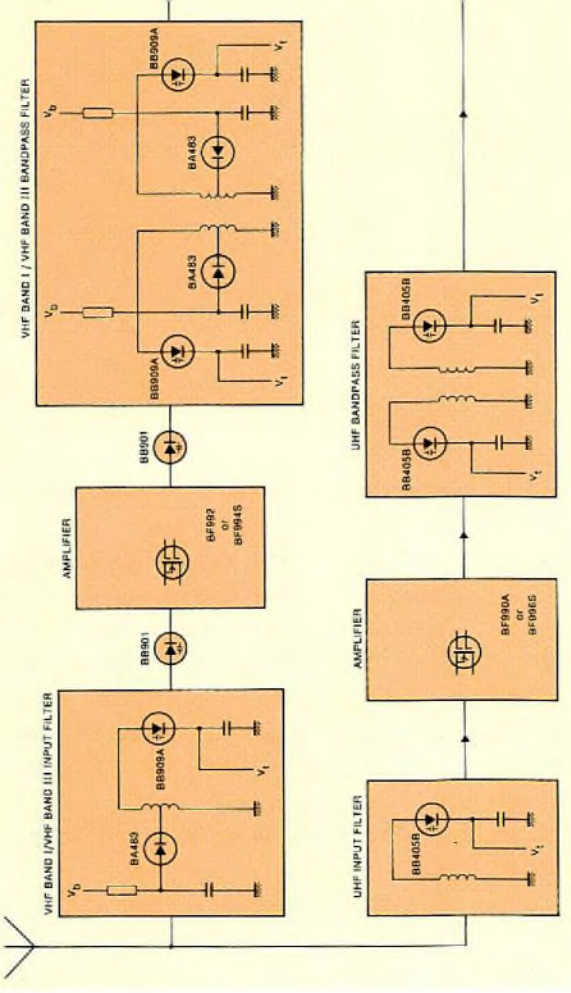
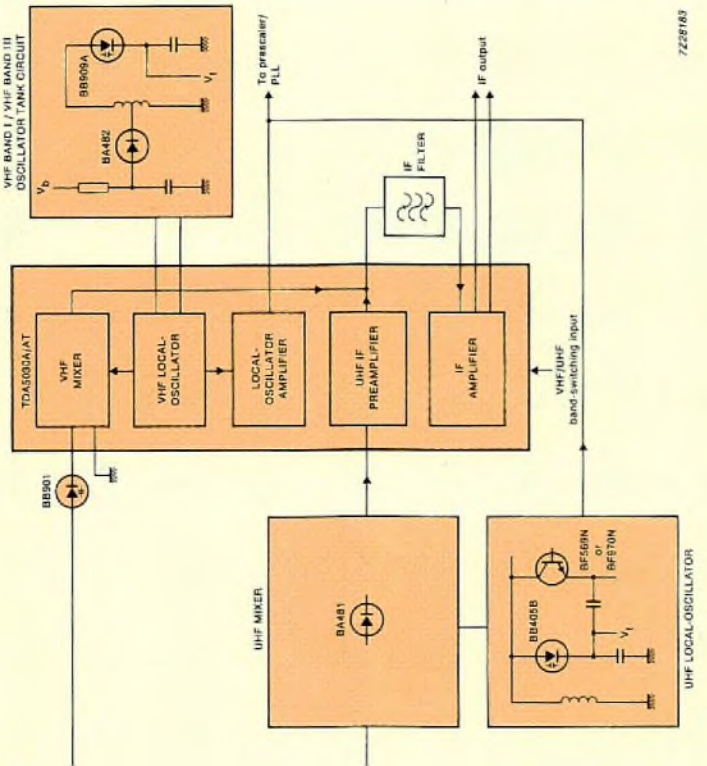


Fig.3 A TV tuner using the TDA5030A mixer/oscillator IC for VHF band I/III + CATV "S" channels, and a discrete-component mixer/oscillator for UHF. V_t is the tuning voltage for the filters and oscillator tank circuit. V_b is the band-switching voltage


VHF BAND I / VHF BAND III OSCILLATOR TANK CIRCUIT
BB609A
BA482
V_b
V_t
To prescaler/ PLL
IF output
IF FILTER
TDA5030A/AT
VHF MIXER
VHF LOCAL-OSCILLATOR
LOCAL-OSCILLATOR AMPLIFIER
UHF IF PREAMPLIFIER
IF AMPLIFIER
VHF/UHF band-switching input
BB901
UHF MIXER
BA481
BB405B
BF569N or BF670N
UHF LOCAL-OSCILLATOR
7Z28183

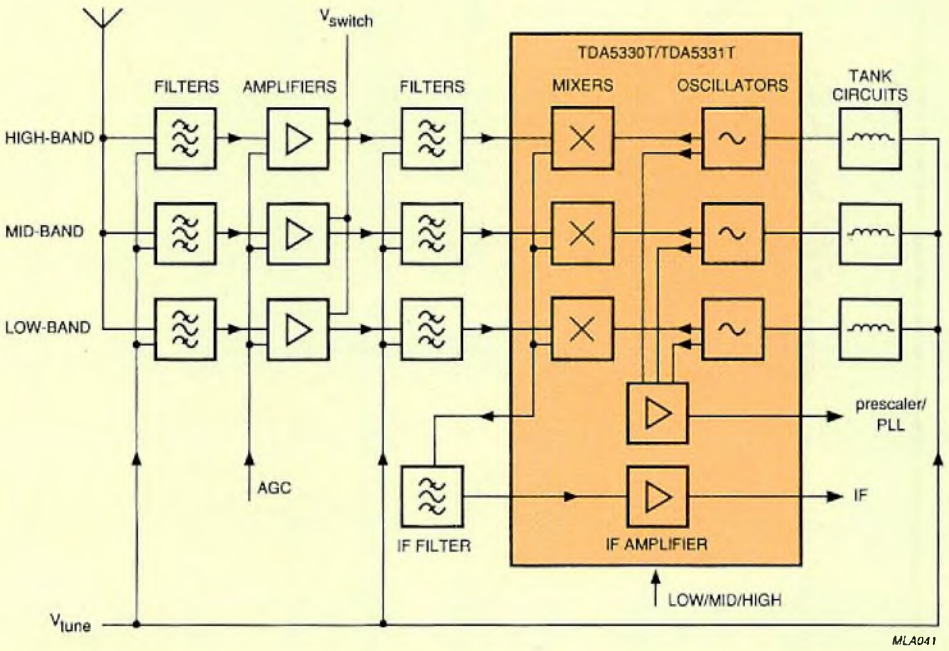


Fig.4 Basic circuit arrangement of a TV tuner using an all-band mixer/oscillator IC TDA5330T or TDA5331T

TDA5330T/TDA5331T

These all-band mixer/oscillator ICs both perform the same functions but the TDA5331T has mirror-image pinning to allow an alternative board layout. Both are in plastic 28-pin small outline packages. They consume about 500 mW from a single 12 V supply and have an operating temperature range of −25 to +80 °C.

The basic circuit arrangement of a TV tuner using one of these ICs is shown in simplified form in Fig.4.

At the inputs to the IC, RF signals from each of the three input bands are processed by dedicated symmetrical input stages, each followed by a double-balanced mixer which eliminates the fundamental frequencies and even harmonics of the RF and local-oscillator signals, as well as suppressing the 'first repeat spot', the 'channel 6 beat', and the incoming IF.

The RMS output at the tank circuit of the asymmetrical low-band oscillator is controlled at about 500 mV. Since this level is an order of magnitude less than the output from a similar circuit built with discrete components, it reduces non-linearity, thereby improving the stability of the oscillator.

The mid and high-band symmetrical oscillators are formed from differential amplifiers with cross-coupled feedback. This symmetry, and the symmetry of the input stages eliminates spurious HF currents in the supply/ground lines and reduces interaction between the RF and oscillator signals, thereby minimizing oscillator pulling, spurious frequency modulation of the oscillators and radiation from the aerial.

The block diagram of an all-band tuner given in Fig.5 includes a simplified block diagram of the TDA5330T/TDA5331T and also shows the most important discrete semiconductors which we can supply to complete the components package for the tuner.

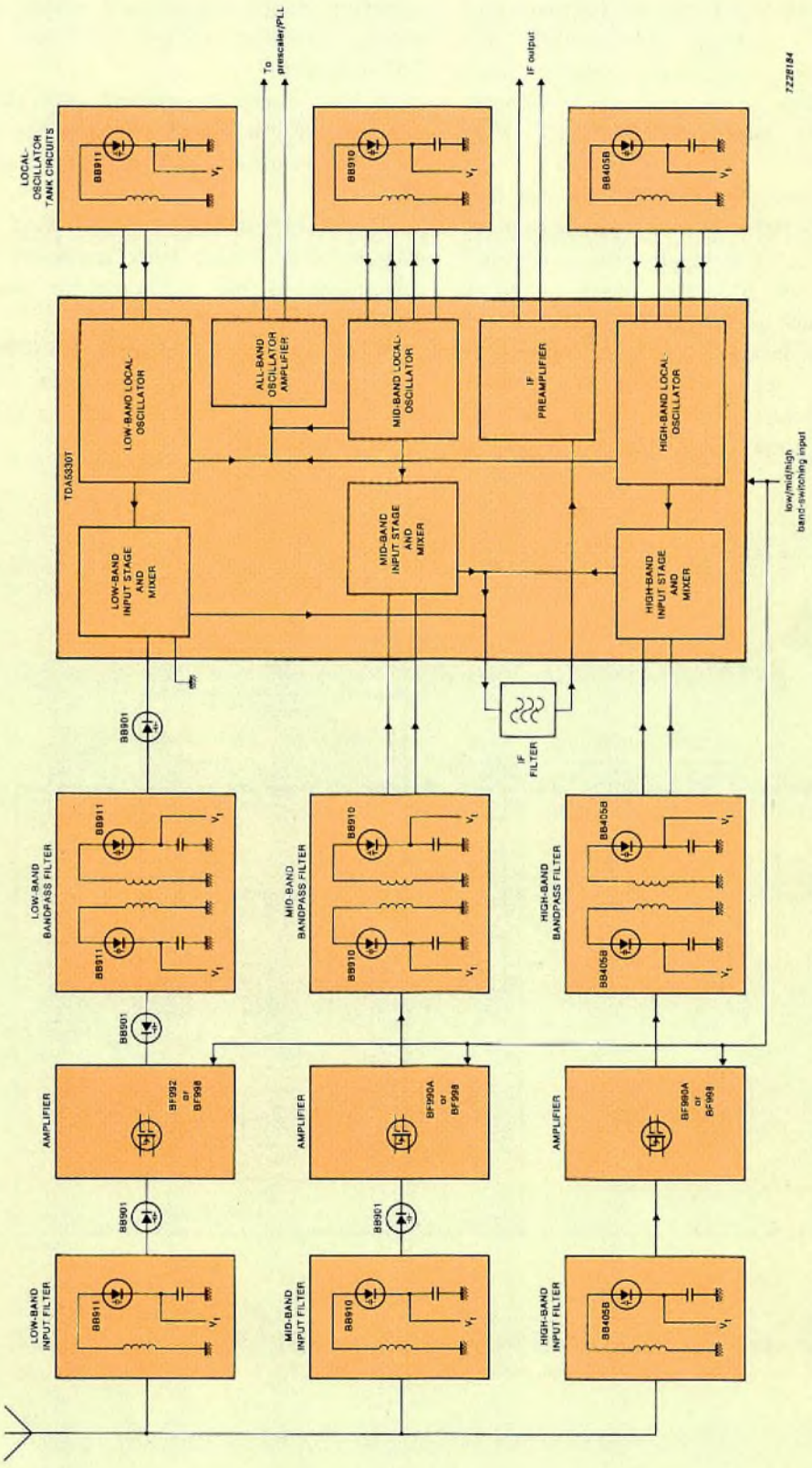


Fig.5 A highly-integrated all-band TV tuner using the TDA5330T mixer/oscillator IC. V_t is the tuning voltage for the filters and oscillator tank circuits

TDA5630T/FT

The TDA5630T/FT perform all the functions of the previously described TDA5330T but are forerunners of a new generation of all-band mixer/oscillator ICs specifically intended for very small economy tuners which can nevertheless meet the most stringent specifications such as those of CENELEC, FTZ/ Amtsblatt and the FCC.

These ICs differ from the TDA5330T in that they consume less power (<300 mW) and operate from an 8 V supply instead of a 12 V supply. Also, since they don't need an external IF filter, fewer peripheral components and IC pins are required. Another difference is that all three local-oscillators are formed by differential amplifiers with cross-coupled feedback instead of the low-band oscillator being amplitude controlled. Instead of being in a plastic 28-pin SO package like the TDA5330T, the TDA5630T is in a plastic 20-pin SO package and the TDA5630FT is in a miniature 20-pin shrink small outline plastic (SSOP) package measuring only 4.4 × 6.5 mm^2 with pins on a 0.65 mm pitch.

A basic circuit arrangement of a TV tuner using a TDA5630T/FT is shown in simplified form in Fig.6 Note that an external IF filter isn't necessary for these ICs.

The TDA5630T/FT can be used in the block diagram of a 3-band tuner shown in Fig.5, but the connections to the local-oscillator tank circuits are slightly different as shown in Fig.7.

If hyperband is not required, the TDA5630T/FT can also be used in a VHF/UHF tuner with three tuned circuits; one for VHF band I, one for VHF band III and the other for UHF.

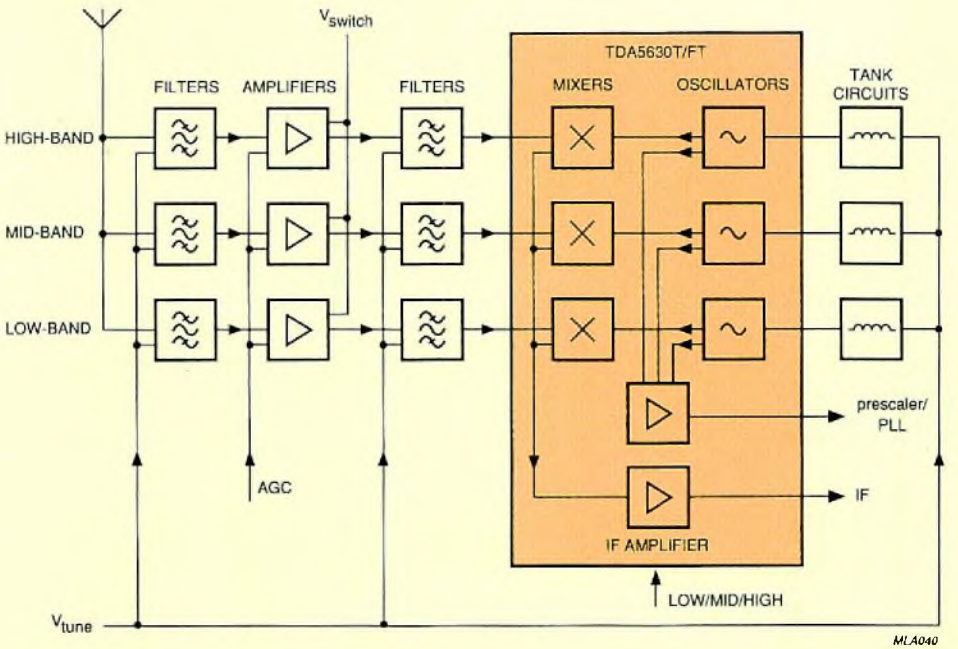


Fig.6 Basic circuit arrangement of a highly-integrated all-band TV tuner using a low-power mixer/oscillator IC TDA5630FT

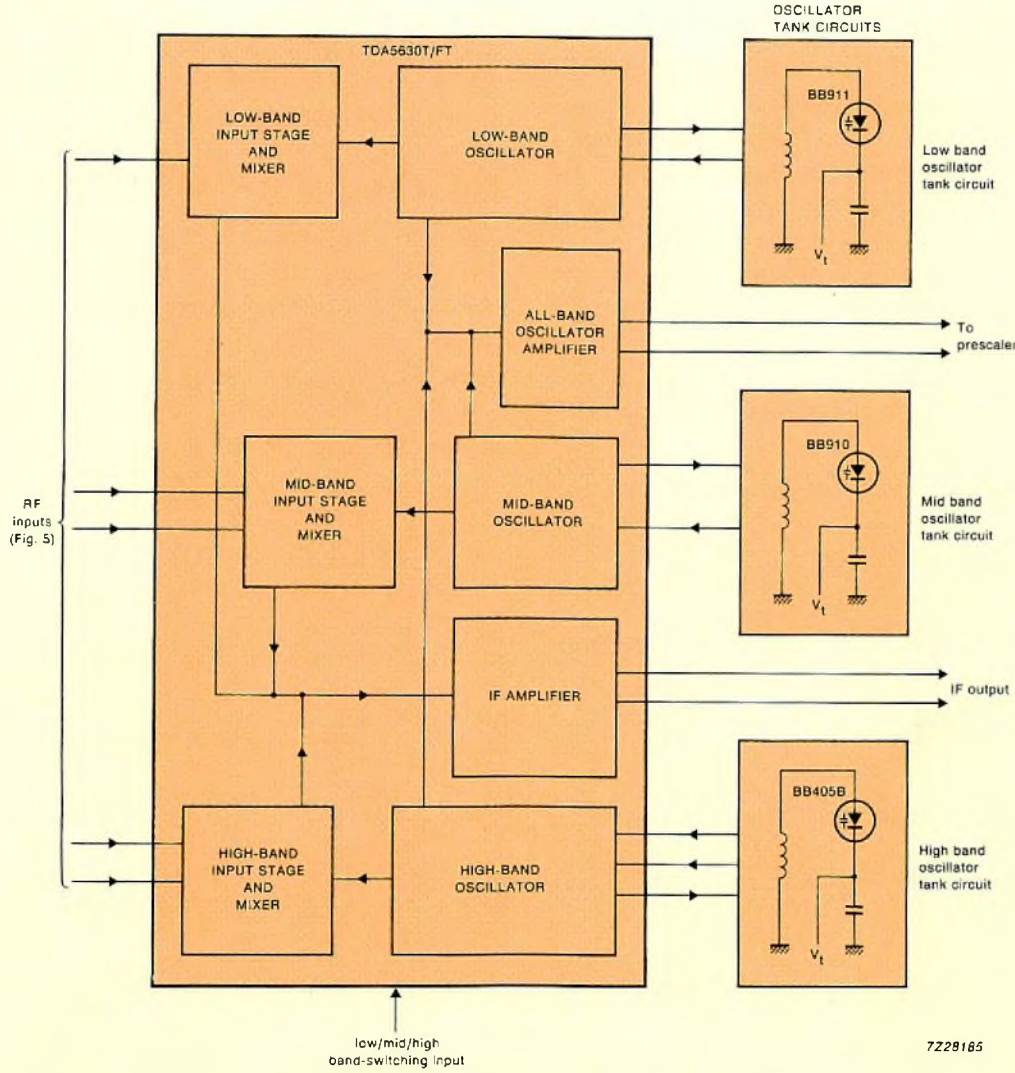


Fig.7 Local-oscillator tank circuit connections when the low-power mixer/oscillator IC TDA5630FT is used in place of the TDA5330T in Fig.5. V_t is the tuning voltage for the oscillator tank circuits

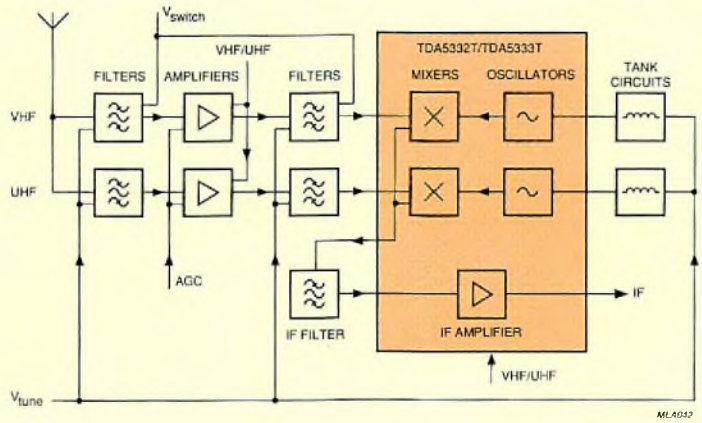


Fig.8 Basic circuit arrangement of a TV tuner using a VHF/UHF mixer/oscillator IC TDA5332T or TDA5333T

Two-band mixer/oscillator ICs for VHF/UHF tuners

TDA5332T/TDA5333T

These mixer/oscillator ICs are two-band (VHF/UHF) versions of the previously described TDA5330T and TDA5331T with all the same features but without a separate buffered output from the local-oscillators. The basic circuit arrangement of a TV tuner using one of these ICs is shown in simplified form in Fig.8.

Although these ICs are specified to cover the frequency bands 45 to 470 MHz and 160 to 860 MHz, in most applications the hyperband will be excluded and the IC will be used to cover VHF bands I and III plus the CATV "S" channels (45 to 300 MHz), and the UHF band (430 to 860 MHz).

Both ICs are in plastic 20-pin small outline (SO) packages for surface mounting and operate from a single 12 V supply over the temperature range −25 to +80 °C. The TDA5333T has mirror-image pinning to allow an alternative board layout.

PLL FREQUENCY SYNTHESIZER ICs

Figure 9 is a simplified block diagram of a complete TV/VCR tuning system in which our mixer/oscillator ICs can be used. The tuning loop is closed by a low power (5 V, 35 mA) single-chip 1.3 GHz PLL frequency synthesizer from our TSA551x family (TSA5511, TSA5512 and TSA5514). A microcontroller in the TV set/VCR selects the frequency bands and

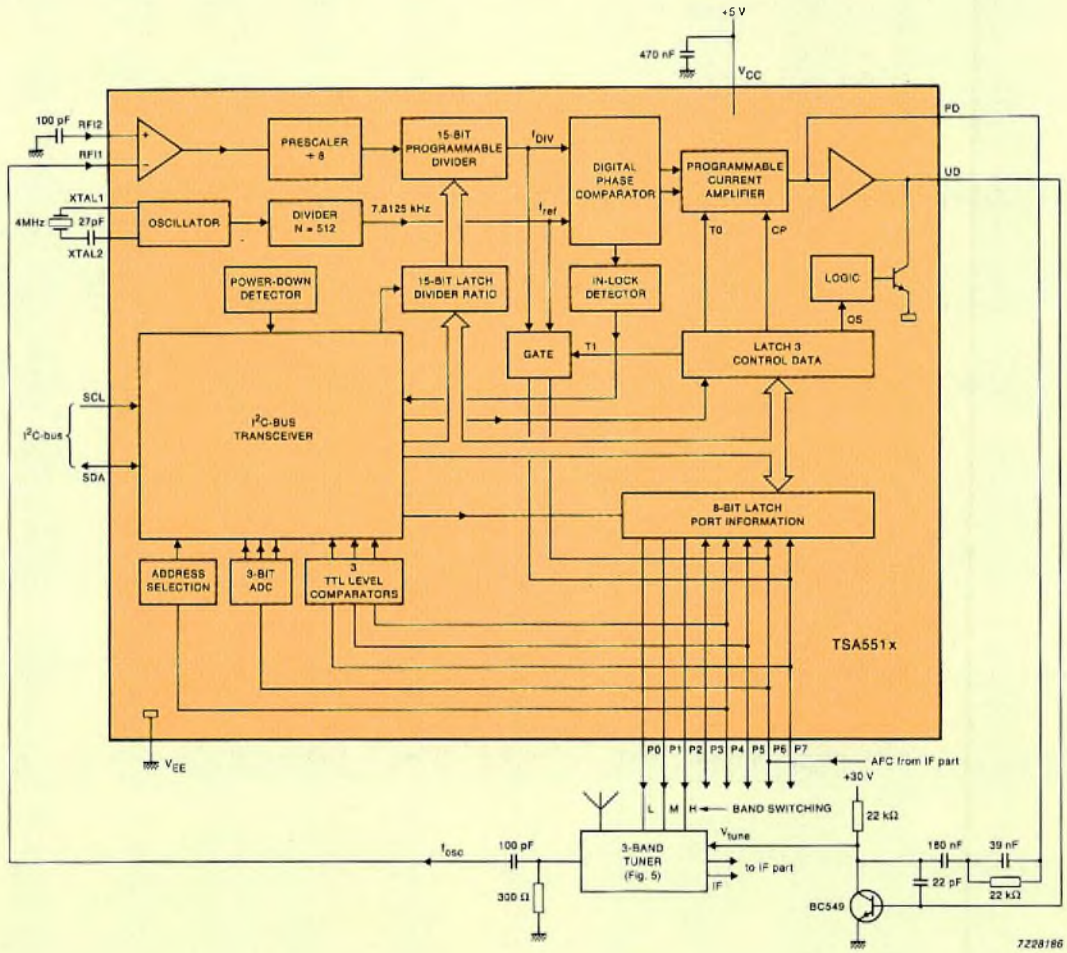


Fig.9 A complete television tuning system using one of our mixer/oscillator ICs together with a PLL frequency synthesizer from our TSA551x family

controls the tuning voltage via the simple two-wire serial I^2C-bus interface of the TSA551x.

All three members of the TSA551x family are available in three different plastic packages; DIL18, SO16 (small) and SO20 (large). They all feature a very low level of radiation and are identical except for the port configurations and addresses.

The TSA5511 has 4 open-collector I/O ports and 4 current-limited ports; 3 of the current-limited ports are outputs and one is bidirectional. It has 1 fixed and 3 voltage-programmable addresses.

The TSA5512 has 8 open-collector ports; 5 are bidirectional and 3 are outputs. It has 1 fixed and 3 voltage-programmable addresses.

The TSA5514 is the same as the TSA5512 except that it has 7 open-collector ports and four programmable addresses.

Unique features of our TSA551x family of integrated PLL frequency synthesizers are:

- tuning loop in-lock flag
- charge-pump output disable for alignment purposes
- fixed/voltage-programmable addresses for multi-tuner applications such as Picture-in-Picture (PIP), DBS tuner etc.
- 5-level ADC for sending AFC information from the IF part of the TV to the microcontroller
- power-down flag

Table 2 shows the functional variations and pinning arrangements for the three types of package in which the TSA5511, TSA5512 and TSA5514 are available

TABLE 2
Pinning and pin functions of the TSA551x family of PLL frequency synthesizers

TSA551xAT (SO20) pin number	TSA551x (DIL18) pin number	TSA551xT (SO16) pin number	pin name	pin function
1	1	1	PD	charge pump output (active loop filter feedback)
2	2	2	XTAL1	crystal-controlled oscillator input 1
3	3	3	XTAL2	crystal-controlled oscillator input 2
4	n.a.	n.a.	n.a.	not connected
5	4	4	SDA	I^2C-bus data line
6	5	5	SCL	I^2C-bus clock line
7	6	6	P7	I/O port 7
8	n.a.	n.a.	n.a.	not connected
9	7	7	P6	I/O port 6
10	8	8	P5	I/O port 5
11	9	9	P4	I/O port 4
12	10	10	P3	output port 3 or address selection input *
13	11	11**	P2	output port 2
14	12	n.a.	P1	output port 1
15	13	n.a.	P0	output port 0
16	14	12	V_{CC}	5 V supply
17	15	13	RFI1	input for VHF/UHF signals
18	16	14	RFI2	RF input amplifier reference
19	17	15	V_{EE}	supply return (ground)
20	18	16	UD	tuning voltage drive output

n.a. = function not applicable

* only an address selection input on TSA5514

** not connected on TSA5511T

Data formats for the TSA551x family

Control data are written to the frequency synthesizer, via the I²C-bus, in five serial bytes as follows:

- address byte
- two bytes for selecting the local-oscillator frequency by programming the division ratio of the 15-bit divider
- a byte for activating the 8 (7 for TSA5514) open-collector ports or setting them to the high-impedance state
- a byte for setting the charge-pump current to 50 µA or 220 µA, enabling/disabling the tuning voltage drive output, and connecting f_{ref} and f_{DIV} (see Fig.9) to ports P6 and P7 respectively for test purposes.

Data bytes can be sent to the IC consecutively without an interposing address byte until the microcontroller sends an I²C-bus STOP condition. This allows a smooth frequency sweep for fine tuning or AFC purposes. Since the VHF/UHF input to the frequency synthesizer from the mixer/oscillator IC is divided by 8, the smallest possible frequency step is 8 times f_{ref} (4 MHz/512 = 7.8125 kHz) = 62.5 kHz. If a minimum frequency step of 50 kHz is required, a 3.2 MHz crystal can be used.

The address and status can be read as two bytes. The status byte includes:

- a power-on reset flag which is set at power-on or if V_{CC} <3 V
- PLL in-lock flag
- digital information for ports P4, P5 and P7
- the 3-bit AFC data from the ADC.

Control program for the TSA551x family

As part of our customer support package for ICs, we have an I²C-bus control program called IICPLL (on 5¼" or 3½" diskette) which allows engineers to evaluate, analyze and test the functions of the TSA551x family of PLL frequency synthesizers. All that's needed to run this program is an IBM compatible PC with MS-DOS/PC-DOS and at least 512 kbytes of RAM, and a simple interface board that we can provide for connection between the parallel CENTRONICS port of the PC and the test board. Further information about this program and the interface board is given in our brochure "I²C-bus control programs for consumer applications", ordering code 9398 362 90011.

PRESCALER ICs

Our range of prescaler ICs for TV and VCR tuners comprises:

SAB6456	sensitive 1 GHz ÷64/÷256 switchable prescaler; plastic DIL package
SAB6456T	as SAB6456 but in a plastic small outline (SO) package for surface mounting
SAB6456A	1.3 GHz, low-spike version of the SAB6456
SAB6456AT	as SAB6456A but in a plastic small outline (SO) package for surface mounting
SAB6457	as SAB6456 but pin-compatible with our TDA551x family of PLL frequency synthesizer ICs.

FURTHER INFORMATION ABOUT OUR ICs FOR TV AND VCR TUNERS

Further details of our mixer/oscillator ICs, integrated PLL frequency synthesizers, and prescaler ICs is given in Data Handbooks IC01 and IC02 which can be obtained from your local Philips representative.

DISCRETE SEMICONDUCTORS FOR TV AND VCR TUNERS

By introducing dual-gate n-channel MOSFETs BF988/BF998 and variable-capacitance diodes in SOD123 plastic encapsulations for the VHF and UHF bands, we have now completed our range of discrete semiconductors for building entirely discrete component TV tuners, or highly-integrated TV tuners using a mixture of discrete components and mixer/oscillator ICs.

Our diodes for tuning, mixing and band switching, embody some of the most advanced techniques in the semiconductor industry. They are manufactured under CECC-approved conditions, and many have full CECC release. All our diodes and MOSFETs are available for either through-hole or surface mounting, allowing circuit designers to satisfy a whole range of design criteria. Advanced production techniques and strict quality-control procedures ensure long-term reliability renowned throughout the industry. Furthermore, all our semiconductors are supported by extensive applications know-how gained during our long experience of manufacturing RF components.

The following overview lists our discrete semiconductors for TV and VCR tuners according to their envelopes.

Variable-capacitance diodes

The main features of all our variable-capacitance diodes for TV and VCR tuners are:

- small capacitance drift with temperature
- extremely smooth C/V characteristic
- wide variety of tuning ranges
- low leakage current
- smooth, well-controlled C_d range
- both leaded types for through-hole mounting or surface-mounting types are available.

Dual-gate n-channel MOSFETs

Our dual-gate n-channel MOSFETs for TV and VCR tuners are listed in Table 4. Their main features are:

- low input capacitance
- high transfer conductance
- low noise
- excellent gain control
- silicon-nitride glass barrier passivation for high reliability
- integrated back-to-back protection diodes.

TABLE 3
Variable-capacitance diodes for TV and VCR tuners

	leaded diodes		surface-mount diodes			
Envelope →	SOD27	SOD68	SOD80	SOT23	SOT143	SOD123
Application ↓						
AFC	BB119					
		BB417				
VHF		BB809		BBY40		
		BB909A/B	BB219	BBY42		BB619
		BB910	BB240			
		BB911	BB241			BB620
			BB249			
				BB901		
UHF		BB405B	BB215	BBY31		BB515
				BBY39		
					BBY62	
Satellite				BBY39		
						BB811

TABLE 4
Dual-gate n-channel MOSFETS for TV and VCR tuners

	Envelope		Characteristics			
Application	SOT103	SOT143	Y_{fs} @ f = 1 kHz (ms)	C_{is} typical (pF)	C_{os} typical (pF)	F typical (dB)
VHF	BF964S	BF994S	15	2.5	1.0	1.0
	BF965	BF997	15	2.5	1.0	1.0
	BF981	BF991	10	2.1	1.1	0.7
	BF982	BF992	20	4.0	2.0	1.2
	BF988	BF998	24	2.1	1.05	1.0
UHF	BF960	BF989	9.5	1.8	0.9	2.8
	BF966S	BF996S	15	2.3	0.8	1.8
	BF980A	BF990A	18	2.6	1.2	2.0
	BF988	BF998	24	2.1	1.05	1.0

Bipolar transistors

Table 5 lists our range of bipolar transistors for TV and VCR tuners:

TABLE 5
Bipolar transistors for TV and VCR tuners

Envelope			Application
TO92	SOT37	SOT23	
Type			
BF496			gain-controlled VHF pre-amplifier
BF748		BF747	oscillator in VHF/UHF tuners
	BF970N	BF569N	self-oscillating mixer in UHF tuners
	BF979	BF579	UHF applications
BF926			preamplifier, mixer, oscillator in VHF/UHF tuners
BF506			preamplifier, mixer, oscillator in VHF/UHF tuners
		BF660	oscillator in VHF tuners
		BFS17	VHF/UHF applications

Band switching diodes

Table 6 lists our band switching diodes for TV and VCR tuners.

TABLE 6
Band switching diodes for TV and VCR tuners

Envelope			Characteristics	
DO35	SOD80	SOD123	r_s @ I_f = 3 mA, f = 200 MHz (Ω)	C_d @ V_r = 3 V, f = 100 MHz (pF)
Type				
BA482	BA682		<0.7	<1.2
BA483			<1.2	<1.0
BA484			<1.2	<1.6
	BA683		<1.2	<1.2
		BA582	<0.7	<1.1

Schottky-barrier mixer diode

Table 7 shows the characteristics of our BA481 Schottky-barrier mixer diode for TV and VCR tuners.

TABLE 7
Schottky-barrier mixer diode for TV and VCR tuners

		Characteristics		
		V_f @ 1 mA	R_s @ f = 1 kHz, I_f = 5 mA	C_d @ V_r = 0 V
		(mV)	(Ω)	(pF)
Type	Envelope			
BA481	DO34	450	13	1.1

Further information about discrete semiconductors and passive components for TV and VCR tuners

For further details about our discrete semiconductors and passive components for TV and VCR tuners, reference should be made to the appropriate Data Handbooks which are available from your local Philips representative.

Abstracts

ICs and Discrete Semiconductors for TV and VCR Tuners
This article shows how the lengthy specialist task of designing TV and VCR tuners is much simplified if the most difficult circuitry is integrated. The article describes our wide range of mixer/oscillator ICs and shows how they can be used in restricted-band and all-band highly-integrated tuners. It also shows how the tuners can be incorporated in complete TV tuning systems by adding a selection from our range of integrated PLL frequency synthesizers and prescalers. To complete, the information, a list is given of our small-signal bipolar RF transistors and MOSFETs, and our diodes for tuning, mixing and band-switching.

Analog multi-standard colour decoder ICs TDA4650 and TDA4660
A multi-standard TV colour decoder is based on the well-known and successful TDA4557 colour decoder which is adapted to a 64 µs glass delay line. The TDA4650 identifies and demodulates CVBS/S-VHS chrominance signals but is adapted to the baseband colour-difference comb filters contained in a new IC – the TDA4660. The two comb filters are CMOS switched-capacitor delay lines that sample and store a complete horizontal line of colour-difference signal values. All internal clocks are locked to the line frequency so that the comb filter delays are automatically synchronized to the input line frequency. The comb filters are therefore optimized for all colour standards without having to be switched. The comb filters eliminate cross-colour interference for the NTSC colour standard.

Logic-level FETs
The Philips Components' range of rugged L^2FETs allows cost-effective drive-circuit design without compromising ruggedness or reliability. Since they enable power loads to be driven directly from logic ICs they can be considered as the first step towards intelligent power switching. Thanks to their good reliability and 175 °C T_{jmax} temperature rating, they are displacing mechanical relays in automotive body electrical functions, and are now being used in such safety critical areas as ABS (anti-lock braking systems).

ICs for electronically tuned car radios
This article describes how we have extended the horizons of car radio design with a state-of-the-art set of ICs for electronically-tuned car radios. The chip set is partitioned with the aim of avoiding peripheral interfaces and meeting specific car radio requirements such as unconditional stability, minimal wiring, high input sensitivity, elimination of elaborate AM/FM window detection circuitry for search tuning, and avoidance of spurious feedback. A description is given of demonstration circuitry and software for an AM/FM stereo electronic car radio in which the tuning system, frequency display, stored station memory and audio functions are microcomputer-controlled via the simple bidirectional two-wire Inter IC (I^2C) bus.

Chip-on-foil – the flexible approach to LCD modules
A major feature of the LCD is its very thin profile, making it the first choice for hand-held applications such as telephones and pagers, where space is restricted. But conventional LCD modules have the drive electronics mounted on a PCB at the rear of the display, so the overall module thickness is much greater than that of the LCD itself. By bonding the driver IC(s) directly to flexible film and bonding this to one side of the LCD, Philips have produced a much thinner and more adaptable LCD module – the chip-on-foil module. This article shows how chip-on-foil modules are made and, taking a telephone display as an example, gives all the necessary information for connecting the module and controlling it via an I^2C-bus.

Analoge Multistandard-Farbdecoder-ICs TDA4650 und TDA4660
Der Multistandard-Farbdecoder für Fernsehgeräte basiert auf dem bekannten und weitverbreiteten Farbdecoder TDA4557, der an eine parameterunabhängige 64-µs-Verzögerungsleitung angepaßt ist. Der TDA4650 identifiziert und demoduliert FBAS/S-VHS-Chrominanzsignale, ist aber an die Basisband-Farbdifferenz-Kammfilter im neuen IC, dem TDA 4660, angepaßt. Die beiden Kammfilter bestehen aus Verzögerungsleitungen mit geschaltetem CMOS-Kondensator, die Farbdifferenz-Signalwerte einer kompletten horizontalen Zeile abtasten und speichern. Alle internen Takte sind mit der Zeilenfrequenz verriegelt, so daß die Kammfilter-Verzögerungen automatisch mit der Eingangszeilenfrequenz synchronisiert werden. Die Kammfilter sind daher für alle Farbnormen geeignet und müssen nicht umgeschaltet werden. Sie eliminieren auch Farbinterferenzen beim NTSC-Standard.

Logikpegel-FETs
Mit den robusten L^2FETs von Philips Components lassen sich Treiberschaltungen realisieren, ohne irgendwelche Kompromisse bezüglich Zuverlässigkeit der Schaltungen unter erschwerten Betriebsbedingungen eingehen zu müssen. Da mit diesen Bauelementen Lasten direkt von Logik-ICs getrieben werden können, sind sie als erster Schritt zu intelligenten Leistungsschaltern zu betrachten. Dank ihrer hohen Zuverlässigkeit und Temperaturfestigkeit aufgrund T_{jmax} = 175 °C können sie mechanische Relais für elektrische Funktionen in Kraftfahrzeugen ersetzen und werden bereits jetzt in sicherheitskritischen Bereichen, wie dem Anti-Blockier-System (ABS), eingesetzt.

ICs für Autoradios mit elektronischer Senderabstimmung
In diesem Artikel werden die neuen Möglichkeiten für die Konzipierung von Autoradios beschrieben, die ein moderner IC-Satz für Autoradios mit elektronischer Abstimmung bietet. Der Chipsatz wurde so zusammengestellt, daß periphere Schnittstellen möglichst vermieden werden und spezifische Autoradio-Anforderungen – wie hohe Empfangsstabilität, minimaler Verdrahtungsaufwand, hohe Eingangsempfindlichkeit, Eliminierung der komplizierten AM/FM-Fenster-Detektorschaltung für den Suchlauf sowie Vermeidung von störenden Rückkopplungen – erfüllt werden. Es wird eine Beispielschaltung mit der zugehörigen Software für ein elektronisches AM/FM-Stereo-Autoradio vorgestellt, bei dem das Abstimmsystem, die Frequenzanzeige, der Vorzugssender-Speicher und die Audiofunktionen über den einfachen bidirektionalen Zweidraht-I^2C-Bus gesteuert werden.

Folien-Chips – die flexible Lösung für LCD-Module
LCDs (Flüssigkristallanzeigen) zeichnen sich vor allem durch ihre außerordentlich flache Bauweise aus, die sie besonders für tragbare Geräte, wie Telefone und Rufempfänger, geeignet macht, in denen nur wenig Raum zur Verfügung steht. Bei herkömmlichen LCD-Modulen ist die Treiberelektronik auf einer Leiterplatte an der Rückseite des LCD montiert, wodurch das gesamte Modul wesentlich dicker wird als die LCD-Anzeige selbst. Philips hat nun Folien-Chip-Module entwickelt, bei denen die Treiber-ICs direkt auf eine flexible Folie gebondet werden und diese wiederum mit einer Seite des LCD verbunden wird, so daß man erheblich flachere und besser adaptierbare LCD-Module erhält. Dieser Beitrag beschreibt, wie die Folien-Chip-Module gefertigt werden. Am Beispiel eines Telefon-Displays wird erläutert, wie das Modul angeschlossen und über einen I²C-Bus gesteuert wird.

ICs und Diskrete Halbleiter für Fernseh- und Videorecorder-Tuner
Dieser Beitrag beschreibt, wie sich der zeitaufwendige Entwurf von Fernseh- und Videorecorder-Tunern wesentlich vereinfachen läßt, indem die kompliziertesten Schaltungen integriert werden. In diesem Artikel wird unser umfassendes Angebot an Mischer/Oszillator-ICs vorgestellt und erläutert, wie sie in hochintegrierten Schmalband- und Breitband-Tunern eingesetzt werden können. Darüber hinaus wird gezeigt, wie die Tuner mit Hilfe unserer integrierten PLL-Frequenzsynthesizer und Verteiler in kompletten Fernseh-Abstimmsystemen eingesetzt werden können. Zusätzlich sind auch unsere bipolaren Kleinsignal-HF-Transistoren und MOSFETs sowie unsere Abstimm-, Misch- und Bandumschaltungsdioden aufgeführt.

Les circuits intégrés décodeurs couleur multistandard analogiques TDA4650 et TDA4660.
Le nouveau décodeur TV couleur multistandard, le TDA4650, est basé sur le décodeur couleur bien connu et testé TDA4557, qui est adapté à une ligne à retard en verre de 64 µs. Le TDA4650 identifie et démodule les signaux de chrominance CVBS/S-VHS, mais il est adapté aux filtres en peigne de différence de couleur de bande de base contenus dans un nouveau circuit intégré, le TDA4660. Les deux filtres en peigne sont des lignes à retard CMOS à condensateur commuté, qui échantillonnent et mettent en mémoire les valeurs des signaux de différence de couleur d'une ligne horizontale complète. Toutes les horloges internes sont verrouillées sur la fréquence de ligne, de sorte que les retards des filtres en peigne sont synchronisés automatiquement avec la fréquence de ligne d'entrée. Les filtres en peigne sont donc optimisés pour tous les standards couleur sans avoir à être commutés. Les filtres en peigne éliminent la diaphotie luminance/chrominance pour le standard couleur NTSC.

Transistors FET à niveau logique
Les robustes transistors L²FET de la gamme produite par la division Composants de Philips permettent de réaliser des circuits de commande ayant un bon rapport efficacité-coût sans compromettre la robustesse ni la fiabilité. Permettant la commande directe de courants forts par des circuits intégrés logiques, ils peuvent être considérés comme la première étape vers la commutation de puissance intelligente. Grâce à leur bonne fiabilité et à leur caractéristique de température T_{jmax} de 175 °C, ils supplantent les relais mécaniques dans les applications aux circuits électriques des véhicules et on les emploie maintenant dans des domaines critiques pour la sécurité tels que les systèmes ABS d'anti-blocage des freins.

Des circuits intégrés pour autoradios à syntonisation électronique
Cet article décrit comment nous avons élargi les possibilités de réalisation des autoradios par la mise au point d'un ensemble évolué de circuits intégrés pour autoradios à syntonisation électronique. Le jeu de puces est cloisonné pour éviter les interfaces périphériques et satisfaire aux impératifs spécifiques des autoradios tels que stabilité inconditionnelle, minimum de câblage, haute sensibilité d'entrée, simplification de la détection de fenêtres AM/FM pour la recherche d'émetteurs, et absence de contre-réaction parasite. On décrit les circuits de démonstration et un logiciel pour un autoradio électronique stéréophonique AM/FM dans lequel les fonctions de syntonisation d'affichage de fréquence, de présélection d'émetteurs et audio sont gérées par microprocesseur par l'intermédiaire du bus directionnel I²C.

Le module à puce sur film – approche flexible des afficheurs à cristaux liquides
Une importante caractéristique des afficheurs à cristaux liquides est leur faible épaisseur, qui les rend idéals pour les applications, telles que la téléphonie et les systèmes de recherche de personnes, qui demandent des appareils récepteurs très compacts. Mais, dans les modules à cristaux liquides conventionnels, les circuits de commande sont montés sur une carte de circuit imprimé à l'arrière de l'afficheur, de sorte que l'épaisseur globale du module est bien plus grande que celle de l'afficheur lui-même. En collant directement le ou les circuits intégrés drivers sur un film flexible et en collant ce dernier sur une des faces de l'afficheur à cristaux liquides, Philips a réalisé un module d'affichage bien plus mince et bien plus adaptable – le module à puce sur film. L'article montre comment de tels modules sont réalisés et, prenant un afficheur de téléphone comme exemple, donne toutes les informations nécessaires pour connecter le module et le commander par l'intermédiaire d'un bus I²C.

Circuits intégrés et semiconducteurs discrets pour tuners de téléviseurs et de magnétoscopes
Cet article montre à quel point la tâche fastidieuse et spécialisée qu'est la conception des tuners de téléviseurs et de magnétoscopes est simplifiée, si les circuits les plus complexes sont intégrés. L'article décrit notre importante gamme de circuits intégrés mélangeurs/oscillateurs et montre comment les utiliser dans des tuners à bande restreinte et toutes bandes à haut niveau d'intégration. Il montre également comment les tuners peuvent être incorporés à des systèmes complets de syntonisation TV en ajoutant quelques synthétiseurs de fréquence PLL et des circuits prédiviseurs. En complément d'information, on trouvera une liste de nos transistors RF bipolaires et MOSFET pour petits signaux et de nos diodes de syntonisation, de mélange et de commutation de bande.

Circuitos integrados decodificadores multinorma de color TDA4650 y TDA4660

Un decodificador de color multinorma para TV se basa en el conocido y acreditado decodificador de color TDA4557, que se adapta a una línea de retardo de cristal de 64 µs. El TDA4650 identifica y demodula las señales de crominancia CVBS/S-VHS, pero está adaptado a los filtros peine de diferencia de color en banda base contenidos en un nuevo CI, el TDA4660. Los dos filtros peine son líneas de retardo de condensador conmutado CMOS que muestrean y almacenan una línea horizontal completa de valores de la señal de diferencia de color. Todos los relojes internos van bloqueados a la frecuencia de línea, de modo que los retardos de filtros peine se sincronizan automáticamente a la frecuencia de línea de entrada. Por consiguiente, los filtros peine están optimizados para todas las normas de color, sin necesidad de conmutación. Los filtros peine eliminan la diafonía cromática de la norma de color NTSC.

Transistores de efecto de campo (FETs) de nivel lógico

La gama de transistores de efecto de campo L^2FETs de Philips Components hace posible el diseño económico de circuitos de excitación sin pérdida de resistencia ni de fiabilidad. Como estos componentes permiten excitar directamente cargas de potencia a partir de circuitos integrados lógicos, pueden considerarse como el primer paso hacia la conmutación inteligente de potencia. Gracias a su gran fiabilidad y a su valor nominal de temperatura igual a 175°C están desplazando a los relés mecánicos en las funciones eléctricas en los automóviles y actualmente se utilizan en áreas críticas de seguridad tales como los sistemas antibloqueo de frenos ABS.

Circuitos integrados para autorradios con sintonía electrónica

Este artículo describe la forma en que hemos ampliado el horizonte del diseño de los autorradios con una serie de CIs de la tecnología más reciente para autorradios sintonizados electrónicamente. El montaje está dividido a fin de evitar interfases periféricas y poder cumplir con los requisitos específicos de los autorradios, tales como la estabilidad incondicional, el cableado mínimo, la alta sensibilidad de entrada, la eliminación de una complicada circuitería de detección de AM/FM para sintonización y el evitar la realimentación parásita. Se da una descripción de la circuitería y el software de demostración para un autorradio electrónico estéreo AM/FM, en el que el sistema de sintonía, la indicación de frecuencia, la memoria de emisoras y las funciones de audio están controladas por microordenador a través de un único bus bidireccional Inter IC (I^2C) de dos hilos.

Chip en lámina: el diseño flexible de módulos visualizadores de cristal líquido (LCD)

Una característica importante del LCD es su muy reducido perfil, por lo que se suele elegir preferentemente para aparatos manuales, como teléfonos y buscapersonas, en los que se dispone de poco espacio. No obstante, los LCD convencionales tienen la electrónica de excitación montada en una placa de circuito impreso en la parte posterior de la pantalla, de modo que el espesor total del módulo es muy superior al del propio LCD. Uniendo los CIs de excitación directamente a una lámina flexible, y ésta a un lado del LCD, Philips ha conseguido fabricar un módulo LCD mucho más estrecho y adaptable: el módulo chip en lámina. En este artículo se ilustra la fabricación de estos módulos y, tomando la pantalla de un teléfono como ejemplo, se da toda la información necesaria para conectar el módulo y controlarlo a través de un bus I^2C.

Circuitos integrados y semiconductores discretos para sintonizadores de TV y Vídeo

Este artículo muestra cómo la ardua y especializada tarea de diseño de sintonizadores de TV y VCR se simplifica sobremanera si se integra la circuitería más difícil. El artículo describe nuestra amplia gama de CIs mezcladores/osciladores, mostrando cómo pueden utilizarse en sintonizadores de banda completa y banda restringida altamente integrados y cómo pueden incorporarse en sistemas completos de sintonía de TV añadiendo un circuito integrado de nuestra gama de sintetizadores de frecuencia PLL y precontadores. Para completar la información, se da una lista de nuestros transistores de RF bipolares y MOSFET para pequeña señal en RF y nuestros diodos para sintonía, mezclado y conmutación de banda.

Authors

Nico Baars was born in Vinkeveen, The Netherlands in 1944. He graduated from the Utrecht Technical School in 1964 and subsequently joined Philips Components' Application Laboratories, where he was responsible for TV tuner and IF applications. In 1982 he became leader of an IC design group at RTC Compelec, Caen, in charge of HF, video and analog bipolar ICs for consumer applications. Since 1987 he has been strategic marketing manager for consumer ICs.

Klaus Juhnke was born in Stettin, Germany in 1938. He graduated in electrical engineering from the Fachhochschule, Hamburg in 1961. Since then he has been a member of the Product Concept and Application Laboratory of Philips Components, Hamburg, working in the television group on system and circuit design and application of colour TV decoders.

Eckhard Bruns was born in Lüneburg, Germany in 1957. He received his Diplom Ingenieur degree from the Fachhochschule, Hamburg in 1982. The same year he joined the development department for telecines in the Bosch Division for professional TV Systems (now BTS) in Darmstadt, Germany. In 1987 he moved to Philips Components' Application Laboratory, Hamburg to work on ICs for colour decoding in TV sets, especially in switched-capacitor technology.

Wim Stijns was born in Brunssum, The Netherlands in 1961. He graduated in 1985 at the Higher Technical School of Heerlen and subsequently joined Philips LCDs in the same town. Working for the Innovation Group, he provided test support for LCD manufacture and quality control. Since 1989 he has given customer support as applications engineer for LCD modules and flat panels.

Arnold Garskamp was born in Rotterdam, The Netherlands in 1936 and graduated in electrical and radio engineering in 1967. After military service, he joined the Central Application Laboratory of Philips Components where he was involved in the application of semiconductors in radio and audio circuits. For the past twelve years, he has concentrated on design techniques for radio circuits intended for subsequent integration.

Arthur Woodworth was born in Manchester in 1945. He took a BSc in electrical engineering at Salford University in 1968 and later that year joined Mullard, Stockport (now Philips Components Ltd.) where he is now head of the Electrical Development Department responsible for the specification and evaluation of a wide range of rectifiers, thyristors, triacs and GTOs. He is currently specializing in the area of automotive products.

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